

## FEATURES

- 25, 35, 45, and 55 ns Read Access & R/W Cycle Times
- Unlimited Read/Write Endurance
- Pin compatible with Industry Standard SRAMs
- Software-initiated Non-Volatile *STORE*
- Automatic *RECALL* to SRAM on Power Up
- Unlimited *RECALL* cycles
- 1 Million *STORE* Cycles
- 100-Year Non-volatile Data Retention
- Single 5V  $\pm$  10% Operation
- Commercial, Industrial, and Military Temperatures
- 28 pin 330 mil SOIC (RoHS-Compatible)
- 28-pin CDIP and LCC packages

## DESCRIPTION

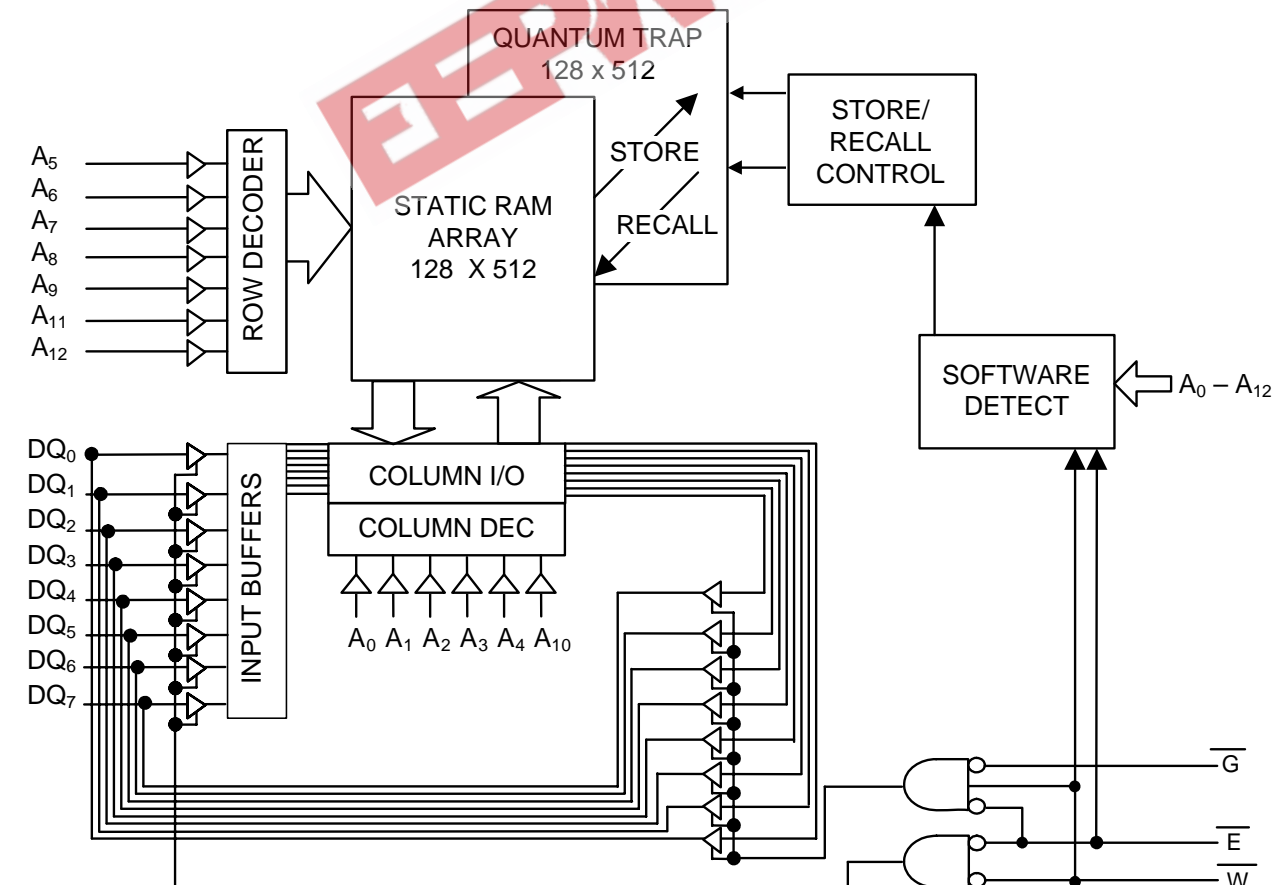
The Simtek STK11C68 is a 64Kb fast static RAM with a nonvolatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use, and unlimited read & write endurance of a normal SRAM.

Data transfers under software control to the non-volatile storage cells (the *STORE* operation). On power-up, data is automatically restored to the SRAM (the *RECALL* operation). *RECALL* operations are also available under software control.

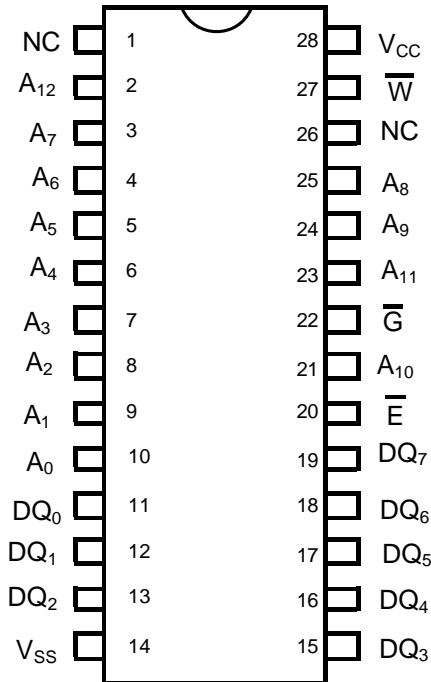
The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

## BLOCK DIAGRAM



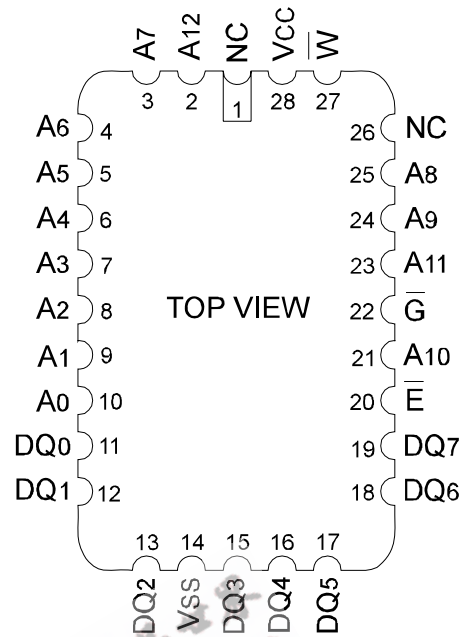
# STK11C68 (SMD5962-92324)

## PIN CONFIGURATIONS



28-Pin DIP

28-Pin SOIC



28-Pin LCC

## PIN NAMES

| Pin Name                         | I/O          | Description  |
|----------------------------------|--------------|--|
| A <sub>12</sub> -A <sub>0</sub>  | Input        | Address: The 13 address inputs select one of 8,192 bytes in the nvSRAM array   |
| DQ <sub>7</sub> -DQ <sub>0</sub> | I/O          | Data: Bi-directional 8-bit data bus for accessing the nvSRAM   |
| $\bar{E}$                        | Input        | Chip Enable: The active low $\bar{E}$ input selects the device   |
| $\bar{W}$                        | Input        | Write Enable: The active low $\bar{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\bar{E}$              |
| $\bar{G}$                        | Input        | Output Enable: The active low $\bar{G}$ input enables the data output buffers during read cycles. De-asserting $\bar{G}$ high caused the DQ pins to tri-state. |
| V <sub>CC</sub>                  | Power Supply | Power: 5.0V, ±10%  |
| V <sub>SS</sub>                  | Power Supply | Ground   |

## ABSOLUTE MAXIMUM RATINGS<sup>a</sup>

|   |   |
|---|---|
| Voltage on Input Relative to Ground                 | .....-0.5V to 7.0V                      |
| Voltage on Input Relative to V <sub>SS</sub>        | ..... -0.6V to (V <sub>CC</sub> + 0.5V) |
| Voltage on DQ <sub>0-7</sub>                        | ..... -0.5V to (V <sub>CC</sub> + 0.5V) |
| Temperature under Bias                              | ..... -55°C to 125°C                    |
| Storage Temperature                                 | ..... -65°C to 150°C                    |
| Power Dissipation                                   | ..... 1W                                |
| DC Output Current (1 output at a time, 1s duration) | ..... 15mA                              |

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 10%)

| SYMBOL                        | PARAMETER   | COMMERCIAL           |                       | INDUSTRIAL/<br>MILITARY |                      | UNITS | NOTES  |
|-------------------------------|---|----------------------|-----------------------|-------------------------|----------------------|-------|--|
|                               |   | MIN                  | MAX                   | MIN                     | MAX                  |       |  |
| I <sub>CC1</sub> <sup>b</sup> | Average V <sub>CC</sub> Current   |                      | 90<br>75<br>65<br>N/A |                         | 90<br>75<br>65<br>55 | mA    | t <sub>AVAV</sub> = 25ns<br>t <sub>AVAV</sub> = 35ns<br>t <sub>AVAV</sub> = 45ns<br>t <sub>AVAV</sub> = 55ns   |
| I <sub>CC2</sub> <sup>c</sup> | Average V <sub>CC</sub> Current during STORE                                      |                      | 3                     |                         | 3                    | mA    | All Inputs Don't Care, V <sub>CC</sub> = max   |
| I <sub>CC3</sub> <sup>b</sup> | Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200ns<br>5V, 25°C, Typical |                      | 10                    |                         | 10                   | mA    | $\bar{W} \geq (V_{CC} - 0.2V)$<br>All Others Cycling, CMOS Levels  |
| I <sub>SB1</sub> <sup>d</sup> | Average V <sub>CC</sub> Current<br>(Standby, Cycling TTL Input Levels)            |                      | 27<br>23<br>20<br>N/A |                         | 28<br>24<br>21<br>20 | mA    | t <sub>AVAV</sub> = 25ns, $\bar{E} \geq V_{IH}$<br>t <sub>AVAV</sub> = 35ns, $\bar{E} \geq V_{IH}$<br>t <sub>AVAV</sub> = 45ns, $\bar{E} \geq V_{IH}$<br>t <sub>AVAV</sub> = 55ns, $\bar{E} \geq V_{IH}$ |
| I <sub>SB2</sub> <sup>d</sup> | V <sub>CC</sub> Standby Current<br>(Standby, Stable CMOS Input Levels)            |                      | 750                   |                         | 1500                 | µA    | $\bar{E} \geq (V_{CC} - 0.2V)$<br>All Others V <sub>IN</sub> ≤ 0.2V or ≥ (V <sub>CC</sub> - 0.2V)  |
| I <sub>ILK</sub>              | Input Leakage Current   |                      | ±1                    |                         | ±1                   | µA    | V <sub>CC</sub> = max<br>V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>  |
| I <sub>OLK</sub>              | Off-State Output Leakage Current  |                      | ±5                    |                         | ±5                   | µA    | V <sub>CC</sub> = max<br>V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\bar{E}$ or $\bar{G} \geq V_{IH}$   |
| V <sub>IH</sub>               | Input Logic "1" Voltage   | 2.2                  | V <sub>CC</sub> + .5  | 2.2                     | V <sub>CC</sub> + .5 | V     | All Inputs   |
| V <sub>IL</sub>               | Input Logic "0" Voltage   | V <sub>SS</sub> - .5 | 0.8                   | V <sub>SS</sub> - .5    | 0.8                  | V     | All Inputs   |
| V <sub>OH</sub>               | Output Logic "1" Voltage  | 2.4                  |                       | 2.4                     |                      | V     | I <sub>OUT</sub> = -4mA  |
| V <sub>OL</sub>               | Output Logic "0" Voltage  |                      | 0.4                   |                         | 0.4                  | V     | I <sub>OUT</sub> = 8mA   |
| T <sub>A</sub>                | Operating Temperature   | 0                    | 70                    | -40                     | 85                   | °C    |  |

Note b: I<sub>CC1</sub> and I<sub>CC3</sub> are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I<sub>CC2</sub> is the average current required for the duration of the STORE cycle (t<sub>STORE</sub>).

Note d:  $\bar{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.

## AC TEST CONDITIONS

|  |                    |
|--|--------------------|
| Input Pulse Levels                       | ..... 0V to 3V     |
| Input Rise and Fall Times                | ..... ≤ 5ns        |
| Input and Output Timing Reference Levels | ..... 1.5V         |
| Output Load                              | ..... See Figure 1 |

## CAPACITANCE<sup>e</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

| SYMBOL           | PARAMETER          | MAX | UNITS | CONDITIONS   |
|------------------|--------------------|-----|-------|--------------|
| C <sub>IN</sub>  | Input capacitance  | 8   | pF    | ΔV = 0 to 3V |
| C <sub>OUT</sub> | Output Capacitance | 7   | pF    | ΔV = 0 to 3V |

Note e: These parameters are guaranteed but not tested.

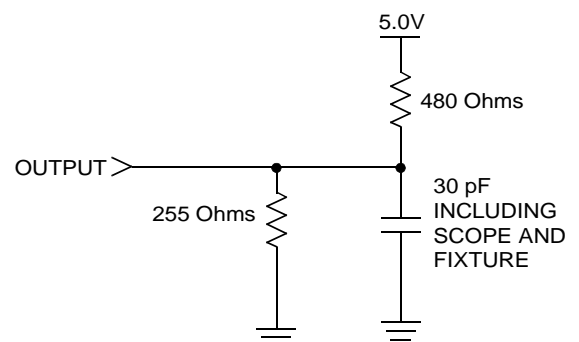


Figure 1: AC Output Loading

# STK11C68 (SMD5962-92324)

## SRAM READ CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )

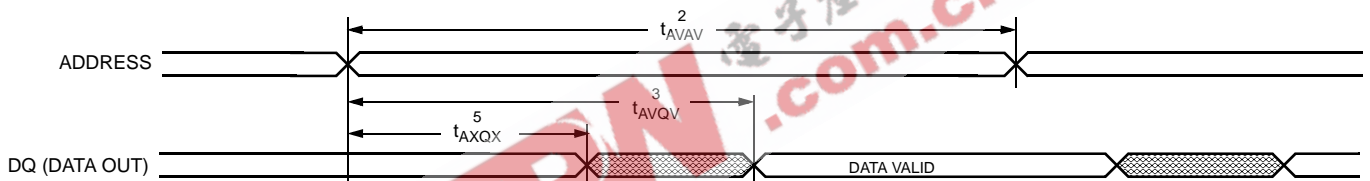
| NO. | SYMBOLS            |           | PARAMETER                         | STK11C68-25 |     | STK11C68-35 |     | STK11C68-45 |     | STK11C68-55 |     | UNITS |
|-----|--------------------|-----------|-----------------------------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------|
|     | #1, #2             | Alt.      |                                   | MIN         | MAX | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |
| 1   | $t_{ELQV}$         | $t_{ACS}$ | Chip Enable Access Time           |             | 25  |             | 35  |             | 45  |             | 55  | ns    |
| 2   | $t_{AVAV}^f$       | $t_{RC}$  | Read Cycle Time                   | 25          |     | 35          |     | 45          |     | 55          |     | ns    |
| 3   | $t_{AVQV}^g$       | $t_{AA}$  | Address Access Time               |             | 25  |             | 35  |             | 45  |             | 55  | ns    |
| 4   | $t_{GLQV}$         | $t_{OE}$  | Output Enable to Data Valid       |             | 10  |             | 15  |             | 20  |             | 25  | ns    |
| 5   | $t_{AXQX}^g$       | $t_{OH}$  | Output Hold after Address Change  | 5           |     | 5           |     | 5           |     | 5           |     | ns    |
| 6   | $t_{ELQX}$         | $t_{LZ}$  | Chip Enable to Output Active      | 5           |     | 5           |     | 5           |     | 5           |     | ns    |
| 7   | $t_{EHQZ}^h$       | $t_{HZ}$  | Chip Disable to Output Inactive   |             | 10  |             | 13  |             | 15  |             | 25  | ns    |
| 8   | $t_{GLQX}$         | $t_{OLZ}$ | Output Enable to Output Active    | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 9   | $t_{GHQZ}^h$       | $t_{OHZ}$ | Output Disable to Output Inactive |             | 10  |             | 13  |             | 15  |             | 25  | ns    |
| 10  | $t_{ELICCH}^e$     | $t_{PA}$  | Chip Enable to Power Active       | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 11  | $t_{EHICCL}^{d,e}$ | $t_{PS}$  | Chip Disable to Power Standby     |             | 25  |             | 35  |             | 45  |             | 55  | ns    |

Note f:  $\bar{W}$  must be high during SRAM READ cycles and low during SRAM WRITE cycles.

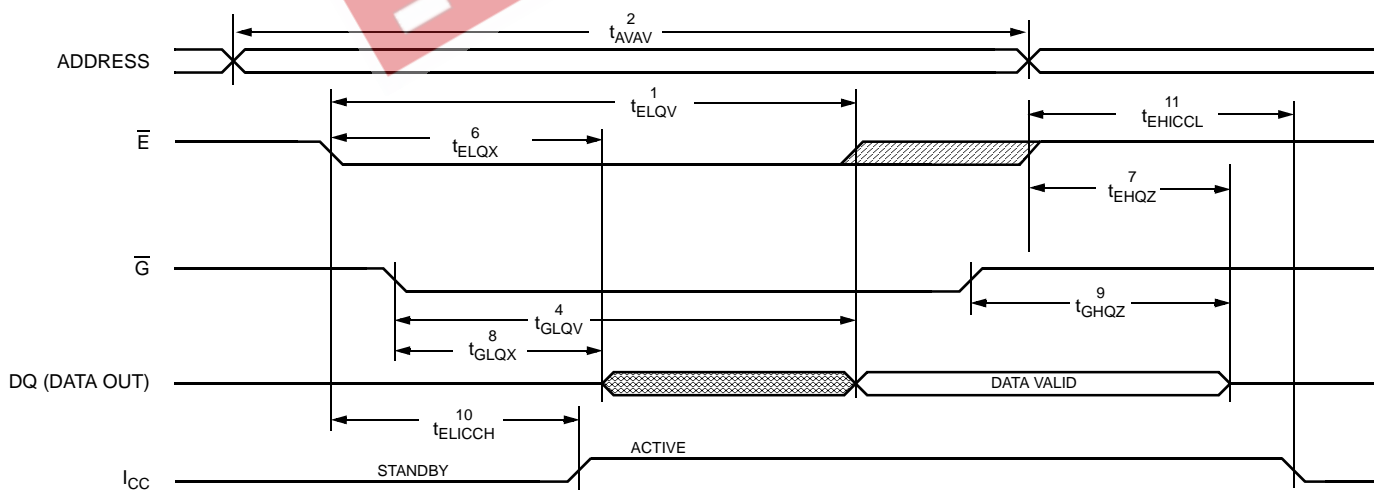
Note g: I/O state assumes  $\bar{E}, \bar{G} < V_{IL}$  and  $\bar{W} > V_{IH}$ ; device is continuously selected.

Note h: Measured  $\pm 200mV$  from steady state output voltage.

### SRAM READ CYCLE #1: Address Controlled<sup>f, g</sup>



### SRAM READ CYCLE #2: $\bar{E}$ Controlled<sup>f</sup>



# STK11C68 (SMD5962-92324)

## SRAM WRITE CYCLES #1 & #2

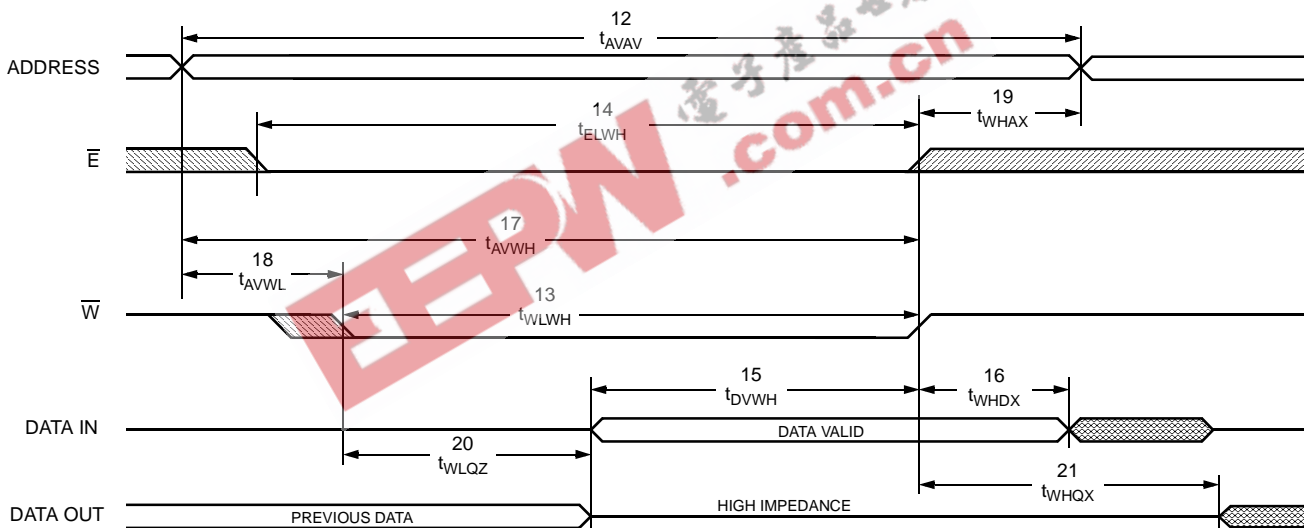
( $V_{CC} = 5.0V \pm 10\%$ )

| NO. | SYMBOLS          |            |          | PARAMETER                        | STK11C68-25 |     | STK11C68-35 |     | STK11C68-45 |     | STK11C68-55 |     | UNITS |
|-----|------------------|------------|----------|----------------------------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------|
|     | #1               | #2         | Alt.     |                                  | MIN         | MAX | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |
| 12  | $t_{AVAV}$       | $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time                 | 25          |     | 35          |     | 45          |     | 55          |     | ns    |
| 13  | $t_{WLWH}$       | $t_{WLEH}$ | $t_{WP}$ | Write Pulse Width                | 20          |     | 25          |     | 30          |     | 45          |     | ns    |
| 14  | $t_{ELWH}$       | $t_{ELEH}$ | $t_{CW}$ | Chip Enable to End of Write      | 20          |     | 25          |     | 30          |     | 45          |     | ns    |
| 15  | $t_{DVWH}$       | $t_{DVEH}$ | $t_{DW}$ | Data Set-up to End of Write      | 10          |     | 12          |     | 15          |     | 30          |     | ns    |
| 16  | $t_{WHDX}$       | $t_{EHDX}$ | $t_{DH}$ | Data Hold after End of Write     | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 17  | $t_{AVWH}$       | $t_{AVEH}$ | $t_{AW}$ | Address Set-up to End of Write   | 20          |     | 25          |     | 30          |     | 45          |     | ns    |
| 18  | $t_{AVWL}$       | $t_{AVEL}$ | $t_{AS}$ | Address Set-up to Start of Write | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 19  | $t_{WHAX}$       | $t_{EHAX}$ | $t_{WR}$ | Address Hold after End of Write  | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 20  | $t_{WLQZ}^{h,i}$ |            | $t_{WZ}$ | Write Enable to Output Disable   |             | 10  |             | 13  |             | 15  |             | 35  | ns    |
| 21  | $t_{WHQX}$       |            | $t_{OW}$ | Output Active after End of Write | 5           |     | 5           |     | 5           |     | 5           |     | ns    |

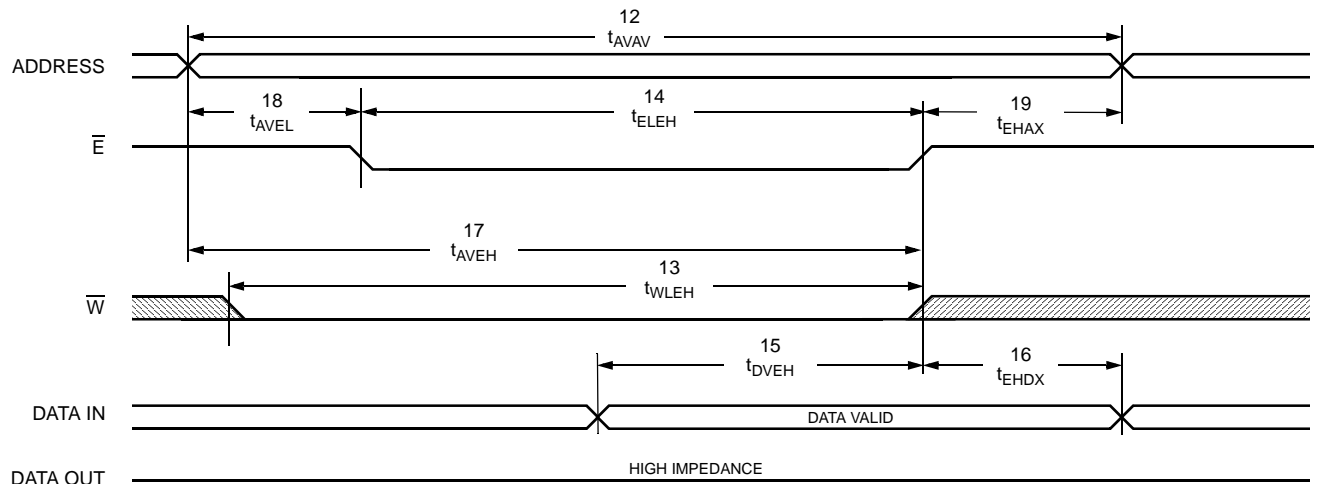
Note i: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.

Note j:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

### SRAM WRITE CYCLE #1: $\bar{W}$ Controlled<sup>j</sup>



### SRAM WRITE CYCLE #2: $\bar{E}$ Controlled<sup>j</sup>



# STK11C68 (SMD5962-92324)

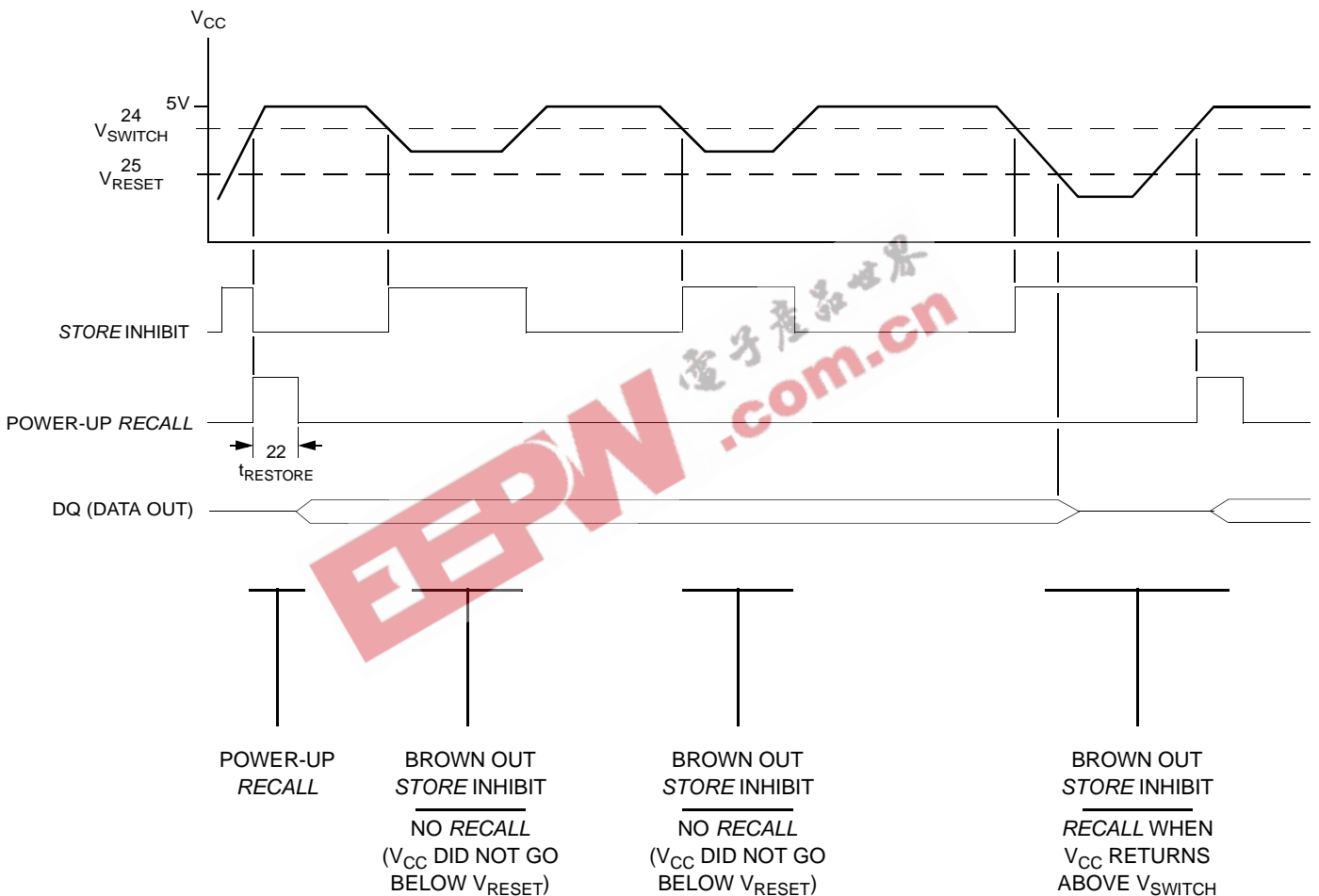
## STORE INHIBIT/POWER-UP RECALL

( $V_{CC} = 5.0V \pm 10\%$ )

| NO. | SYMBOLS       | PARAMETER                       | STK11C68 |     | UNITS   | NOTES |
|-----|---------------|---------------------------------|----------|-----|---------|-------|
|     | Standard      |                                 | MIN      | MAX |         |       |
| 22  | $t_{RESTORE}$ | Power-up <i>RECALL</i> Duration |          | 550 | $\mu s$ | k     |
| 23  | $t_{STORE}$   | <i>STORE</i> Cycle Duration     |          | 10  | ms      |       |
| 24  | $V_{SWITCH}$  | Low Voltage Trigger Level       | 4.0      | 4.5 | V       |       |
| 25  | $V_{RESET}$   | Low Voltage Reset Level         |          | 3.6 | V       |       |

Note k:  $t_{RESTORE}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .

## STORE INHIBIT/POWER-UP RECALL



## SOFTWARE STORE/RECALL MODE SELECTION

| $\bar{E}$ | $\bar{W}$ | A <sub>12</sub> - A <sub>0</sub> (hex)       | MODE   | I/O  | NOTES |
|-----------|-----------|--|--|--|-------|
| L         | H         | 0000<br>1555<br>0AAA<br>1FFF<br>10F0<br>0F0F | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile <i>STORE</i>  | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | I     |
| L         | H         | 0000<br>1555<br>0AAA<br>1FFF<br>10F0<br>0F0E | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile <i>RECALL</i> | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | I     |

Note l: The six consecutive addresses must be in the order listed.  $\bar{W}$  must be high during all six consecutive cycles to enable a nonvolatile cycle.

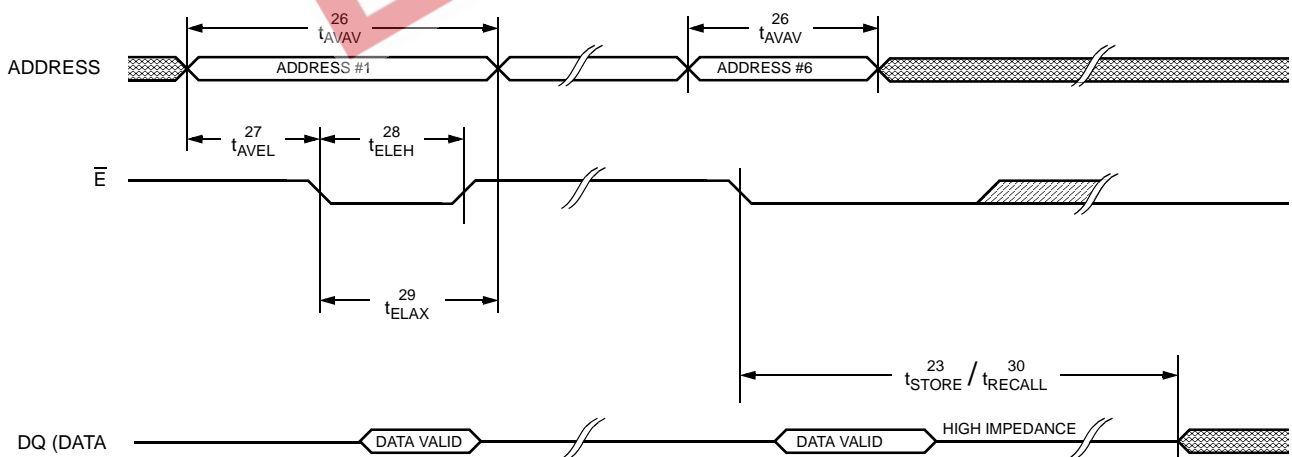
## SOFTWARE STORE/RECALL CYCLE<sup>m, n</sup> (V<sub>CC</sub> = 5.0V ± 10%)

| NO. | SYMBOLS                          | PARAMETER                          | STK11C68-25 |     | STK11C68-35 |     | STK11C68-45 |     | STK11C68-55 |     | UNITS |
|-----|----------------------------------|------------------------------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------|
|     |                                  |                                    | MIN         | MAX | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |
| 26  | t <sub>AVAV</sub>                | STORE/RECALL Initiation Cycle Time | 25          |     | 35          |     | 45          |     | 55          |     | ns    |
| 27  | t <sub>AVEL</sub> <sup>m</sup>   | Address Set-up Time                | 0           |     | 0           |     | 0           |     | 0           |     | ns    |
| 28  | t <sub>ELEH</sub> <sup>m</sup>   | Clock Pulse Width                  | 20          |     | 25          |     | 30          |     | 35          |     | ns    |
| 29  | t <sub>ELAX</sub> <sup>m</sup>   | Address Hold Time                  | 20          |     | 20          |     | 20          |     | 20          |     | ns    |
| 30  | t <sub>RECALL</sub> <sup>m</sup> | RECALL Duration                    |             | 20  |             | 20  |             | 20  |             | 20  | μs    |

Note m: The software sequence is clocked with  $\bar{E}$  controlled reads.

Note n: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles.

## SOFTWARE STORE/RECALL CYCLE: $\bar{E}$ Controlled<sup>n</sup>



## DEVICE OPERATION

The STK11C68 is a versatile memory chip that provides several modes of operation. The STK11C68 can operate as a standard 8K x 8 SRAM. It has an 8K x 8 Nonvolatile Elements shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

### NOISE CONSIDERATIONS

Note that the STK11C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

### SRAM READ

The STK11C68 performs a READ cycle whenever  $\bar{E}$  and  $\bar{G}$  are low and  $\bar{W}$  is high. The address specified on pins  $A_{0-12}$  determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\bar{E}$  or  $\bar{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\bar{E}$  or  $\bar{G}$  is brought high.

### SRAM WRITE

A WRITE cycle is performed whenever  $\bar{E}$  and  $\bar{W}$  are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\bar{E}$  or  $\bar{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\bar{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\bar{E}$  controlled WRITE.

It is recommended that  $\bar{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If  $\bar{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\bar{W}$  goes low.

### SOFTWARE NONVOLATILE STORE

The STK11C68 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

|                 |            |                      |
|-----------------|------------|----------------------|
| 1. Read address | 0000 (hex) | Valid READ           |
| 2. Read address | 1555 (hex) | Valid READ           |
| 3. Read address | 0AAA (hex) | Valid READ           |
| 4. Read address | 1FFF (hex) | Valid READ           |
| 5. Read address | 10F0 (hex) | Valid READ           |
| 6. Read address | 0F0F (hex) | Initiate STORE cycle |

The software sequence must be clocked with  $\bar{E}$  controlled READs.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\bar{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

### SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

|                 |            |                       |
|-----------------|------------|-----------------------|
| 1. Read address | 0000 (hex) | Valid READ            |
| 2. Read address | 1555 (hex) | Valid READ            |
| 3. Read address | 0AAA (hex) | Valid READ            |
| 4. Read address | 1FFF (hex) | Valid READ            |
| 5. Read address | 10F0 (hex) | Valid READ            |
| 6. Read address | 0F0E (hex) | Initiate RECALL cycle |



Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Elements. The nonvolatile data can be recalled an unlimited number of times.

## POWER-UP RECALL

During power up, or after any low-power condition ( $V_{CC} < V_{RESET}$ ), an internal *RECALL* request will be latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK11C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between  $\bar{W}$  and system  $V_{CC}$  or between  $\bar{E}$  and system  $V_{CC}$ .

## HARDWARE PROTECT

The STK11C68 offers hardware protection against inadvertent *STORE* operation during low-voltage conditions. When  $V_{CC} < V_{SWITCH}$ , software *STORE* operations are inhibited.

## LOW AVERAGE ACTIVE POWER

The STK11C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between  $I_{CC}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 5.5V$ , 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READS to WRITES; 5) the operating temperature; 6) the  $V_{CC}$  level; and 7) I/O loading.

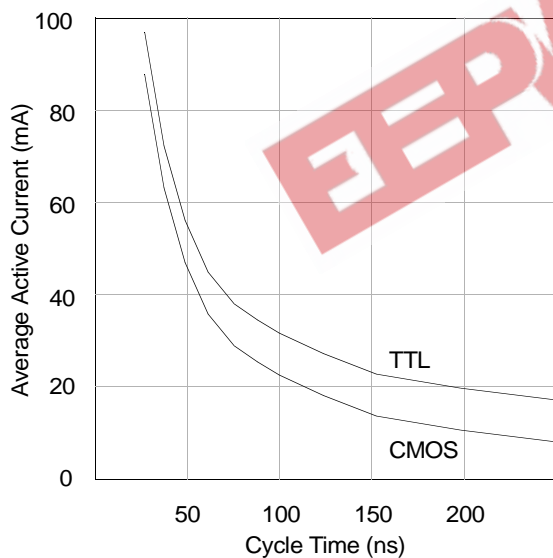


Figure 2:  $I_{CC}$  (max) Reads

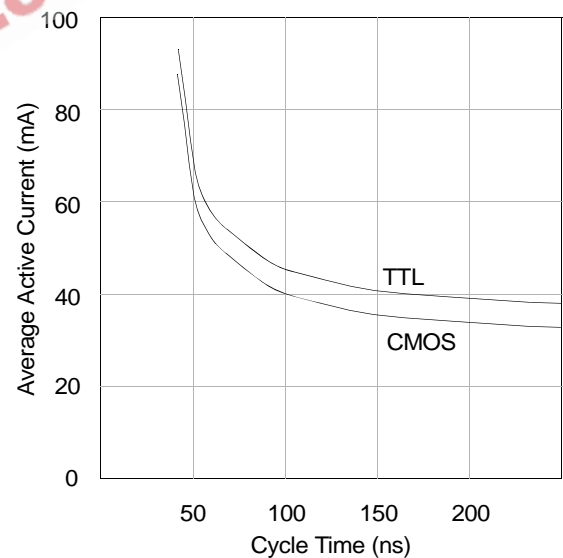
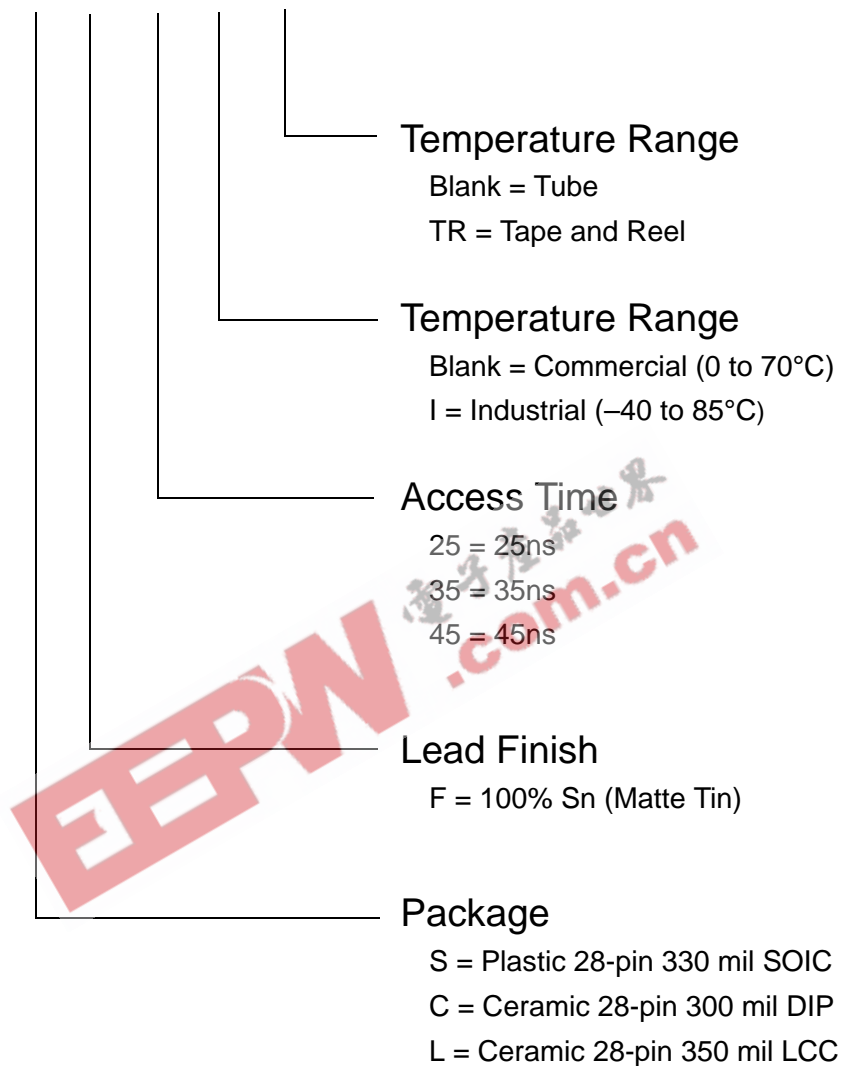


Figure 3:  $I_{CC}$  (max) Writes

# STK11C68 (SMD5962-92324)

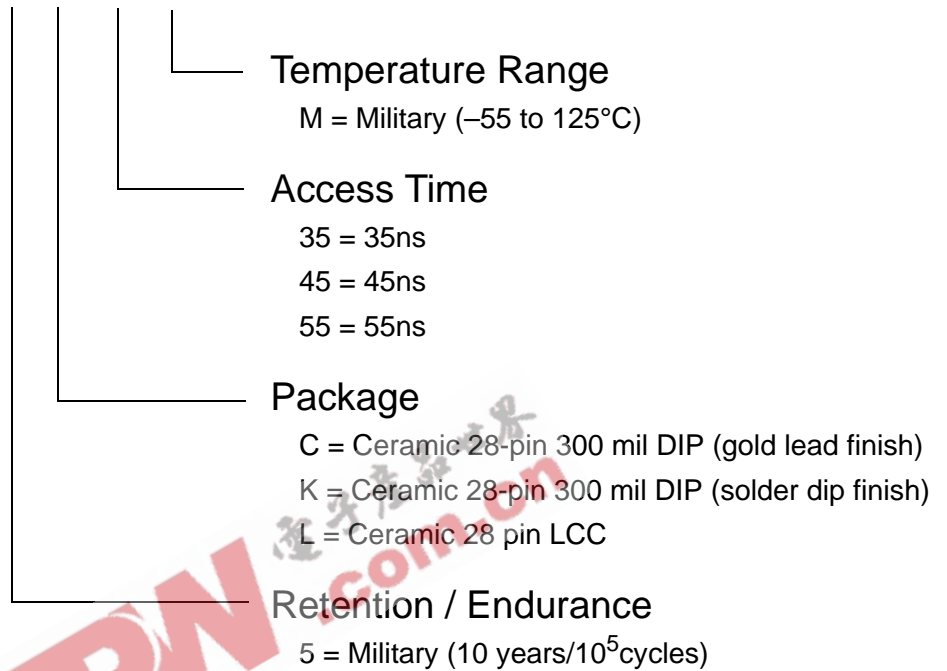
## Commercial/Industrial Ordering Information

STK11C68 - S F 45 I TR

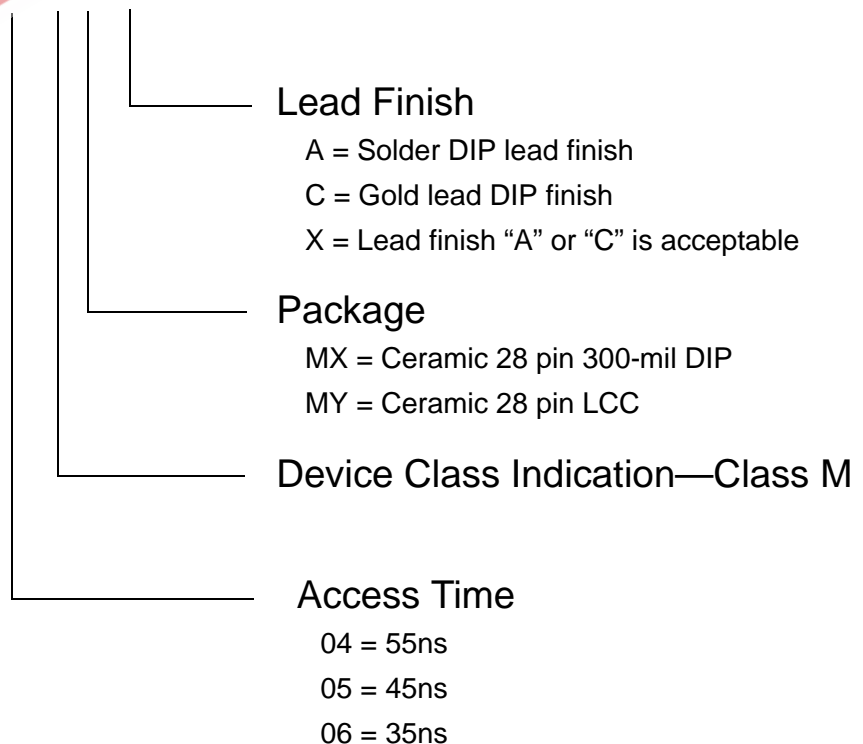


**Military Ordering Information**

**STK11C68 - 5 C 45 M**



**SMD5962-92324 04 MX X**



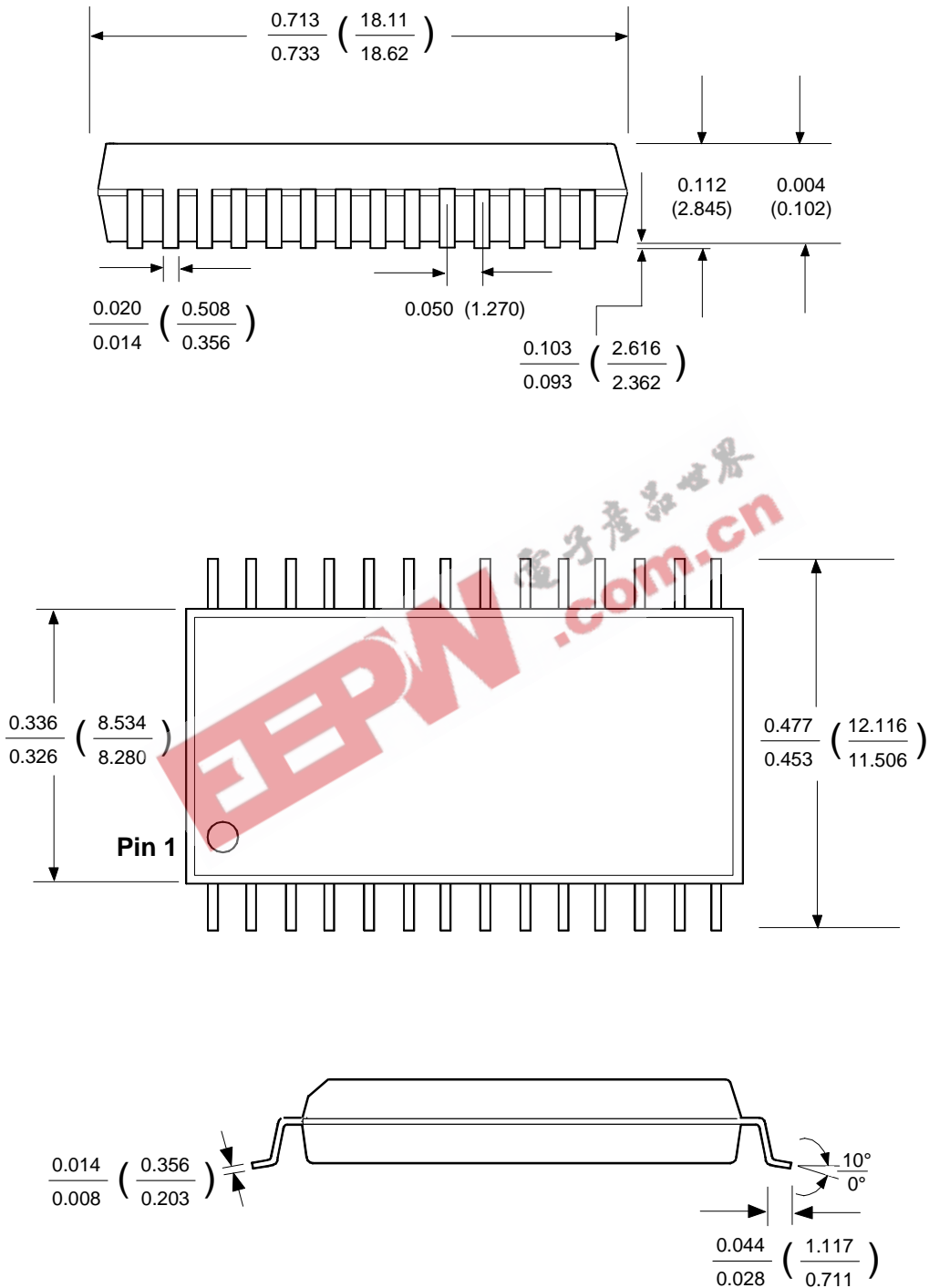
# STK11C68 (SMD5962-92324)

## Ordering Information

| Part Number         | Description                           | Temperature |
|---------------------|---------------------------------------|-------------|
| STK11C68-SF25       | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-SF35       | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-SF45       | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-SF25TR     | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-SF35TR     | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-SF45TR     | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Commercial  |
| STK11C68-L35        | 5V 64K-8b SoftStore nvSRAM CLCC28     | Commercial  |
| STK11C68-L45        | 5V 64K-8b SoftStore nvSRAM CLCC28     | Commercial  |
| STK11C68-C35        | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Commercial  |
| STK11C68-C45        | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Commercial  |
| STK11C68-SF25I      | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-SF35I      | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-SF45I      | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-SF25ITR    | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-SF35ITR    | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-SF45ITR    | 5V 64K-8b SoftStore nvSRAM SOP28-330  | Industrial  |
| STK11C68-L35I       | 5V 64K-8b SoftStore nvSRAM CLCC28     | Industrial  |
| STK11C68-L45I       | 5V 64K-8b SoftStore nvSRAM CLCC28     | Industrial  |
| STK11C68-C35I       | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Industrial  |
| STK11C68-C45I       | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Industrial  |
| STK11C68-5L35M      | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| STK11C68-5L45M      | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| STK11C68-5L55M      | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| STK11C68-5C35M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| STK11C68-5C45M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| STK11C68-5C55M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| STK11C68-5K35M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| STK11C68-5K45M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| STK11C68-5K55M      | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD5962-9232406MXA  | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232405MXA | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232404MXA | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232406MXC | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232405MXC | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232404MXC | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232406MXX | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232405MXX | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232404MXX | 5V 64K-8b SoftStore nvSRAM CDIP28-300 | Military    |
| SMD 5962-9232406MYA | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| SMD 5962-9232405MYA | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| SMD 5962-9232404MYA | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| SMD 5962-9232406MYX | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| SMD 5962-9232405MYX | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |
| SMD 5962-9232404MYX | 5V 64K-8b SoftStore nvSRAM CLCC28     | Military    |

Package Diagrams

28 Pin 330 mil SOIC

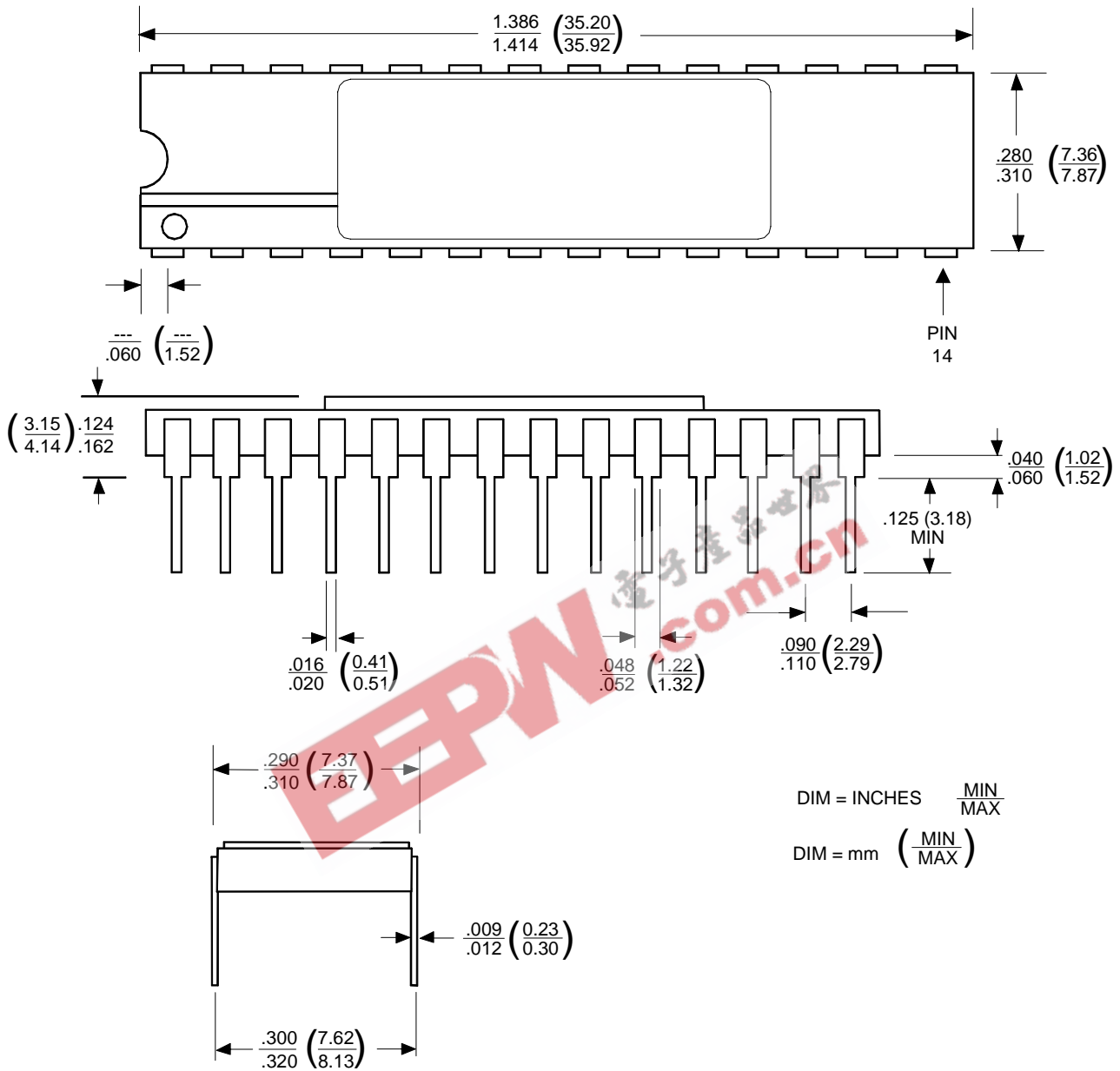


DIM = INCHES       $\frac{\text{MIN}}{\text{MAX}}$

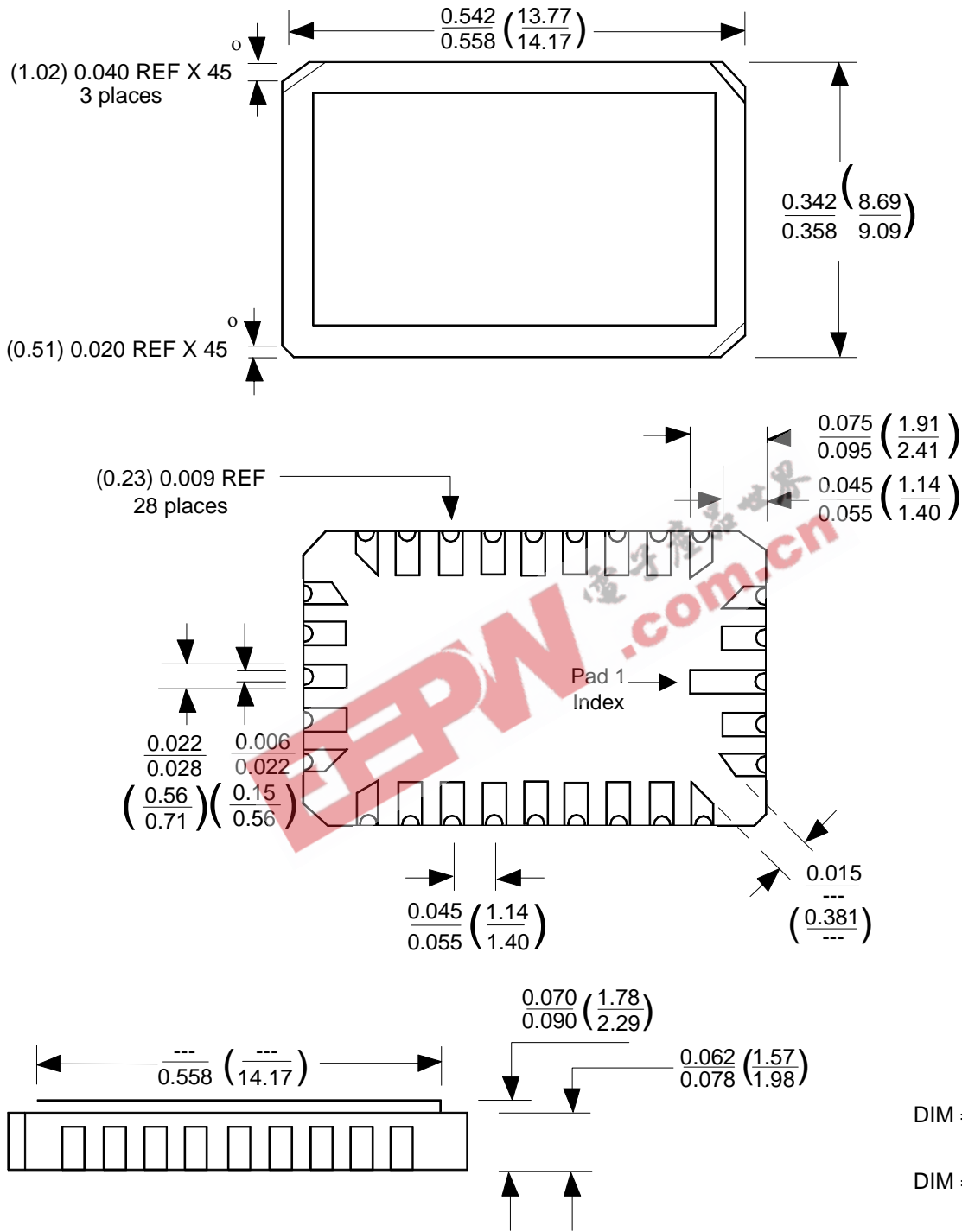
DIM = mm      (  $\frac{\text{MIN}}{\text{MAX}}$  )

# STK11C68 (SMD5962-92324)

## 28 Pin 300 mil SP DIL Sidebrazed



28 Pin 350 mil LCC



# STK11C68 (SMD5962–92324)

## Document Revision History

| Revision | Date           | Summary   |
|----------|----------------|---|
| 0.0      | December 2002  | Combined commercial, industrial and military data sheets. Removed 20 nsec device.   |
| 0.1      | September 2003 | Added lead-free lead finish   |
| 0.2      | March 2006     | Removed leaded lead finish for all Commercial/Industrial Parts, Removed "P" package.  |
| 0.3      | February 2007  | Add fast power-down slew RSK information<br>Restore Comm/Ind C & L Package Options<br>Add Tape Reel Ordering Options<br>Add Product Ordering Code Listing<br>Add Package Outline Drawings<br>Reformat Entire Document |

SIMTEK STK11C68 Datasheet, February 2007

Copyright 2007, Simtek Corporation. All rights reserved.

This datasheet may only be printed for the expressed use of Simtek Customers. No part of the datasheet may be reproduced in any other form or means without the express written permission from Simtek Corporation. The information contained in this publication is believed to be accurate, but changes may be made without notice. Simtek does not assume responsibility for, or grant or imply any warranty, including MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE regarding this information, the product or its use. Nothing herein constitutes a license, grant or transfer of any rights to any Simtek patent, copyright, trademark, or other proprietary right.

EEPW 电子產品世界  
.com.cn