

**FEATURES**

- 35, 45 ns Read Access & R/W Cycle Time
- Unlimited Read/Write Endurance
- Automatic Non-volatile STORE on Power Loss
- Non-Volatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 1 Million STORE Cycles
- 100-Year Non-volatile Data Retention
- Single 3.3V  $\pm 0.3V$  Power Supply
- Commercial and Industrial Temperatures
- 32-Pin 300 mil SOIC and 600 mil PDIP Packages (RoHS-Compliant)

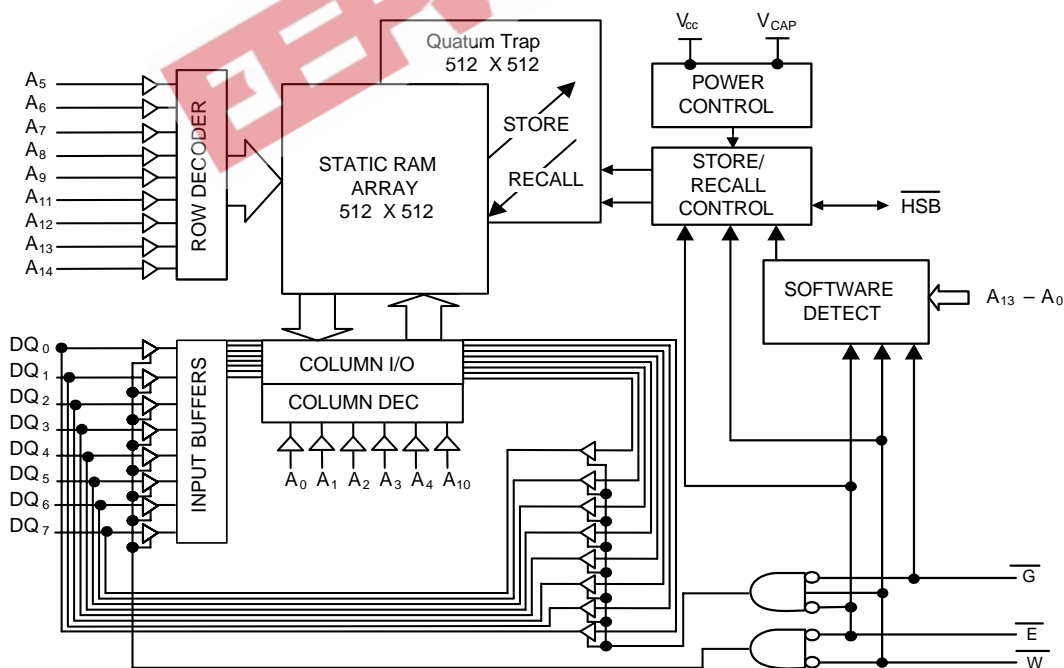
**DESCRIPTION**

The Simtek STK14C88-3 is a 256Kb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

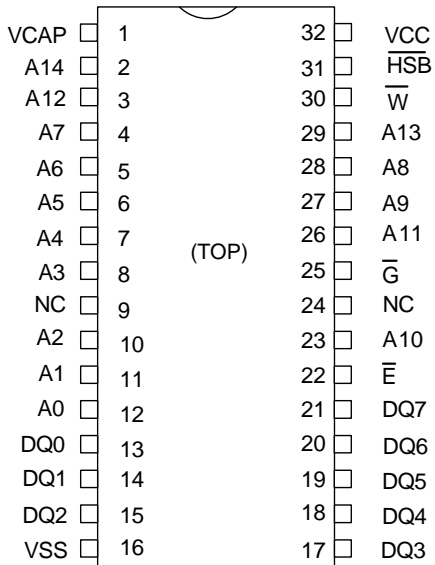
The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

Data transfers automatically to the non-volatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

**BLOCK DIAGRAM**


## STK14C88-3



32-Pin SOIC

32-Pin PDIP

### PIN DESCRIPTIONS

Pin Name	I/O	Description
A <sub>14</sub> -A <sub>0</sub>	Input	Address: The 15 address inputs select one of 32,768 bytes in the nvSRAM array
DQ <sub>7</sub> -DQ <sub>0</sub>	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{\text{E}}$	Input	Chip Enable: The active low $\overline{\text{E}}$ input selects the device
$\overline{\text{W}}$	Input	Write Enable: The active low $\overline{\text{W}}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{\text{E}}$
$\overline{\text{G}}$	Input	Output Enable: The active low $\overline{\text{G}}$ input enables the data output buffers during read cycles. De-asserting $\overline{\text{G}}$ high caused the DQ pins to tri-state.
V <sub>CC</sub>	Power Supply	Power: 3.3V, $\pm 0.3\text{V}$
$\overline{\text{HSB}}$	I/O	Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
V <sub>CAP</sub>	Power Supply	AutoStore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V <sub>SS</sub>	Power Supply	Ground

**ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Voltage on Input Relative to Ground . . . . . -0.5V to 7.0V  
 Voltage on Input Relative to V<sub>SS</sub> . . . . . -0.6V to (V<sub>CC</sub> + 0.5V)  
 Voltage on DQ<sub>0-7</sub> or HSB . . . . . -0.5V to (V<sub>CC</sub> + 0.5V)  
 Temperature under Bias . . . . . -55°C to 125°C  
 Storage Temperature . . . . . -65°C to 150°C  
 Power Dissipation . . . . . 1W  
 DC Output Current (1 output at a time, 1s duration) . . . . . 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**NF (SOP-32) PACKAGE THERMAL CHARACTERISTICS**

θ<sub>Jc</sub> 5.4 C/W; θ<sub>ja</sub> 44.3 [0fpm], 37.9 [200fpm], 35.1 C/W [500fpm].

**WF (PDIP-32) PACKAGE THERMAL CHARACTERISTICS**

θ<sub>Jc</sub> ND; θ<sub>ja</sub> 40 [0fpm], 34.5 [200fpm], 32.3 C/W [500fpm].

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 3 - 3.6V)<sup>e</sup>

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I <sub>CC1</sub> <sup>b</sup>	Average V <sub>CC</sub> Current		50 42	52 44		mA	t <sub>AVAV</sub> = 35ns t <sub>AVAV</sub> = 45ns
I <sub>CC2</sub> <sup>c</sup>	Average V <sub>CC</sub> Current during STORE		3	3		mA	All Inputs Don't Care, V <sub>CC</sub> = max
I <sub>CC3</sub> <sup>b</sup>	Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200ns 5V, 25°C, Typical		9	9		mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I <sub>CC4</sub> <sup>c</sup>	Average V <sub>CAP</sub> Current during AutoStore Cycle		2	2		mA	All Inputs Don't Care
I <sub>SB1</sub> <sup>d</sup>	Average V <sub>CC</sub> Current (Standby, Cycling TTL Input Levels)		18 16	19 17		mA	t <sub>AVAV</sub> = 35ns, $\bar{E} \geq V_{IH}$ t <sub>AVAV</sub> = 45ns, $\bar{E} \geq V_{IH}$
I <sub>SB2</sub> <sup>d</sup>	V <sub>CC</sub> Standby Current (Standby, Stable CMOS Input Levels)		1	1		mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All Others V <sub>IN</sub> ≤ 0.2V or ≥ (V <sub>CC</sub> - 0.2V)
I <sub>ILK</sub>	Input Leakage Current		±1	±1		µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>OLK</sub>	Off-State Output Leakage Current		±1	±1		µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\bar{E}$ or $\bar{G} \geq V_{IH}$
V <sub>IH</sub>	Input Logic "1" Voltage	2.2	V <sub>CC</sub> + .5	2.2	V <sub>CC</sub> + .5	V	All Inputs
V <sub>IL</sub>	Input Logic "0" Voltage	V <sub>SS</sub> - .5	0.8	V <sub>SS</sub> - .5	0.8	V	All Inputs
V <sub>OH</sub>	Output Logic "1" Voltage	2.4		2.4		V	I <sub>OUT</sub> = -4mA except HSB
V <sub>OL</sub>	Output Logic "0" Voltage		0.4		0.4	V	I <sub>OUT</sub> = 8mA except HSB
V <sub>BL</sub>	Logic "0" Voltage on HSB Output		0.4		0.4	V	I <sub>OUT</sub> = 3mA
T <sub>A</sub>	Operating Temperature	0	70	-40	85	°C	
V <sub>CC</sub>	Operating Voltage	3.0	3.6	3.0	3.6	V	3.3V ± 0.3V
V <sub>CAP</sub>	Storage Capacitor	54	264	54	264	µF	68 to 220µF ± 20%, 4.7v Rated
NV <sub>C</sub>	Nonvolatile STORE operations	1,000		1,000		K	
DATA <sub>R</sub>	Data Retention	100		100		Years	@55 °C

Note b: I<sub>CC1</sub> and I<sub>CC3</sub> are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I<sub>CC2</sub> and I<sub>CC4</sub> are the average currents required for the duration of the respective STORE cycles (t<sub>STORE</sub>).

Note d:  $\bar{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.

Note e: V<sub>CC</sub> reference levels throughout this datasheet refer to V<sub>CC</sub> if that is where the power supply connection is made, or V<sub>CAP</sub> if V<sub>CC</sub> is connected to ground.

# STK14C88-3

## AC TEST CONDITIONS

Input Pulse Levels .....	0V to 3V
Input Rise and Fall Times .....	≤ 5ns
Input and Output Timing Reference Levels .....	1.5V
Output Load .....	See Figure 1

## CAPACITANCE<sup>†</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C <sub>IN</sub>	Input Capacitance	5	pF	ΔV = 0 to 3V
C <sub>OUT</sub>	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

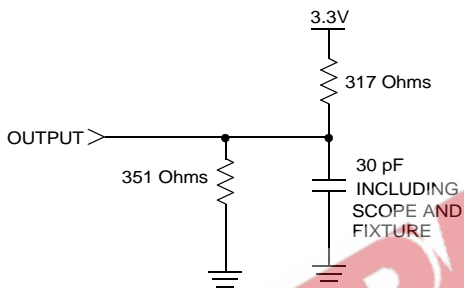


Figure 1. AC Output Loading

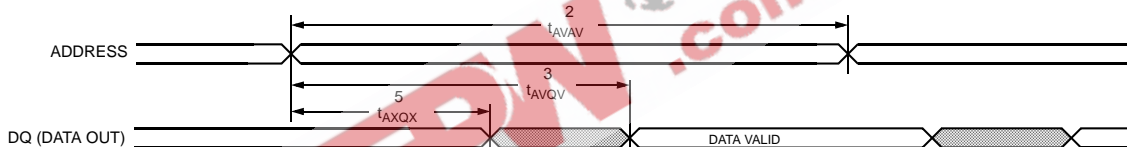
SRAM READ CYCLES #1 & #2

(V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>

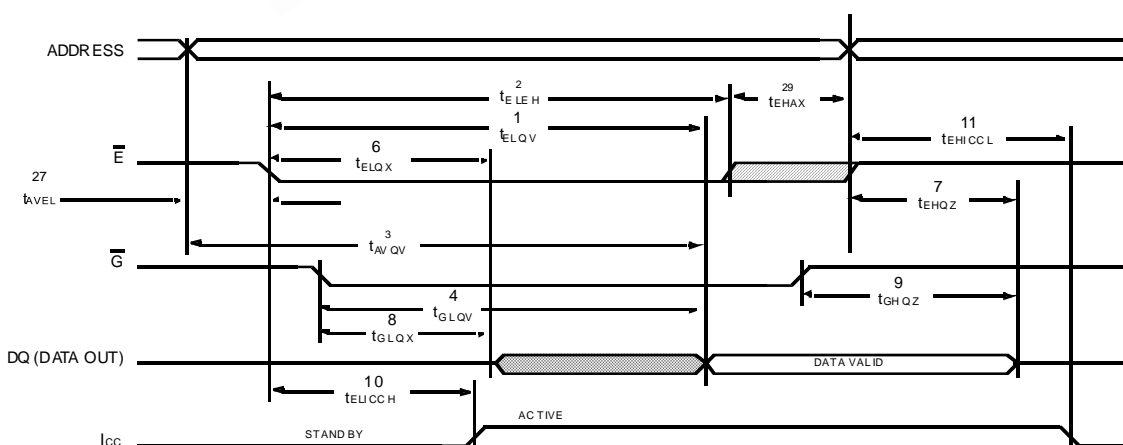
NO.	SYMBOLS		PARAMETER	STK14C88-3-35		STK14C88-3-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	
1	t <sub>ELQV</sub>	t <sub>ACS</sub>	Chip Enable Access Time		35		45	ns
2	t <sub>AVAV</sub> <sup>g</sup> , t <sub>ELEH</sub> <sup>g</sup>	t <sub>RC</sub>	Read Cycle Time	35		45		ns
3	t <sub>AVQV</sub> <sup>h</sup>	t <sub>AA</sub>	Address Access Time		35		45	ns
4	t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Data Valid		15		20	ns
5	t <sub>AXQX</sub> <sup>h</sup>	t <sub>OH</sub>	Output Hold after Address Change	5		5		ns
6	t <sub>ELQX</sub>	t <sub>LZ</sub>	Address Change or Chip Enable to Output Active	5		5		ns
7	t <sub>EHQZ</sub> <sup>i</sup>	t <sub>HZ</sub>	Address Change or Chip Disable to Output Inactive		13		15	ns
8	t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output Active	0		0		ns
9	t <sub>GHQZ</sub> <sup>i</sup>	t <sub>OHZ</sub>	Output Disable to Output Inactive		13		15	ns
10	t <sub>ELICCH</sub> <sup>f</sup>	t <sub>PA</sub>	Chip Enable to Power Active	0		0		ns
11	t <sub>EHICCL</sub> <sup>f</sup>	t <sub>PS</sub>	Chip Disable to Power Standby		35		45	ns

Note g:  $\overline{W}$  and  $\overline{HSB}$  must be high during SRAM READ cycles.  
 Note h: /O state assumes  $\overline{E}$  and  $\overline{G} \leq V_{IL}$  and  $\overline{W} \geq V_{IH}$ ; device is continuously selected.  
 Note i: Measured  $\pm 200mV$  from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled<sup>g, h</sup>



SRAM READ CYCLE #2:  $\overline{E}$  and  $\overline{G}$  Controlled<sup>g</sup>



# STK14C88-3

## SRAM WRITE CYCLES #1 & #2

(V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>

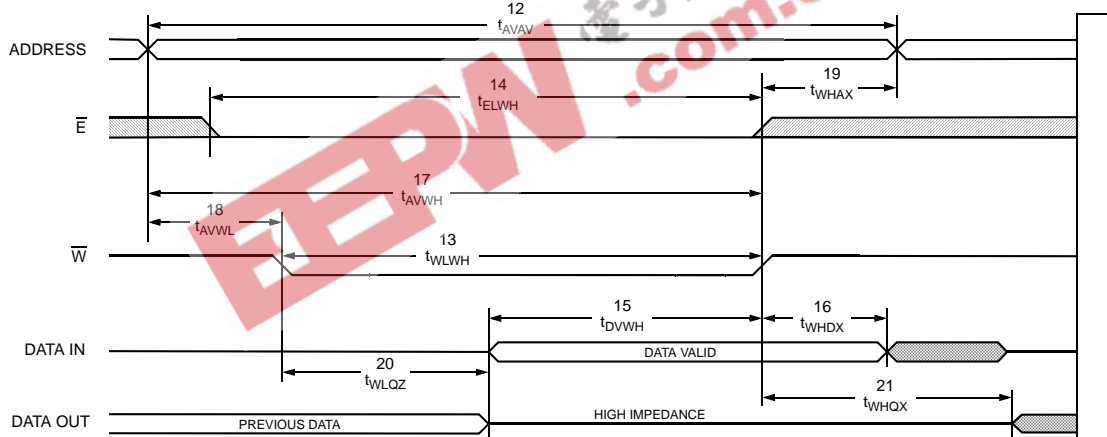
NO.	SYMBOLS			PARAMETER	STK14C88-3-35		STK14C88-3-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	
12	t <sub>AVAV</sub>	t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time	35		45		ns
13	t <sub>WLWH</sub>	t <sub>WLEH</sub>	t <sub>WP</sub>	Write Pulse Width	25		30		ns
14	t <sub>ELWH</sub>	t <sub>ELEH</sub>	t <sub>CW</sub>	Chip Enable to End of Write	25		30		ns
15	t <sub>DVWH</sub>	t <sub>DVEH</sub>	t <sub>DW</sub>	Data Set-up to End of Write	12		15		ns
16	t <sub>WHDX</sub>	t <sub>EHDX</sub>	t <sub>DH</sub>	Data Hold after End of Write	0		0		ns
17	t <sub>AVWH</sub>	t <sub>AVEH</sub>	t <sub>AW</sub>	Address Set-up to End of Write	25		30		ns
18	t <sub>AVWL</sub>	t <sub>AVEL</sub>	t <sub>AS</sub>	Address Set-up to Start of Write	0		0		ns
19	t <sub>WHAX</sub>	t <sub>EHAX</sub>	t <sub>WR</sub>	Address Hold after End of Write	0		0		ns
20	t <sub>WLOZ</sub> <sup>i,j</sup>		t <sub>WZ</sub>	Write Enable to Output Disable		13		15	ns
21	t <sub>WHQX</sub>		t <sub>OW</sub>	Output Active after End of Write	5		5		ns

Note j:  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.

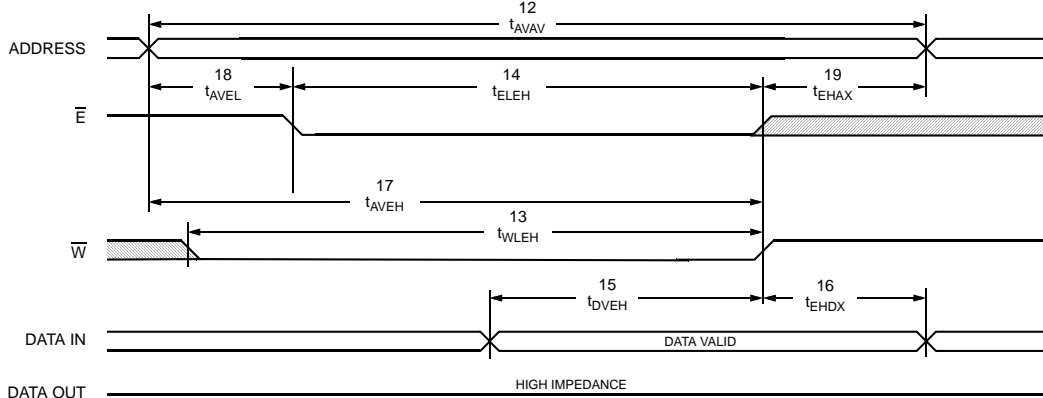
Note k:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

Note l:  $\bar{HSB}$  must be high during SRAM WRITE cycles.

### SRAM WRITE CYCLE #1: $\bar{W}$ Controlled<sup>k, l</sup>



### SRAM WRITE CYCLE #2: $\bar{E}$ Controlled<sup>k, l</sup>



**HARDWARE MODE SELECTION**

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A <sub>13</sub> - A <sub>0</sub> (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	t
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile STORE	Output High Z	I <sub>CC2</sub>	m

Note m:  $\overline{HSB}$  STORE operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the STORE (if any) completes, the part will go into standby mode, inhibiting all operations until  $\overline{HSB}$  rises.

**HARDWARE STORE CYCLE**

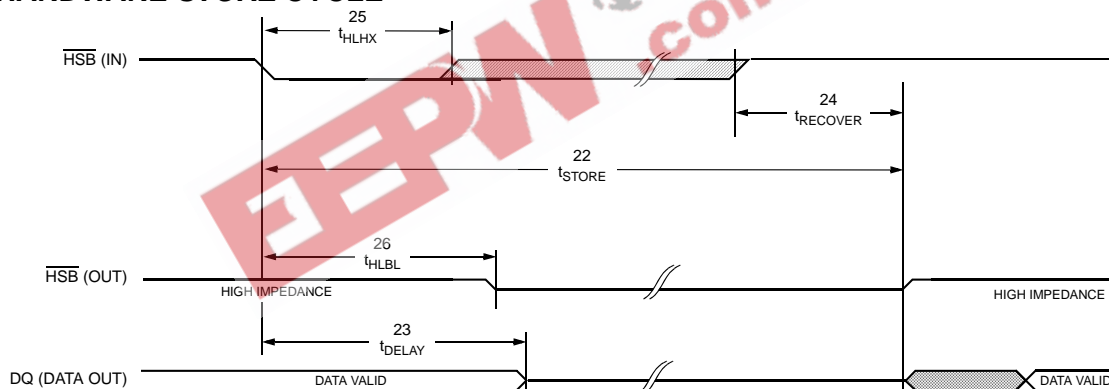
(V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>

NO.	SYMBOLS		PARAMETER	STK14C88-3		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t <sub>STORE</sub>	t <sub>HLHZ</sub>	STORE Cycle Duration		10	ms	n
23	t <sub>DELAY</sub>	t <sub>HLQZ</sub>	Time Allowed to Complete SRAM Cycle	1		μs	n
24	t <sub>RECOVER</sub>	t <sub>HHQX</sub>	Hardware STORE High to Inhibit Off		700	ns	n, o
25	t <sub>HLHX</sub>		Hardware STORE Pulse Width	15		ns	
26	t <sub>HLBL</sub>		Hardware STORE Low to STORE Busy		300	ns	

Note n:  $\overline{E}$  and  $\overline{G}$  low and  $\overline{W}$  high for output behavior.

Note o: t<sub>RECOVER</sub> is only applicable after t<sub>STORE</sub> is complete.

**HARDWARE STORE CYCLE**



# STK14C88-3

## AutoStore/POWER-UP RECALL

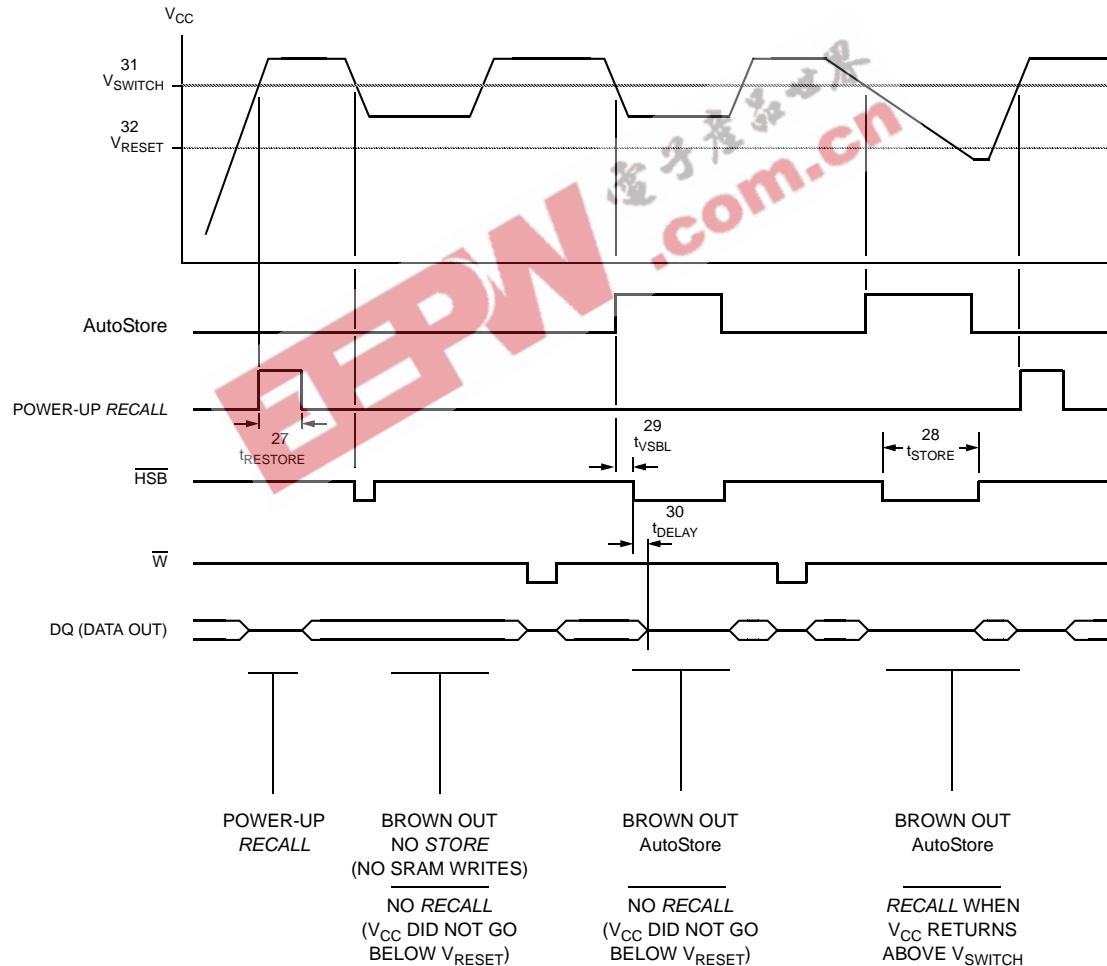
(V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>

NO.	SYMBOLS		PARAMETER	STK14C88-3		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	t <sub>RESTORE</sub>		Power-up RECALL Duration		550	μs	p
28	t <sub>STORE</sub>	t <sub>HLHZ</sub>	STORE Cycle Duration		10	ms	n, q
29	t <sub>VSBL</sub>		Low Voltage Trigger (V <sub>SWITCH</sub> ) to HSB Low		300	ns	l
30	t <sub>DELAY</sub>	t <sub>BLOZ</sub>	Time Allowed to Complete SRAM Cycle	1		μs	n
31	V <sub>SWITCH</sub>		Low Voltage Trigger Level	2.7	2.95	V	
32	V <sub>RESET</sub>		Low Voltage Reset Level		2.4	V	

Note p: t<sub>RESTORE</sub> starts from the time V<sub>CC</sub> rises above V<sub>SWITCH</sub>.

Note q: HSB is asserted low for 1μs when V<sub>CAP</sub> drops through V<sub>SWITCH</sub>. If an SRAM WRITE has not taken place since the last nonvolatile cycle, HSB will be released and no STORE will take place.

## AutoStore/POWER-UP RECALL





**SOFTWARE STORE/RECALL MODE SELECTION**

$\bar{E}$	$\bar{W}$	A <sub>13</sub> - A <sub>0</sub> (hex)	MODE	I/O	POWER	NOTES
L	H	0E38	Read SRAM	Output Data	Active	n, r, s, t
		31C7	Read SRAM	Output Data		
		03E0	Read SRAM	Output Data		
		3C1F	Read SRAM	Output Data		
		303F	Read SRAM	Output Data		
		0FC0	Nonvolatile STORE	Output High Z		
L	H	0E38	Read SRAM	Output Data	Active	n, r, s, t
		31C7	Read SRAM	Output Data		
		03E0	Read SRAM	Output Data		
		3C1F	Read SRAM	Output Data		
		303F	Read SRAM	Output Data		
		0C63	Nonvolatile RECALL	Output High Z		

**SOFTWARE-CONTROLLED STORE/RECALL CYCLE<sup>V</sup> (V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>**

NO.	SYMBOLS		PARAMETER	STK14C88-3-35		STK14C88-3-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
33	t <sub>AVAV</sub>	t <sub>RC</sub>	STORE/RECALL Initiation Cycle Time	35		45		ns	n
34	t <sub>AVEL</sub>	t <sub>AS</sub>	Address Set-up Time	0		0		ns	u, v
35	t <sub>ELEH</sub>	t <sub>CW</sub>	Clock Pulse Width	25		30		ns	u, v
36	t <sub>ELAX</sub>		Address Hold Time	20		20		ns	u, v
37	t <sub>RECALL</sub>		RECALL Duration	20		20		μs	

Note r: The six consecutive addresses must be in the order listed.  $\bar{W}$  must be high during all six consecutive  $\bar{E}$  controlled cycles to enable a nonvolatile cycle.

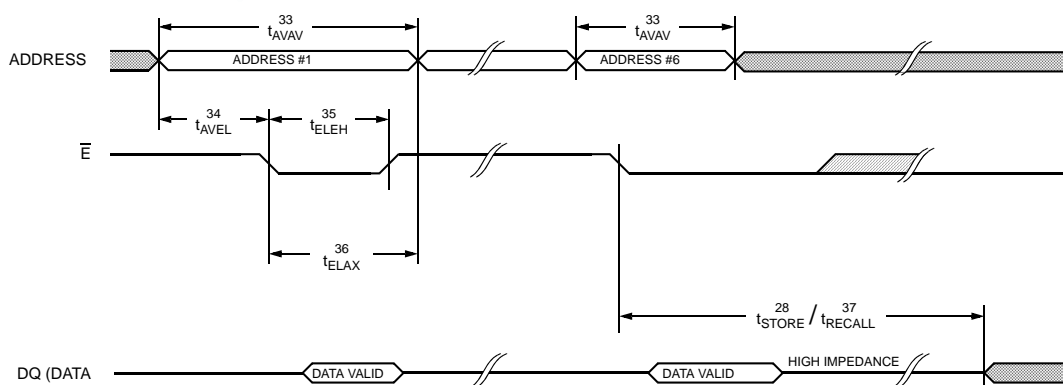
Note s: While there are 15 addresses on the STK14C88-3, only the lower 14 are used to control software modes.

Note t: I/O state assumes  $\bar{G} \leq V_{IL}$ . Activation of nonvolatile cycles does not depend on state of  $\bar{G}$ .

Note u: The software sequence is clocked on the falling edge of  $\bar{E}$  controlled READs without involving  $\bar{G}$  (double clocking will abort the sequence). See application note: MA0002 <http://www.simtek.com/attachments/AppNote02.pdf>.

Note v: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles.

**SOFTWARE STORE/RECALL CYCLE:  $\bar{E}$  CONTROLLED<sup>V</sup>**



**nvSRAM OPERATION**

The STK14C88-3 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to nonvolatile elements (the *STORE* operation) or from nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

**NOISE CONSIDERATIONS**

The STK14C88-3 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CAP}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

**SRAM READ**

The STK14C88-3 performs a READ cycle whenever  $\bar{E}$  and  $\bar{G}$  are low and  $\bar{W}$  and HSB are high. The address specified on pins  $A_{0-14}$  determines which of the 32,768 data byte will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\bar{E}$  or  $\bar{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\bar{E}$  or  $\bar{G}$  is brought high, or  $\bar{W}$  or HSB is brought low.

**SRAM WRITE**

A WRITE cycle is performed whenever  $\bar{E}$  and  $\bar{W}$  are low and HSB is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\bar{E}$  or  $\bar{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\bar{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\bar{E}$  controlled WRITE.

It is recommended that  $\bar{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If  $\bar{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLOZ}$  after  $\bar{W}$  goes low.

**POWER-UP RECALL**

During power up, or after any low-power condition ( $V_{CAP} < V_{RESET}$ ), an internal *RECALL* request will be latched. When  $V_{CAP}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK14C88-3 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between  $\bar{W}$  and system  $V_{CC}$  or between  $\bar{E}$  and system  $V_{CC}$ .

**SOFTWARE NONVOLATILE STORE**

The STK14C88-3 software *STORE* cycle is initiated by executing sequential  $\bar{E}$  controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

- |                 |            |                             |
|-----------------|------------|-----------------------------|
| 1. Read address | 0E38 (hex) | Valid READ                  |
| 2. Read address | 31C7 (hex) | Valid READ                  |
| 3. Read address | 03E0 (hex) | Valid READ                  |
| 4. Read address | 3C1F (hex) | Valid READ                  |
| 5. Read address | 303F (hex) | Valid READ                  |
| 6. Read address | 0FC0 (hex) | Initiate <i>STORE</i> cycle |

The software sequence must be clocked with  $\bar{E}$  controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\bar{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

### SOFTWARE NONVOLATILE RECALL

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of  $\bar{E}$  controlled READ operations must be performed:

1. Read address 0E38 (hex) Valid READ
2. Read address 31C7 (hex) Valid READ
3. Read address 03E0 (hex) Valid READ
4. Read address 3C1F (hex) Valid READ
5. Read address 303F (hex) Valid READ
6. Read address 0C63 (hex) Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

### AutoStore MODE

The STK14C88-3 can be powered in one of three modes.

During normal AutoStore operation, the STK14C88-3 will draw current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the  $V_{CAP}$  pin drops below  $V_{SWITCH}$ , the part will automatically disconnect the  $V_{CAP}$  pin from  $V_{CC}$  and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between  $68\mu F$  and  $220\mu F (\pm 20\%)$  rated at 4.7V should be provided.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving  $\bar{H}SB$  low will be ignored unless at least one *WRITE* operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a *WRITE* operation has taken place.

If the power supply drops faster than  $20 \mu s/volt$  before  $V_{CC}$  reaches  $V_{SWITCH}$ , then a 1 ohm resistor should be inserted between  $V_{CC}$  and the system supply to avoid momentary excess of current between  $V_{CC}$  and  $V_{cap}$ .

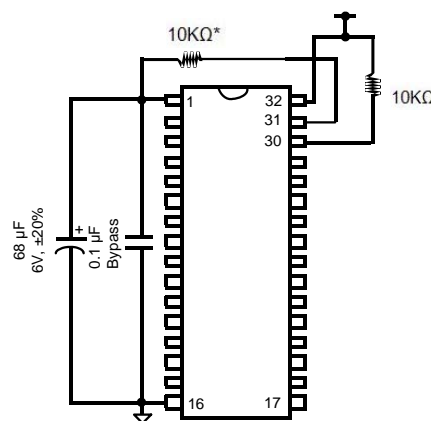


Figure 2: AutoStore Mode  
\*If  $\bar{H}SB$  is not used, it should be left unconnected.

### AutoStore INHIBIT MODE

If an automatic *STORE* on power loss is not required, then  $V_{CC}$  can be tied to ground and system power applied to  $V_{CAP}$  (Figure 3). This is the *AutoStore* Inhibit mode, in which the *AutoStore* function is disabled. If the STK14C88-3 is operated in this configuration, references to  $V_{CC}$  should be changed to  $V_{CAP}$  throughout this data sheet. In this mode, *STORE* operations may be triggered through software control. It is not permissible to change between these three options “on the fly.”

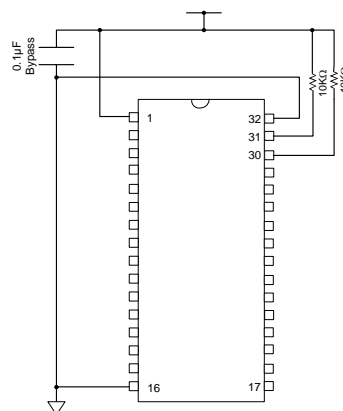


Figure 3: AutoStore Inhibit Mode  
\*If  $\bar{H}SB$  is not used, it should be left unconnected.

## STK14C88-3

### HSB OPERATION

The STK14C88-3 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the *STORE* operations. The  $\overline{\text{HSB}}$  pin can be used to request a hardware *STORE* cycle. When the  $\overline{\text{HSB}}$  pin is driven low, the STK14C88-3 will conditionally initiate a *STORE* operation after  $t_{\text{DELAY}}$ ; an actual *STORE* cycle will only begin if a *WRITE* to the SRAM took place since the last *STORE* or *RECALL* cycle. The  $\overline{\text{HSB}}$  pin has a very resistive pullup and is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to  $V_{\text{CAP}}$  if  $\overline{\text{HSB}}$  is used as a driver.

SRAM READ and *WRITE* operations that are in progress when  $\overline{\text{HSB}}$  is driven low by any means are given time to complete before the *STORE* operation is initiated. After  $\overline{\text{HSB}}$  goes low, the STK14C88-3 will continue SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations may take place. If a *WRITE* is in progress when  $\overline{\text{HSB}}$  is pulled low it will be allowed a time,  $t_{\text{DELAY}}$ , to complete. However, any SRAM *WRITE* cycles requested after  $\overline{\text{HSB}}$  goes low will be inhibited until  $\overline{\text{HSB}}$  returns high.

The  $\overline{\text{HSB}}$  pin can be used to synchronize multiple STK14C88-3s while using a single larger capacitor. To operate in this mode the  $\overline{\text{HSB}}$  pins should be connected together to the  $\overline{\text{HSB}}$  pins from the other STK14C88-3s. An external pull-up resistor to +3.3V is required since  $\overline{\text{HSB}}$  acts as an open drain pull-down. The  $V_{\text{CAP}}$  pins from the other STK14C88-3 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14C88-3s detects a power loss and asserts  $\overline{\text{HSB}}$ , the common  $\overline{\text{HSB}}$  pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK14C88-3s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK14C88-3 will continue to drive the  $\overline{\text{HSB}}$  pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK14C88-3 will remain disabled until the  $\overline{\text{HSB}}$  pin returns high.

If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

### BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (autostore enabled, etc.). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).
- The  $V_{\text{cap}}$  value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max  $V_{\text{cap}}$  value because the nvSRAM internal algorithm calculates  $V_{\text{cap}}$  charge time based on this max  $V_{\text{cap}}$  value. Customers that want to use a larger  $V_{\text{cap}}$  value to make sure there is extra store charge and store time should discuss their  $V_{\text{cap}}$  size selection with Simtek to understand any impact on the  $V_{\text{cap}}$  voltage level at the end of a  $t_{\text{RECALL}}$  period.

**PREVENTING STORES**

The *STORE* function can be disabled on the fly by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30mA at a  $V_{\text{OH}}$  of at least 2.2V, as it will have to overpower the internal pull-down device that drives  $\overline{\text{HSB}}$  low for 20 $\mu\text{s}$  at the onset of a *STORE*. When the STK14C88-3 is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CC}}$  and a 68 $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK14C88-3 will attempt to pull  $\overline{\text{HSB}}$  low; if  $\overline{\text{HSB}}$  doesn't actually get below  $V_{\text{IL}}$ , the part will stop trying to pull  $\overline{\text{HSB}}$  low and abort the *STORE* attempt.

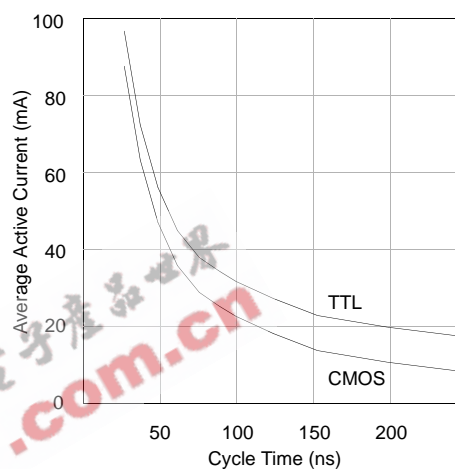
**HARDWARE PROTECT**

The STK14C88-3 offers hardware protection against inadvertent *STORE* operation and SRAM WRITES during low-voltage conditions. When  $V_{\text{CAP}} < V_{\text{SWITCH}}$ , all externally initiated *STORE* operations and SRAM WRITES will be inhibited.

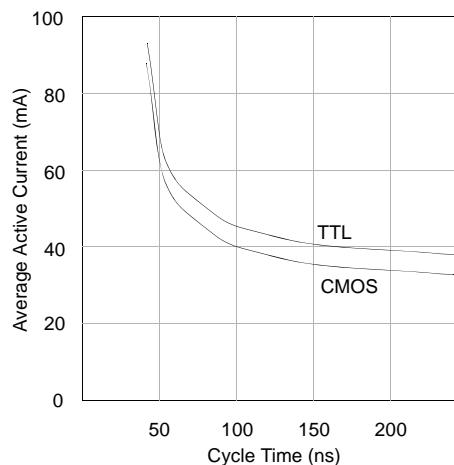
**LOW AVERAGE ACTIVE POWER**

The STK14C88-3 draws significantly less current when it is cycled at times longer than 50ns. Figure 4 shows the relationship between  $I_{\text{CC}}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{\text{CC}} = 3.6\text{V}$ , 100% duty cycle on chip enable). Figure 5 shows the same relationship for WRITE cycles.

If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14C88-3 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READS to WRITES; 5) the operating temperature; 6) the  $V_{\text{CC}}$  level; and 7) I/O loading.



**Figure 4:  $I_{\text{CC}}$  (max) Reads**



**Figure 5:  $I_{\text{CC}}$  (max) Writes**

## STK14C88-3

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### Commercial and Industrial Ordering Information

STK14C88-3 N F 45 I TR

— Packaging Option

Blank = Tube  
TR = Tape and Reel

— Temperature Range

Blank = Commercial (0 to 70°C)  
I = Industrial (-40 to 85°C)

— Access Time

35 = 35ns  
45 = 45ns

— Lead Finish

F = 100% Sn (Matte Tin)

— Package

N = Plastic 32-pin 300 mil SOIC  
W = Plastic 32-pin 600 mil DIP

**ORDERING INFORMATION**

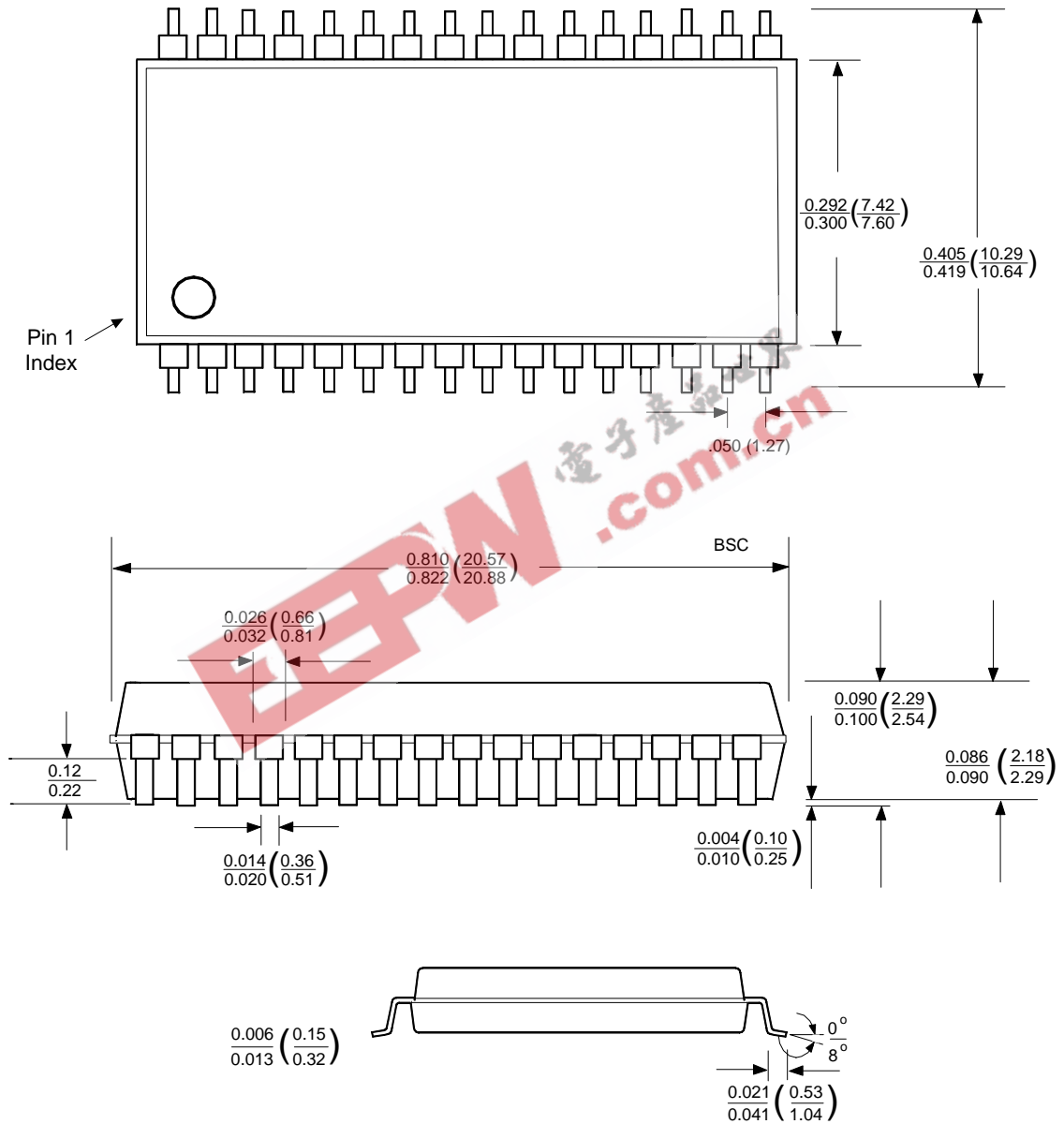
<b>Part Number</b>	<b>Description</b>	<b>Access Times</b>	<b>Temperature</b>
STK14C88-3WF35	3.3V 32Kx8 AutoStore nvSRAM PDIP32-600	35 ns access time	Commercial
STK14C88-3WF45	3.3V 32Kx8 AutoStore nvSRAM PDIP32-600	45 ns access time	Commercial
STK14C88-3NF35	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14C88-3NF45	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14C88-3NF35TR	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14C88-3NF45TR	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14C88-3WF35I	3.3V 32Kx8 AutoStore nvSRAM PDIP32-600	35 ns access time	Industrial
STK14C88-3WF45I	3.3V 32Kx8 AutoStore nvSRAM PDIP32-600	45 ns access time	Industrial
STK14C88-3NF35I	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14C88-3NF45I	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial
STK14C88-3NF35ITR	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14C88-3NF45ITR	3.3V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial

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# STK14C88-3

## Package Diagrams

### 32-pin 300 mil SOIC Gull Wing

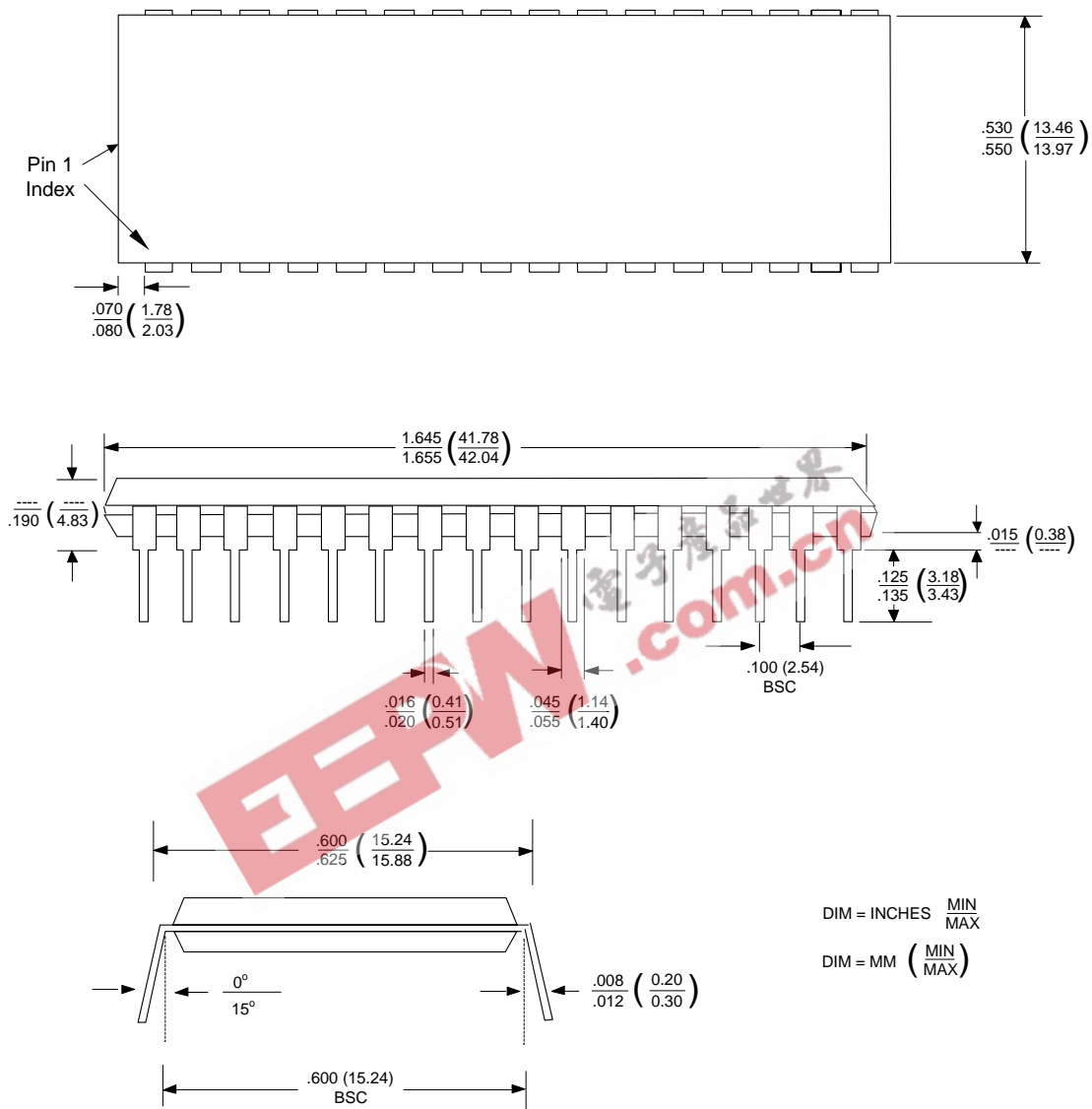


DIM = INCHES  $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm  $\left(\frac{\text{MIN}}{\text{MAX}}\right)$



32-pin 600 mil PDIP



## STK14C88-3

### Document Revision History

Revision	Date	Summary
0.0	January 2003	Added 35 nsec device; added HSB operation; current limiting resistor added to Vcc for extreme power-off slew rate
0.1	February 2003	Added 48 SSOP package
0.2	September 2003	Added lead-free lead finish
0.3	November 2003	Modified pin assignments on 48 SSOP package
0.4	January 2006	Removed 48 pin SSOP package. Removed 55 ns product offering. Added previously unspecified NV <sub>C</sub> and DATA <sub>R</sub> specifications to DC Characteristics.
0.5	March 2006	Removed Leaded Lead Finish
0.6	February 2007	Add Tape Reel Ordering Options Add Product Ordering Code Listing Add Package Drawings Reformat Entire Document
0.7	July 2007	extend definition of t <sub>HZ</sub> (#7) update fig. SRAM READ CYCLE #2, SRAM WRITE CYCLE #1, Note r, Note u and Note v to clarify product usage
2.0	February 2008	Page 1: in the block diagram and elsewhere in the document, removed the "x" from V <sub>CCX</sub> . Page 3: added thermal characteristics. Page 4: in Note g below the SRAM Read Cycles #1 and #2 table, revised note g by deleting "and low during SRAM WRITE cycles; in SRAM Read Cycles #1 & #2 table, revised description for t <sub>ELQX</sub> ; changed Symbol #2 to t <sub>ELEH</sub> for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram; and changed title to add G controlled. Page 7: in Hardware Store Cycle table, removed footnote i for notes 22 and 23. Page 8: in Software Store/Recall Mode Selection table, added footnote n to both rows. Page 11: under HSB Operation, revised first paragraph to read "The HSB pin has a very resistive pullup..." Page 12: added best practices section. Page 15: added access times column to the Ordering codes.

SIMTEK STK14C88-3 Datasheet, February 2008

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