

## FEATURES

- 25, 35, 45 ns Read Access & R/W Cycle Time
- Unlimited Read/Write Endurance
- Automatic Non-volatile STORE on Power Loss
- Non-Volatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 200K STORE Cycles
- 20-Year Non-volatile Data Retention
- Single 3 V + 20%, -10% Power Supply
- Commercial and Industrial Temperatures
- Small Footprint SOIC & SSOP Packages (RoHS-Compliant)

## DESCRIPTION

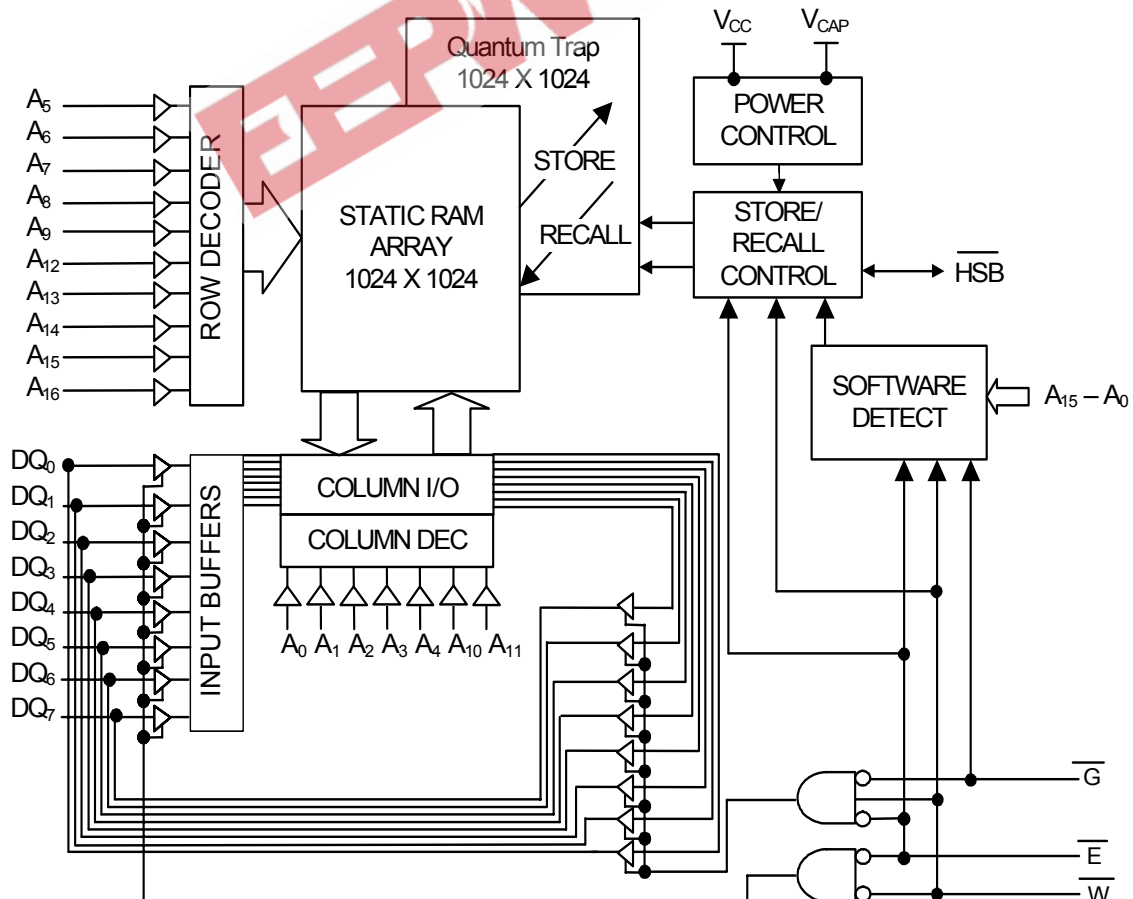
The Simtek STK14CA8 is a 1Mb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power up, data is automatically restored to the SRAM (the *RECALL* operation). Both *STORE* and *RECALL* operations are also available under software control.

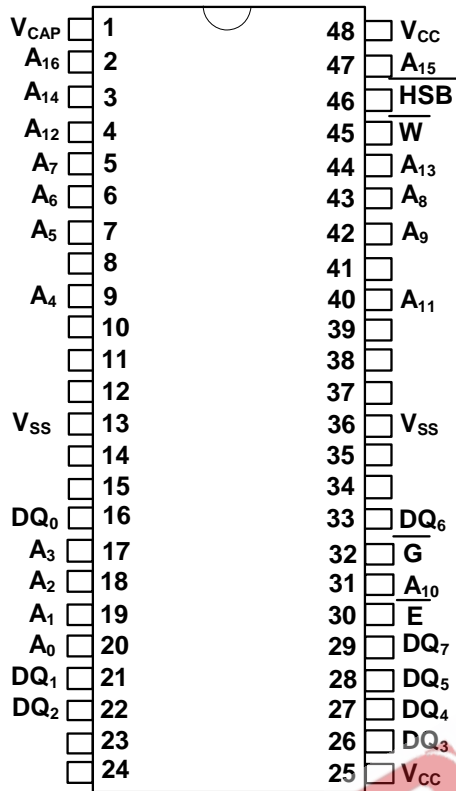
The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

## BLOCK DIAGRAM

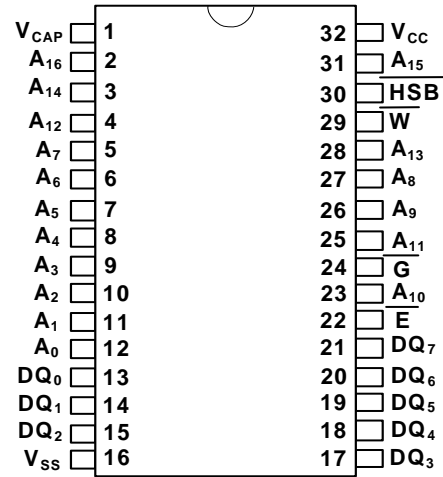


# STK14CA8

## PACKAGES



48 Pin SSOP



32 Pin SOIC



Relative PCB area usage.

See website for detailed package size specifications.

## PIN DESCRIPTIONS

Pin Name	I/O	Description
A <sub>16</sub> -A <sub>0</sub>	Input	Address: The 17 address inputs select one of 131,072 bytes in the nvSRAM array
DQ <sub>7</sub> -DQ <sub>0</sub>	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\bar{E}$	Input	Chip Enable: The active low $\bar{E}$ input selects the device
$\bar{W}$	Input	Write Enable: The active low $\bar{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\bar{E}$
$\bar{G}$	Input	Output Enable: The active low $\bar{G}$ input enables the data output buffers during read cycles. De-asserting $\bar{G}$ high caused the DQ pins to tri-state.
V <sub>CC</sub>	Power Supply	Power: 3.0V, +20%, -10%
$\bar{HSB}$	I/O	Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
V <sub>CAP</sub>	Power Supply	Autostore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V <sub>SS</sub>	Power Supply	Ground
(Blank)	No Connect	Unlabeled pins have no internal connections.

## ABSOLUTE MAXIMUM RATINGS

Voltage on Input Relative to Ground	-0.5V to 4.1V
Voltage on Input Relative to $V_{SS}$	-0.5V to ( $V_{CC} + 0.5V$ )
Voltage on $DQ_{0-7}$ or $\overline{HSB}$	-0.5V to ( $V_{CC} + 0.5V$ )
Temperature under Bias	-55°C to 125°C
Junction Temperature	-55°C to 140°C
Storage Temperature	-65°C to 150°C
Power Dissipation	1W
DC Output Current (1 output at a time, 1s duration)	15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS ( $V_{CC} = 2.7V$ -

Package Thermal Characteristics - See Website at <http://www.simtek.com>

### 3.6V)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
$I_{CC1}$	Average $V_{CC}$ Current		65 55 50		70 60 55	mA	$t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ Dependent on output loading and cycle rate. Values obtained without output loads.
$I_{CC2}$	Average $V_{CC}$ Current during STORE		3		3	mA	All Inputs Don't Care, $V_{CC} = \max$ Average current for duration of STORE cycle ( $t_{STORE}$ )
$I_{CC3}$	Average $V_{CC}$ Current at $t_{AVAV} = 200ns$ 3V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Other Inputs Cycling at CMOS Levels Dependent on output loading and cycle rate. Values obtained without output loads.
$I_{CC4}$	Average $V_{CAP}$ Current during AutoStore Cycle		3		3	mA	All Inputs Don't Care Average current for duration of STORE cycle ( $t_{STORE}$ )
$I_{SB}$	$V_{CC}$ Standby Current (Standby, Stable CMOS Levels)		3		3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ Standby current level after nonvolatile cycle complete
$I_{ILK}$	Input Leakage Current		$\pm 1$		$\pm 1$	$\mu A$	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to $V_{CC}$
$I_{OLK}$	Off-State Output Leakage Current		$\pm 1$		$\pm 1$	$\mu A$	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to $V_{CC}$ , $\overline{E}$ or $\overline{G} \geq V_{IH}$
$V_{IH}$	Input Logic "1" Voltage	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V	All Inputs
$V_{IL}$	Input Logic "0" Voltage	$V_{SS} - 0.5$	0.8	$V_{SS} - 0.5$	0.8	V	All Inputs
$V_{OH}$	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -2mA$
$V_{OL}$	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 4mA$
$T_A$	Operating Temperature	0	70	-40	85	°C	
$V_{CC}$	Operating Voltage	2.7	3.6	2.7	3.6	V	3.3V + 0.3V
$V_{CAP}$	Storage Capacitance	17	120	17	120	$\mu F$	Between $V_{CAP}$ pin and $V_{SS}$ , 5V rated.
$NV_C$	Nonvolatile STORE operations	200		200		K	
$DATA_R$	Data Retention	20		20		Years	@ 55 deg C

Note: The HSB pin has  $I_{OUT} = -10 \mu A$  for  $V_{OH}$  of 2.4 V, this parameter is characterized but not tested.

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## AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

## CAPACITANCE<sup>b</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C <sub>IN</sub>	Input Capacitance	7	pF	ΔV = 0 to 3V
C <sub>OUT</sub>	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: These parameters are guaranteed but not tested.

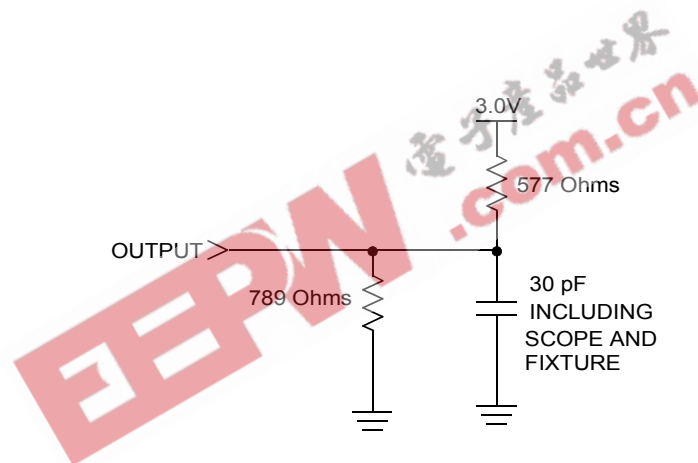


Figure 1: AC Output Loading

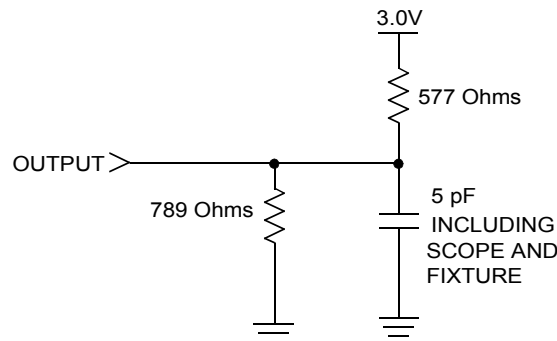


Figure 2: AC Output Loading for Tristate Specs (t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>WLQZ</sub>, t<sub>WHQZ</sub>, t<sub>GLQX</sub>, t<sub>GHQZ</sub>)

## SRAM READ CYCLES #1 & #2

NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1		$t_{ELQV}$	$t_{ACS}$	Chip Enable Access Time		25		35		45	ns
2	$t_{AVAV}^c$	$t_{AVAV}^c$	$t_{RC}$	Read Cycle Time	25		35		45		ns
3	$t_{AVQV}^d$	$t_{AVQV}^d$	$t_{AA}$	Address Access Time		25		35		45	ns
4		$t_{GLQV}$	$t_{OE}$	Output Enable to Data Valid		12		15		20	ns
5	$t_{AXQX}^d$	$t_{AXQX}^d$	$t_{OH}$	Output Hold after Address Change	3		3		3		ns
6		$t_{ELQX}$	$t_{LZ}$	Chip Enable to Output Active	3		3		3		ns
7		$t_{EHQZ}^e$	$t_{HZ}$	Chip Disable to Output Inactive		10		13		15	ns
8		$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		ns
9		$t_{GHQZ}^e$	$t_{OHZ}$	Output Disable to Output Inactive		10		13		15	ns
10		$t_{ELICCH}^b$	$t_{PA}$	Chip Enable to Power Active	0		0		0		ns
11		$t_{EHICCL}^b$	$t_{PS}$	Chip Disable to Power Standby		25		35		45	ns

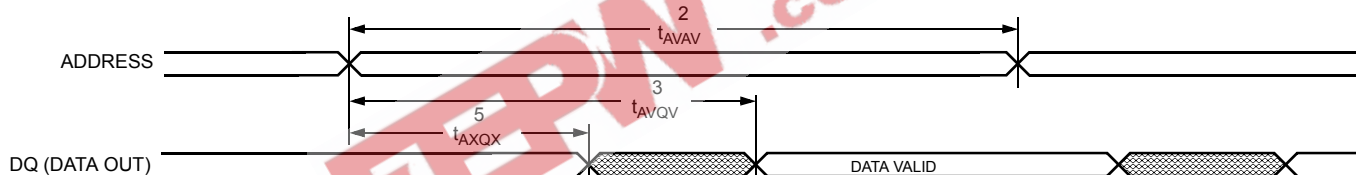
Note c:  $\overline{W}$  must be high during SRAM READ cycles.

Note d: Device is continuously selected with  $\overline{E}$  and  $\overline{G}$  both low

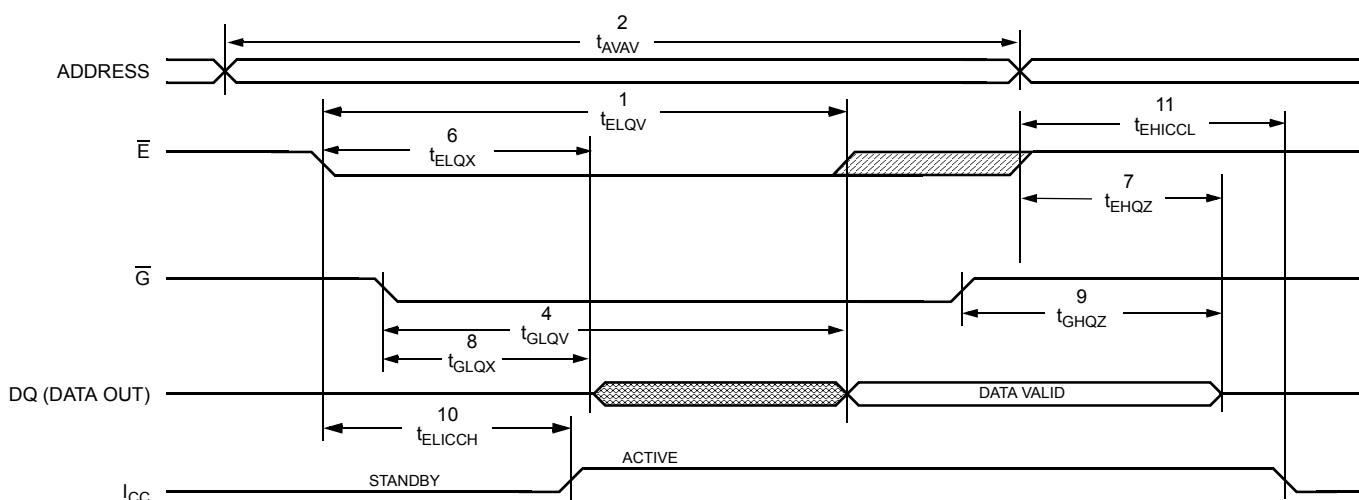
Note e: Measured  $\pm 200mV$  from steady state output voltage.

Note f: HSB must remain high during READ and WRITE cycles.

### SRAM READ CYCLE #1: Address Controlled<sup>c,d,f</sup>



### SRAM READ CYCLE #2: $\overline{E}$ Controlled<sup>c,f</sup>



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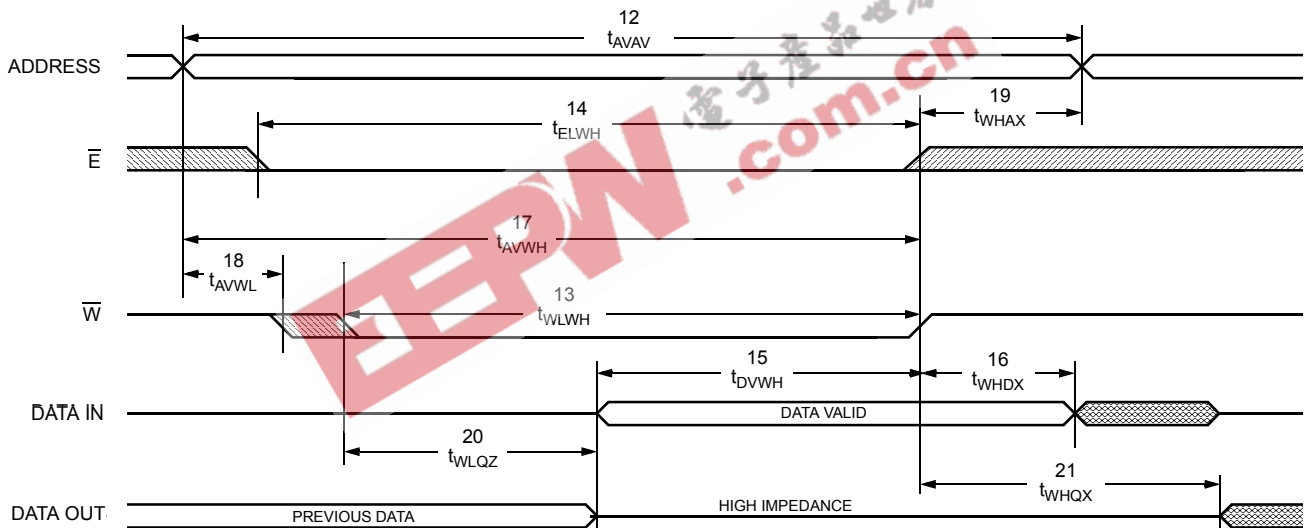
## SRAM WRITE CYCLES #1 & #2

NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAV}$	$t_{AVAV}$	$t_{WC}$	Write Cycle Time	25		35		45		ns
13	$t_{WLWH}$	$t_{WLEH}$	$t_{WP}$	Write Pulse Width	20		25		30		ns
14	$t_{ELWH}$	$t_{ELEH}$	$t_{CW}$	Chip Enable to End of Write	20		25		30		ns
15	$t_{DVWH}$	$t_{DVEH}$	$t_{DW}$	Data Set-up to End of Write	10		12		15		ns
16	$t_{WHDX}$	$t_{EHDX}$	$t_{DH}$	Data Hold after End of Write	0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}$	$t_{AW}$	Address Set-up to End of Write	20		25		30		ns
18	$t_{AVWL}$	$t_{AVEL}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}$	$t_{WR}$	Address Hold after End of Write	0		0		0		ns
20	$t_{WLQZ}^{e,9}$		$t_{WZ}$	Write Enable to Output Disable		10		13		15	ns
21	$t_{WHQX}$		$t_{OW}$	Output Active after End of Write	3		3		3		ns

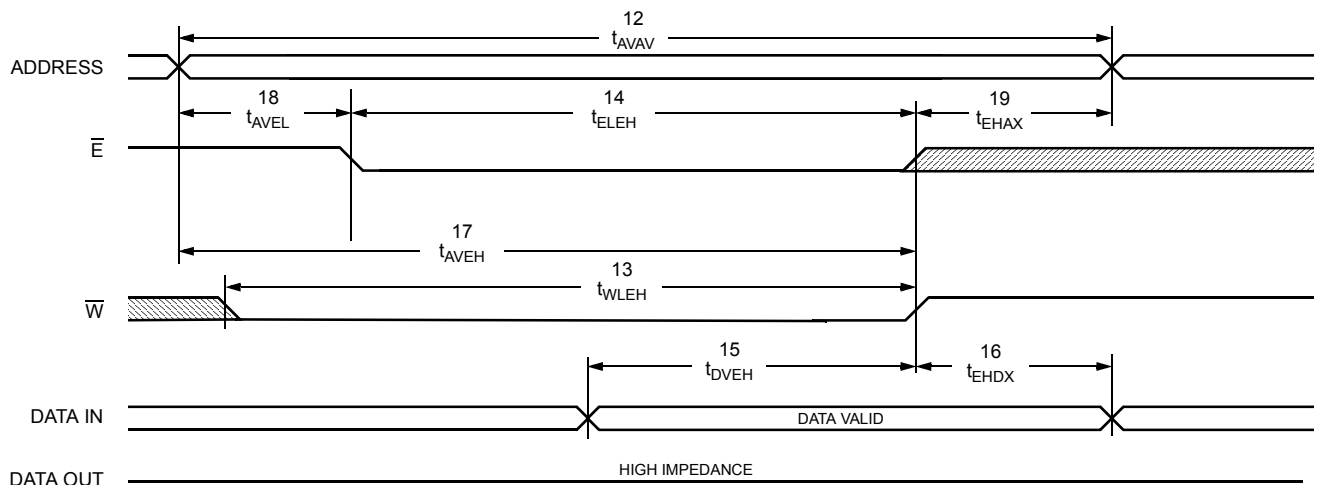
Note g: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.

Note h:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

### SRAM WRITE CYCLE #1: $\bar{W}$ Controlled<sup>g,h</sup>



### SRAM WRITE CYCLE #2: $\bar{E}$ Controlled<sup>g,h</sup>



## AutoStore/POWER-UP RECALL

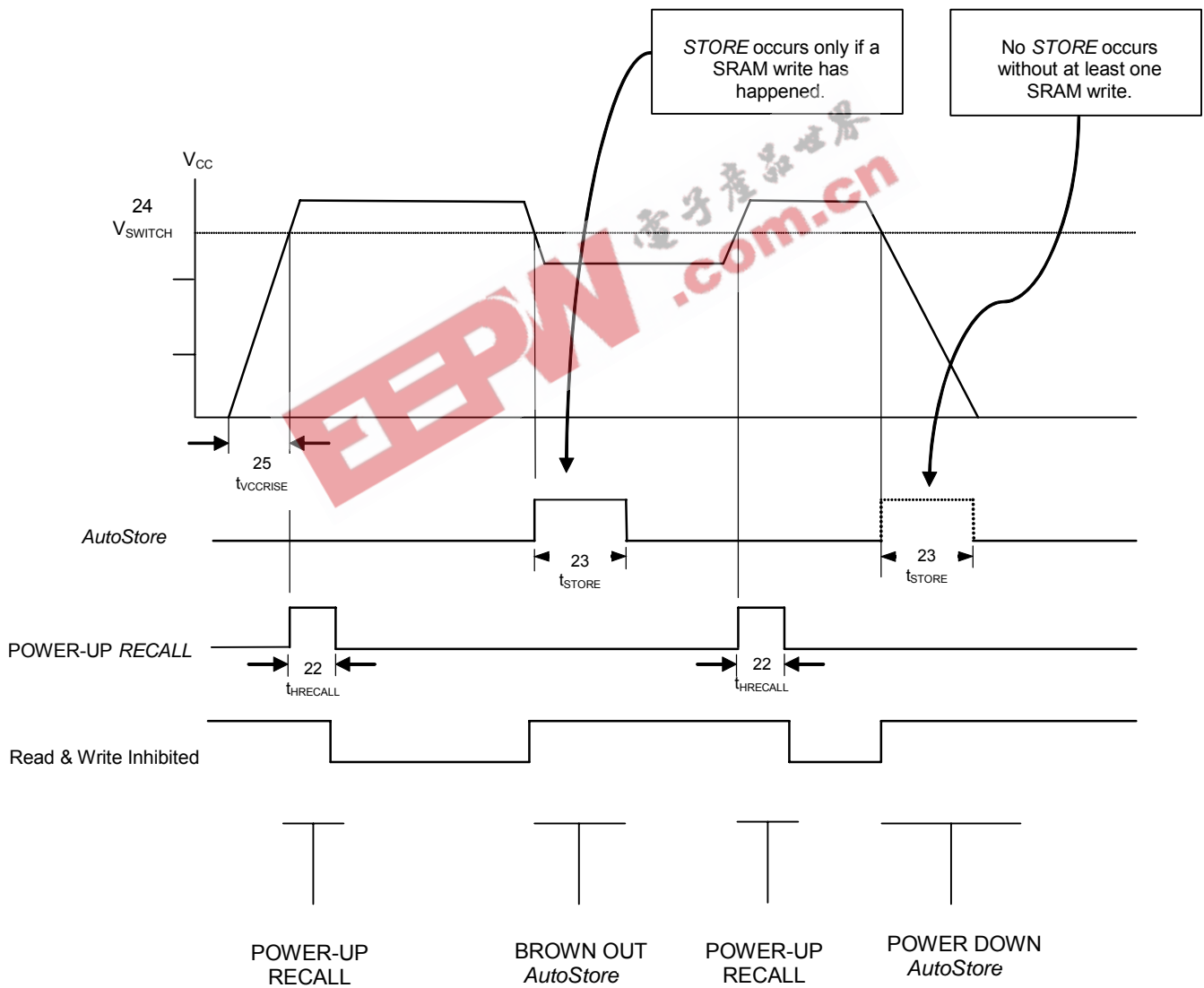
NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{HRECALL}$		Power-up <i>RECALL</i> Duration		20	ms	i
23	$t_{STORE}$	$t_{HLHZ}$	<i>STORE</i> Cycle Duration		12.5	ms	j,k
24	$V_{SWITCH}$		Low Voltage Trigger Level		2.65	V	
25	$V_{CCRISE}$		$V_{CC}$ Rise Time	150		$\mu$ s	

Note i:  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$

Note j: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place

Note k: Industrial Grade Devices require 15 ms MAX.

## AutoStore/POWER-UP RECALL



Note: Read and Write cycles will be ignored during *STORE*, *RECALL* and while  $V_{CC}$  is below  $V_{SWITCH}$

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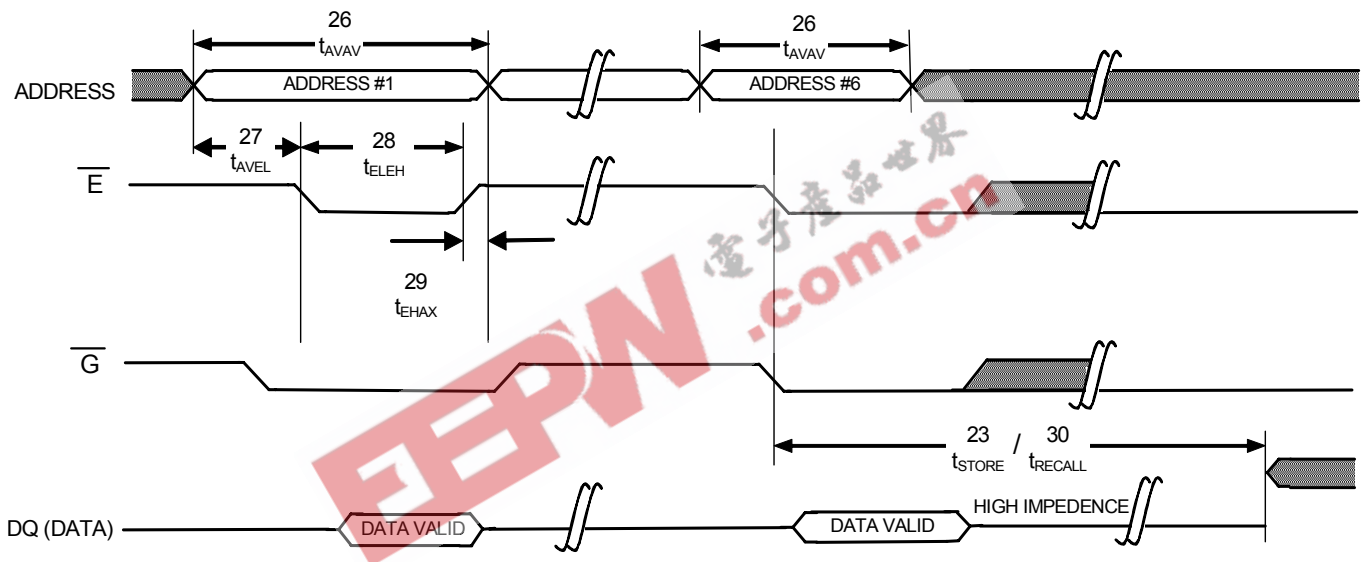
## SOFTWARE-CONTROLLED STORE/RECALL CYCLE<sup>l,m</sup>

NO.	Symbols			PARAMETER	STK14CA8-35		STK14CA8-35		STK14CA8-45		UNITS	NOTES
	$\overline{E}$ Cont	$\overline{G}$ Cont	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
26	$t_{AVAV}$	$t_{AVAV}$	$t_{RC}$	STORE/RECALL Initiation Cycle Time	25		35		45		ns	m
27	$t_{AVEL}$	$t_{AVGL}$	$t_{AS}$	Address Set-up Time	0		0		0		ns	
28	$t_{ELEH}$	$t_{GLGH}$	$t_{CW}$	Clock Pulse Width	20		25		30		ns	
29	$t_{EHAX}$	$t_{GHAX}$		Address Hold Time	1		1		1		ns	
30	$t_{RECALL}$	$t_{RECALL}$		RECALL Duration		50		50		50	$\mu$ s	

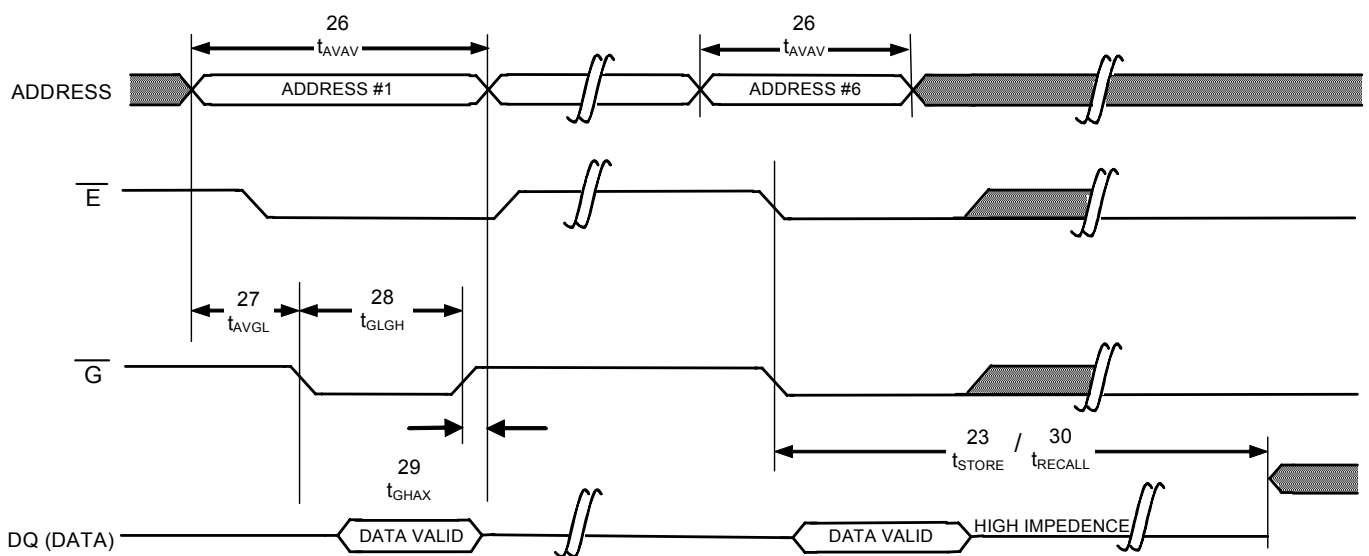
Note l: The software sequence is clocked with  $\overline{E}$  controlled READs or  $\overline{G}$  controlled READs

Note m: The six consecutive addresses must be read in the order listed in the Mode Selection Table.  $\overline{W}$  must be high during all six consecutive cycles.

### SOFTWARE STORE/RECALL CYCLE: $\overline{E}$ CONTROLLED<sup>m</sup>



### SOFTWARE STORE/RECALL CYCLE: $\overline{G}$ CONTROLLED<sup>m</sup>



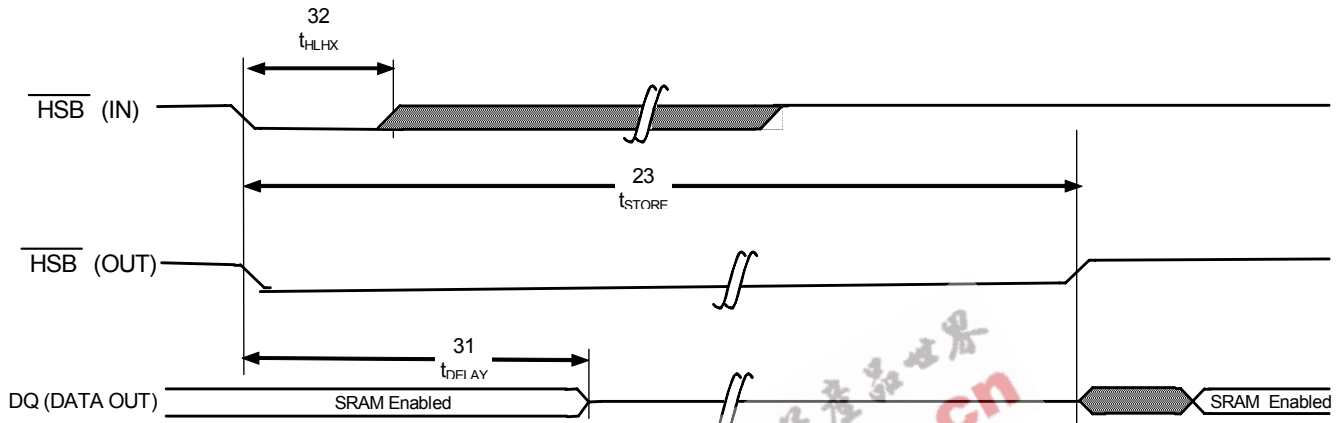


## HARDWARE STORE CYCLE

	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
31	$t_{\text{DELAY}}$	$t_{\text{HLQZ}}$	Hardware STORE to SRAM Disabled	1	70	$\mu\text{s}$	n
32	$t_{\text{HLHX}}$		Hardware STORE Pulse Width	15		ns	

Note n: On a hardware STORE initiation, SRAM operation continues to be enabled for time  $t_{\text{DELAY}}$  to allow read/write cycles to complete

## HARDWARE STORE CYCLE



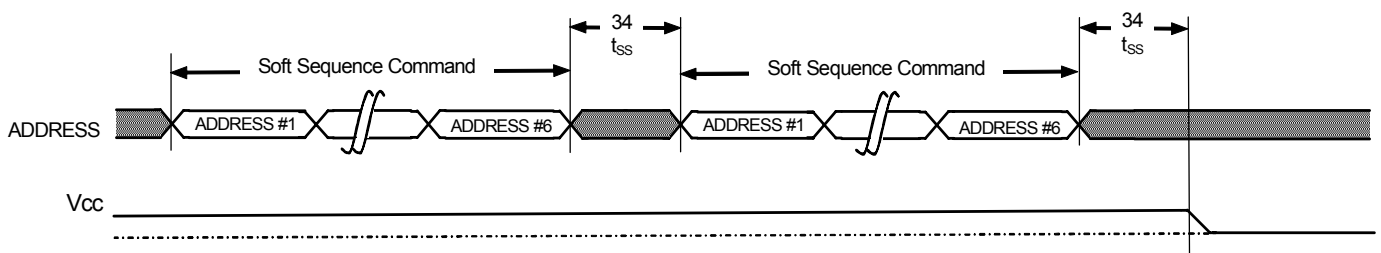
## Soft Sequence Commands

NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard			MIN	MAX		
34	$t_{\text{SS}}$		Soft Sequence Processing Time		70	$\mu\text{s}$	o,p

Notes:

o: This is the amount of time that it takes to take action on a soft sequence command.  $V_{\text{CC}}$  power must remain high to effectively register command.

p: Commands like Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.



# STK14CA8

## MODE SELECTION

$\bar{E}$	$\bar{W}$	$\bar{G}$	A <sub>15</sub> -A <sub>0</sub>	Mode	I/O	Power	Notes
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	q,r,s
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	q,r,s
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I <sub>CC2</sub>	q,r,s
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	q,r,s

### Notes

q: The six consecutive addresses must be in the order listed.  $\bar{W}$  must be high during all six consecutive cycles to enable a nonvolatile cycle.

r: While there are 17 addresses on the STK14CA8, only the lower 16 are used to control software modes

s: I/O state depends on the state of  $\bar{G}$ . The I/O table shown assumes  $\bar{G}$  low

## nvSRAM OPERATION

### nvSRAM

The STK14CA8 nvSRAM is made up of two functional components paired in the same physical cell. These are the SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates like a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The STK14CA8 supports unlimited read and writes like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

### SRAM READ

The STK14CA8 performs a READ cycle whenever  $\overline{E}$  and  $\overline{G}$  are low while  $\overline{W}$  and HSB are high. The address specified on pins  $A_{0-16}$  determine which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\overline{E}$  and  $\overline{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{E}$  or  $\overline{G}$  is brought high, or  $\overline{W}$  and HSB is brought low.

### SRAM WRITE

A WRITE cycle is performed whenever  $\overline{E}$  and  $\overline{W}$  are low and HSB is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{E}$  or  $\overline{W}$  goes high at the end of the cycle. The data on the common I/O pins DQ0-7 will be written into memory if it is valid  $t_{DVWH}$  before the end of a  $\overline{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\overline{E}$  controlled WRITE.

It is recommended that  $\overline{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If  $\overline{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\overline{W}$  goes low.

### AutoStore OPERATION

The STK14CA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store (activated by HSB), Software Store (activated by an address sequence), and AutoStore (on power down).

AutoStore operation is a unique feature of Simtek QuantumTrap technology is enabled by default on the STK14CA8.

During normal operation, the device will draw current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part will automatically disconnect the  $V_{CAP}$  pin from  $V_{CC}$ . A STORE operation will be initiated with power provided by the  $V_{CAP}$  capacitor.

Figure 3 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on  $\overline{W}$  to hold it inactive during power up.

To reduce unneeded nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation

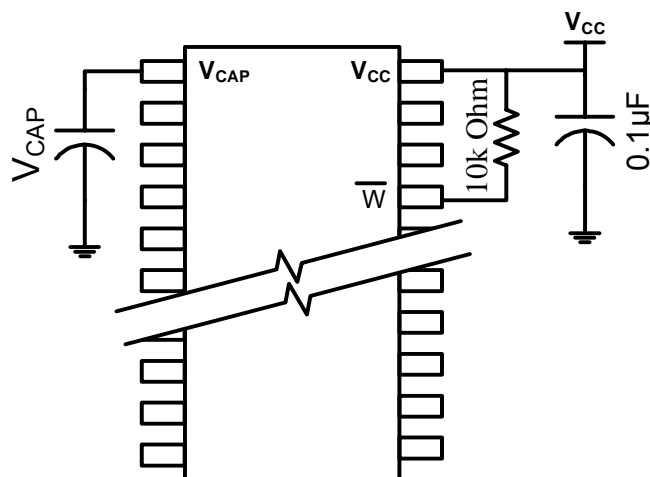


Figure 3. AutoStore Mode

# STK14CA8

has taken place. The  $\overline{\text{HSB}}$  signal can be monitored by the system to detect an AutoStore cycle is in progress.

## HARDWARE STORE ( $\overline{\text{HSB}}$ ) OPERATION

The STK14CA8 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the STORE operations. The  $\overline{\text{HSB}}$  pin can be used to request a hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven low, the STK14CA8 will conditionally initiate a STORE operation after  $t_{\text{DELAY}}$ . An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations that are in progress when  $\overline{\text{HSB}}$  is driven low by any means are given time to complete before the STORE operation is initiated. After  $\overline{\text{HSB}}$  goes low, the STK14CA8 will continue to allow SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations may take place. If a WRITE is in progress when  $\overline{\text{HSB}}$  is pulled low, it will be allowed a time,  $t_{\text{DELAY}}$ , to complete. However, any SRAM WRITE cycles requested after  $\overline{\text{HSB}}$  goes low will be inhibited until  $\overline{\text{HSB}}$  returns high.

If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

## HARDWARE RECALL (POWER-UP)

During power up or after any low-power condition ( $V_{\text{CC}} < V_{\text{SWITCH}}$ ), an internal RECALL request will be latched. When  $V_{\text{CC}}$  once again exceeds the sense voltage of  $V_{\text{SWITCH}}$ , a RECALL cycle will automatically be initiated and will take  $t_{\text{HRECALL}}$  to complete.

## SOFTWARE STORE

Data can be transferred from the SRAM to the non-volatile memory by a software address sequence. The STK14CA8 software STORE cycle is initiated by executing sequential  $\overline{\text{E}}$  controlled or  $\overline{\text{G}}$  controlled READ cycles from six specific address locations in exact order. During the STORE cycle, previous data is erased and then the new data is programmed into the nonvolatile elements. Once a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed.

To initiate the software STORE cycle, the following READ sequence must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x8FC0	Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence and that  $\overline{\text{G}}$  is active. After the  $t_{\text{STORE}}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

## SOFTWARE RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of  $\overline{\text{E}}$  controlled or  $\overline{\text{G}}$  controlled READ operations must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x4C63	Initiate RECALL Cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time, the SRAM will once again be ready for READ or WRITE operations. The RECALL operation in no way alters the data in the nonvolatile storage elements.

## DATA PROTECTION

The STK14CA8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low-voltage condition is detected when  $V_{CC} < V_{SWITCH}$ .

If the STK14CA8 is in a WRITE mode (both  $\bar{E}$  and  $\bar{W}$  low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on  $\bar{E}$  or  $\bar{W}$  is detected. This protects against inadvertent writes during power up or brown out conditions.

## NOISE CONSIDERATIONS

The STK14CA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1  $\mu\text{F}$  connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals will reduce circuit noise.

## LOW AVERAGE ACTIVE POWER

CMOS technology provides the STK14CA8 with the benefit of power supply current that scales with cycle time. Less current will be drawn as the memory cycle time becomes longer than 50 ns. Figure 4 shows the relationship between  $I_{CC}$  and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range,  $V_{CC}=3.6\text{V}$ , and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14CA8 depends on the following items:

- 1 The duty cycle of chip enable
- 2 The overall cycle rate for operations
- 3 The ratio of READS to WRITES
- 4 The operating temperature
- 5 The  $V_{CC}$  Level
- 6 I/O Loading

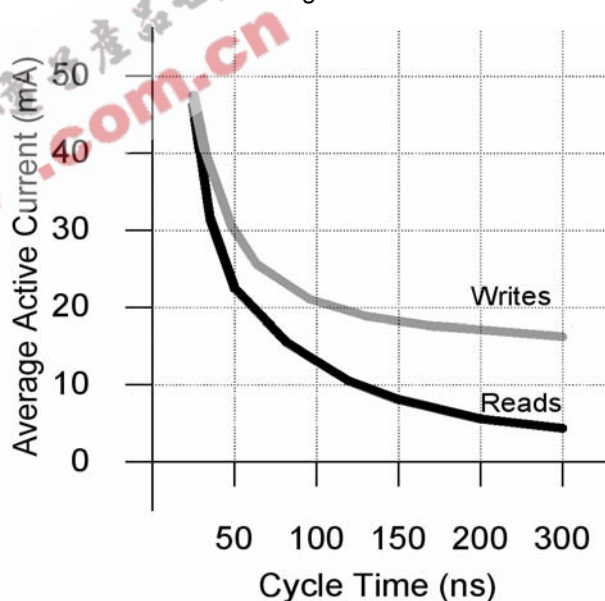


Figure 4 - Current vs Cycle Time

# STK14CA8

## PREVENTING AUTOSTORE

The AutoStore function can be disabled by initiating an *AutoStore Disable* sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the *AutoStore Disable* sequence, the following sequence of  $\bar{E}$  controlled or  $\bar{G}$  controlled READ operations must be performed:

- 1 Read Address 0x4E38 Valid READ
- 2 Read Address 0xB1C7 Valid READ
- 3 Read Address 0x83E0 Valid READ
- 4 Read Address 0x7C1F Valid READ
- 5 Read Address 0x703F Valid READ
- 6 Read Address 0x8B45 AutoStore Disable

The AutoStore can be re-enabled by initiating an *AutoStore Enable* sequence. A sequence of READ

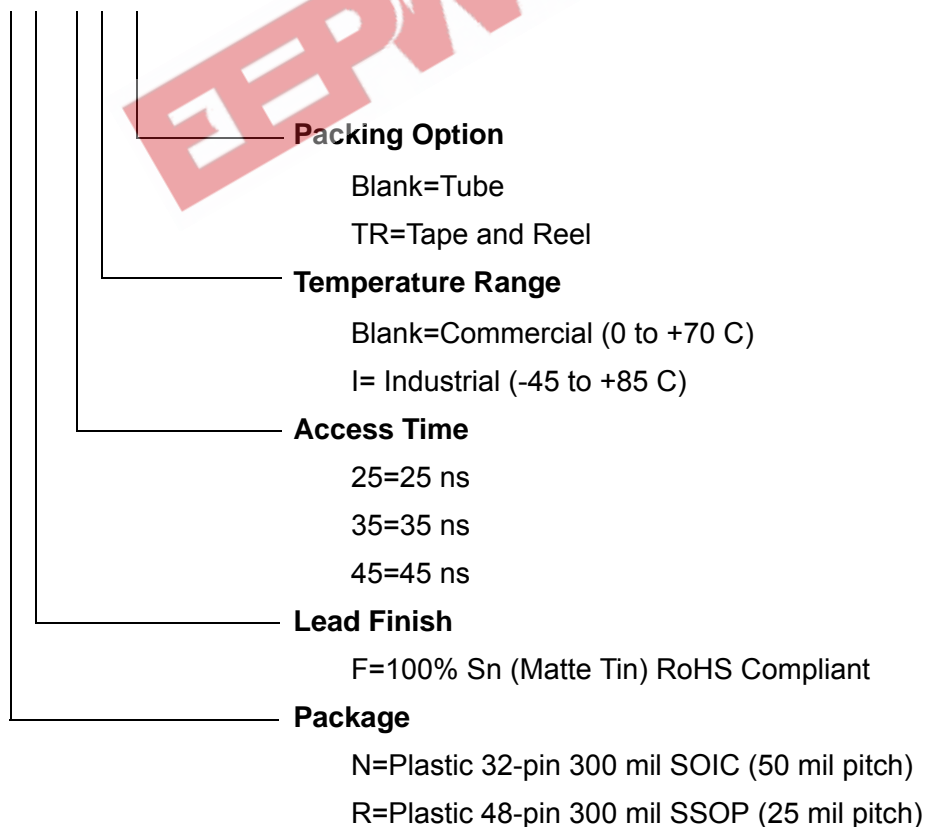
operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Enable* sequence, the following sequence of  $\bar{E}$  controlled or  $\bar{G}$  controlled READ operations must be performed:

- 1 Read Address 0x4E38 Valid READ
- 2 Read Address 0xB1C7 Valid READ
- 3 Read Address 0x83E0 Valid READ
- 4 Read Address 0x7C1F Valid READ
- 5 Read Address 0x703F Valid READ
- 6 Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) needs to be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

## ORDERING INFORMATION

### STK14CA8-R F 45 I TR





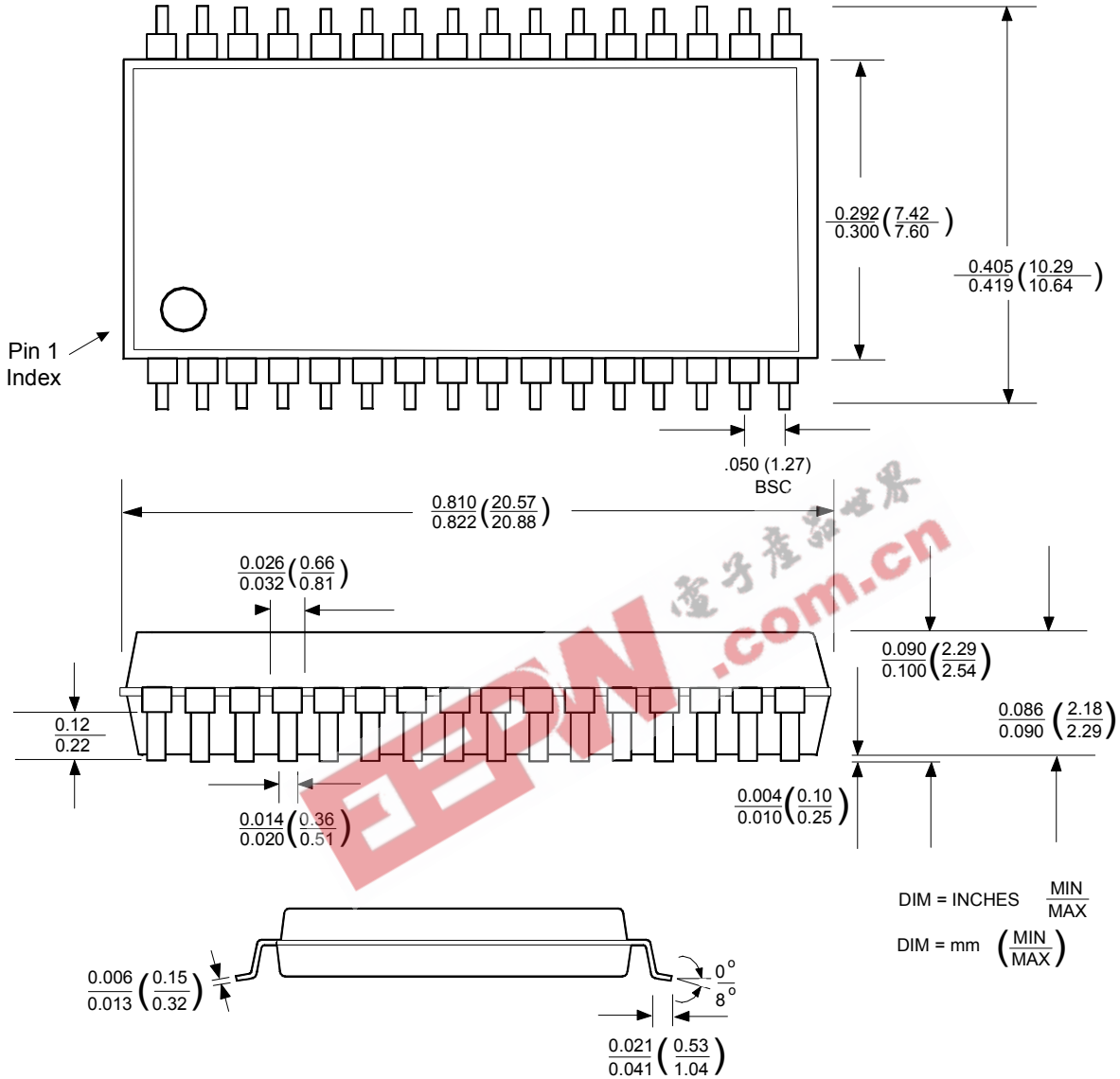
## ORDERING CODES

STK14CA8-NF25	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-NF35	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-NF45	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-NF25TR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-NF35TR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-NF45TR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Commercial
STK14CA8-RF25	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-RF35	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-RF45	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-RF25TR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-RF35TR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-RF45TR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Commercial
STK14CA8-NF25I	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-NF35I	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-NF45I	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-NF25ITR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-NF35ITR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-NF45ITR	3V 128Kx8 AutoStore nvSRAM	SOP32-300	Industrial
STK14CA8-RF25I	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial
STK14CA8-RF35I	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial
STK14CA8-RF45I	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial
STK14CA8-RF25ITR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial
STK14CA8-RF35ITR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial
STK14CA8-RF45ITR	3V 128Kx8 AutoStore nvSRAM	SSOP48-300	Industrial

# STK14CA8

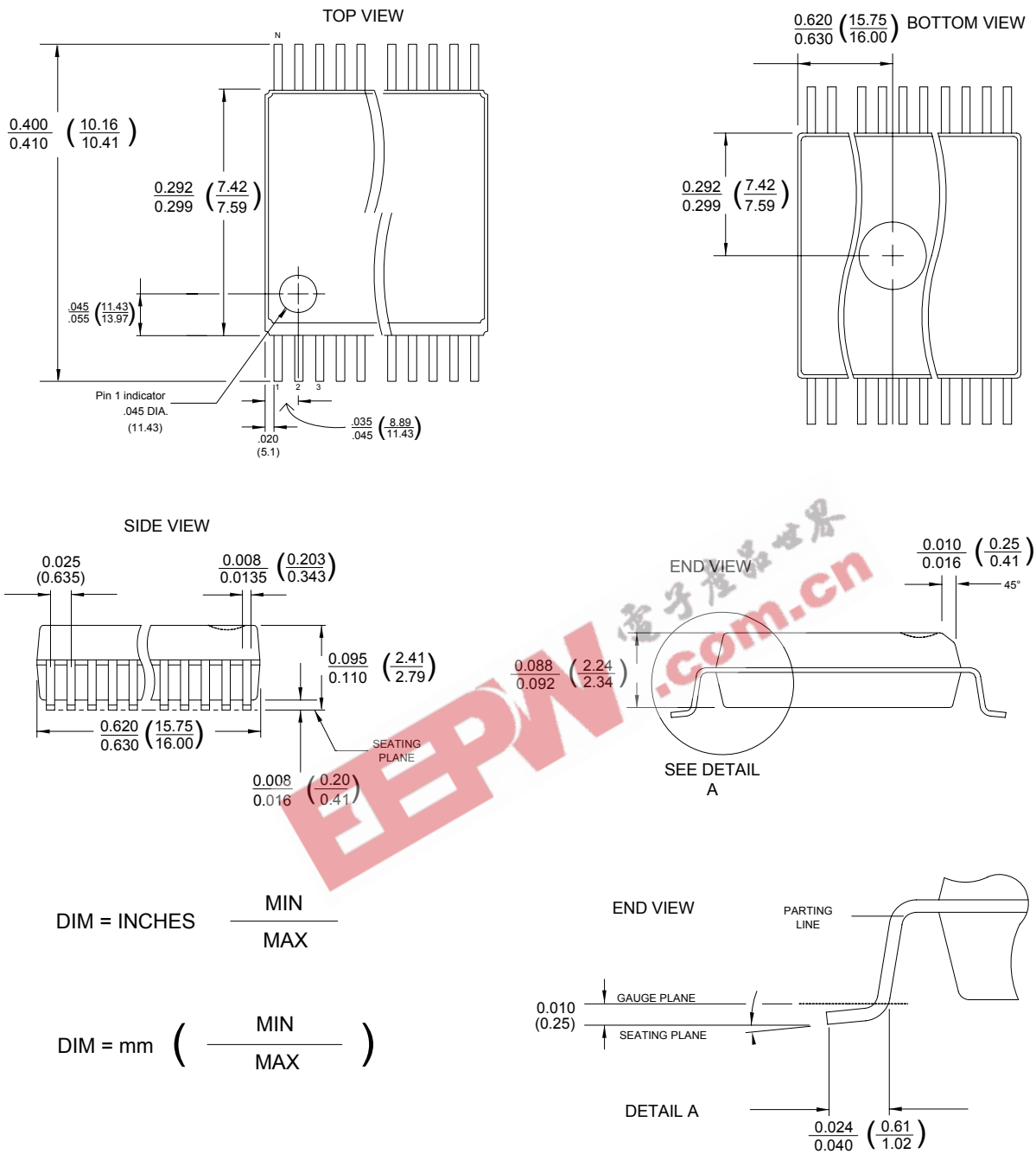
## PACKAGE DRAWINGS

### 32 Pin 300 mil SOIC





## 48 Pin 300 mil SSOP



# STK14CA8

## Document Revision History

Rev	Date	Change																																																												
0.0	January 2003	Publish New Datasheet																																																												
0.1	May 2003	Add 48-pin SSOP, Modify AutoStore Diagram, Update Mode Selection Table and Absolute Maximum Ratings, Added $\bar{G}$ controlled software store.																																																												
0.2	September 2003	Added lead-free finish																																																												
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1.4	March 2006	Removed Lead Plated Lead Finish																																												
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