

Preliminary

FEATURES

- 15, 25, 45 ns Read Access and R/W Cycle Time
- Unlimited Read/Write Endurance
- Automatic Non-volatile STORE on Power Loss
- Non-Volatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 200K STORE Endurance
- 20-Year Non-volatile Data Retention
- Single 3.0V +20%, -10% Operation
- Commercial, Industrial Temperatures
- 44-pin 400-mil TSOPII (RoHS-Compliant)
- 48-ball Fine Pitch Ball Grid Array (FBGA)

DESCRIPTION

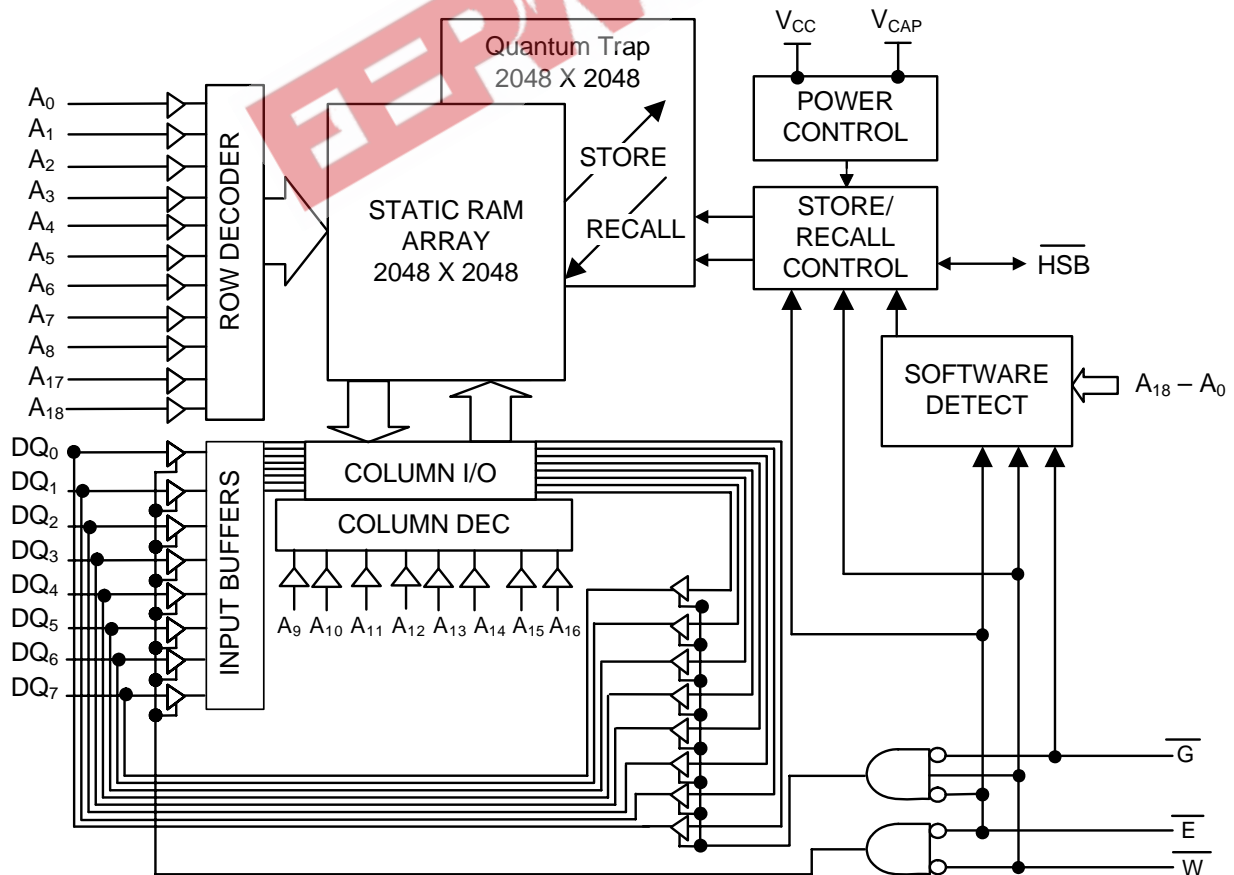
The Simtek STK14EC8 is a 4MB fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

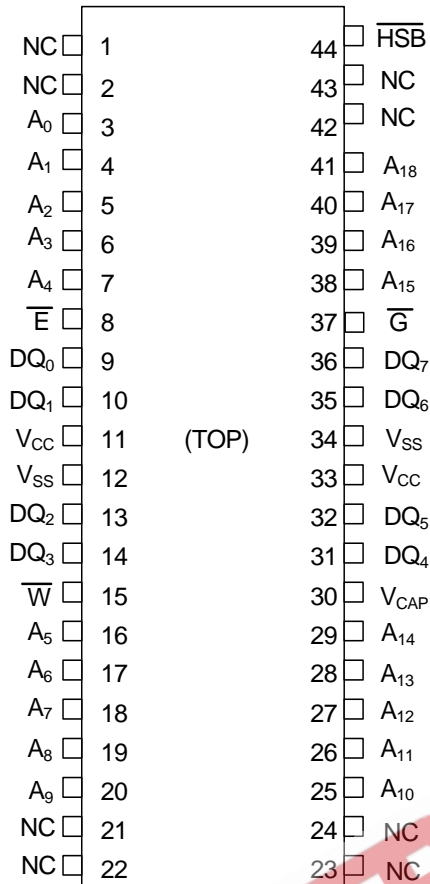
The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power up, data is automatically restored to the SRAM (the *RECALL* operation). Both *STORE* and *RECALL* operations are also available under software control.

The Simtek nvSRAM is the highest performance, most reliable non-volatile memory available.

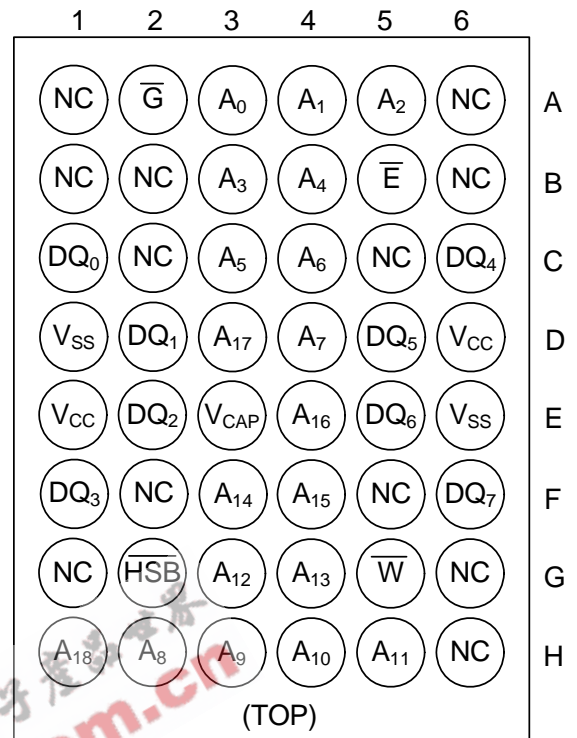
BLOCK DIAGRAM





44-Pin TSOP-II

(See mechanical drawing on page 17)



48-Ball FBGA

(See mechanical drawing on page 18)

PIN DESCRIPTIONS

| Pin Name | I/O | Description |
|----------------------------------|--------------|--|
| A ₁₈ -A ₀ | Input | Address: The 19 address inputs select one of 524,288 bytes in the nvSRAM array |
| DQ ₇ -DQ ₀ | I/O | Data: Bi-directional 8-bit data bus for accessing the nvSRAM |
| \bar{E} | Input | Chip Enable: The active low \bar{E} input selects the device |
| \bar{W} | Input | Write Enable Input, Active Low: When selected low, enables data on the IO pins to be written to the address location latched by the falling edge of \bar{CE} . |
| \bar{G} | Input | Output Enable: The active low \bar{G} input enables the data output buffers during read cycles. De-asserting \bar{G} high causes the DQ pins to tri-state. |
| V _{CC} | Power Supply | Power: 3.0V, +20%, -10% |
| HSB | I/O | Hardware Store Busy: When low this output indicates a Store is in progress (also low during power up while busy). When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional). |
| V _{CAP} | Power Supply | Autostore Capacitor: Supplies power to the nvSRAM during a power loss to store data from SRAM to nonvolatile storage elements. |
| V _{SS} | Power Supply | Ground |
| NC | No Connect | This pin is not connected to the die. (Do not connect in design; reserved for future use) |

ABSOLUTE MAXIMUM RATINGS^a

| | |
|---|-----------------------------------|
| Voltage on Input Relative to Ground | -0.5V to 4.1V |
| Voltage on Input Relative to V _{SS} | -0.5V to (V _{CC} + 0.5V) |
| Voltage on DQ ₀₋₇ or $\overline{\text{HSB}}$ | -0.5V to (V _{CC} + 0.5V) |
| Temperature under Bias | -55°C to 125°C |
| Junction Temperature | -55°C to 140°C |
| Storage Temperature | -65°C to 150°C |
| Power Dissipation | 1W |
| DC Output Current (1 output at a time, 1s duration) | 15mA |

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TF (TSOP-II 44) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} tbd; θ_{ja} tbd [0fpm], tbd [200fpm], tbd C/W [500fpm].

BF (FBGA48) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} tbd C/W; θ_{ja} tbd [0fpm], tbd [200fpm], tbd C/W [500fpm].

DC CHARACTERISTICS

(V_{CC} = 2.7V-3.6V)

| SYMBOL | PARAMETER | COMMERCIAL | | INDUSTRIAL | | UNITS | NOTES |
|-------------------|---|-----------------------|-----------------------|-----------------------|-----------------------|----------------|---|
| | | MIN | MAX | MIN | MAX | | |
| I _{CC1} | Average V _{CC} Current | | 70 65 50 | | 75 70 52 | mA mA mA | t _{AVAV} = 15ns t _{AVAV} = 25ns t _{AVAV} = 45ns Dependent on output loading and cycle rate. Values obtained without output loads. |
| I _{CC2} | Average V _{CC} Current during STORE | | 6 | | 6 | mA | All Inputs Don't Care, V _{CC} = max Average current for duration of STORE cycle (t _{STORE}) |
| I _{CC3} | Average V _{CC} Current at t _{AVAV} = 200ns 3V, 25°C, Typical | | 13 | | 13 | mA | $\overline{W} \geq (V_{CC} - 0.2V)$ All Other Inputs Cycling at CMOS Levels Dependent on output loading and cycle rate. Values obtained without output loads. |
| I _{CC4} | Average V _{CAP} Current during AutoStore™ Cycle | | 6 | | 6 | mA | All Inputs Don't Care Average current for duration of STORE cycle (t _{STORE}) |
| I _{SB} | V _{CC} Standby Current (Standby, Stable CMOS Levels) | | 3 | | 3 | mA | $\overline{E} \geq (V_{CC} - 0.2V)$ All Others V _{IN} ≤ 0.2V or ≥ (V _{CC} -0.2V) Standby current level after nonvolatile cycle complete |
| I _{ILK} | Input Leakage Current | | ±1 | | ±1 | µA | V _{CC} = max V _{IN} = V _{SS} to V _{CC} |
| I _{OLK} | Off-State Output Leakage Current | | ±1 | | ±1 | µA | V _{CC} = max V _{IN} = V _{SS} to V _{CC} , \overline{E} or $\overline{G} \geq V_{IH}$ |
| V _{IH} | Input Logic "1" Voltage | 2.0 | V _{CC} + 0.5 | 2.0 | V _{CC} + 0.5 | V | All Inputs |
| V _{IL} | Input Logic "0" Voltage | V _{SS} - 0.5 | 0.8 | V _{SS} - 0.5 | 0.8 | V | All Inputs |
| V _{OH} | Output Logic "1" Voltage | 2.4 | | 2.4 | | V | I _{OUT} = -2mA (except $\overline{\text{HSB}}$) |
| V _{OL} | Output Logic "0" Voltage | | 0.4 | | 0.4 | V | I _{OUT} = 4mA |
| T _A | Operating Temperature | 0 | 70 | -40 | 85 | °C | |
| V _{CC} | Operating Voltage | 2.7 | 3.6 | 2.7 | 3.6 | V | 3.0V nominal |
| V _{CAP} | Storage Capacitance | 61 | 82 | 61 | 180 | µF | Between V _{CAP} pin and V _{SS} , 5V rated (Nom. 68 µF to 150 µF +20%, - 10%) |
| NV _C | Nonvolatile STORE operations | 200 | | 200 | | K | |
| DATA _R | Data Retention | 20 | | 20 | | Years | @ 55 deg C |

Note: The HSB pin has I_{OUT} = -10 µA for V_{OH} of 2.4 V. This parameter is characterized but not tested.

AC TEST CONDITIONS

| | |
|--|--------------------|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | ≤ 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Figure 1 and 2 |

CAPACITANCE^b (T_A = 25°C, f = 1.0MHz)

| SYMBOL | PARAMETER | MAX | UNITS | CONDITIONS |
|------------------|--------------------|-----|-------|--------------|
| C _{IN} | Input Capacitance | 7 | pF | ΔV = 0 to 3V |
| C _{OUT} | Output Capacitance | 7 | pF | ΔV = 0 to 3V |

Note b: These parameters are guaranteed but not tested.

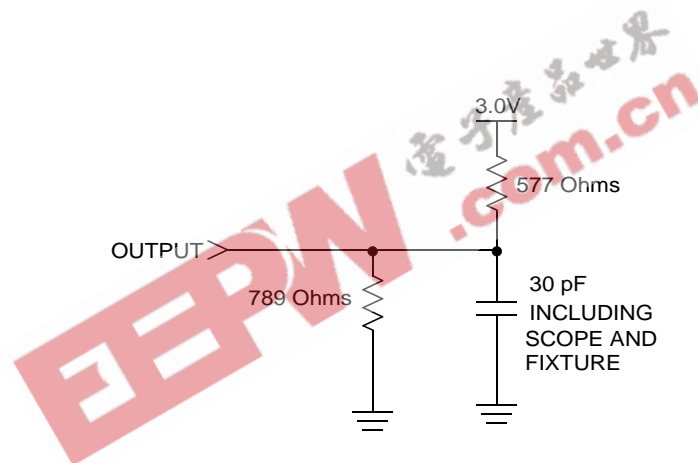


Figure 1: AC Output Loading

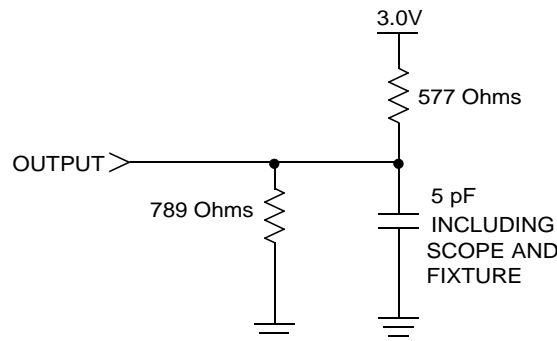


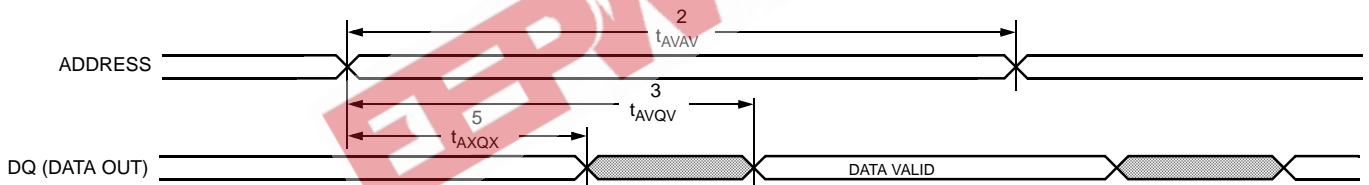
Figure 2: AC Output Loading for Tristate Specs (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ})

SRAM READ CYCLES #1 & #2

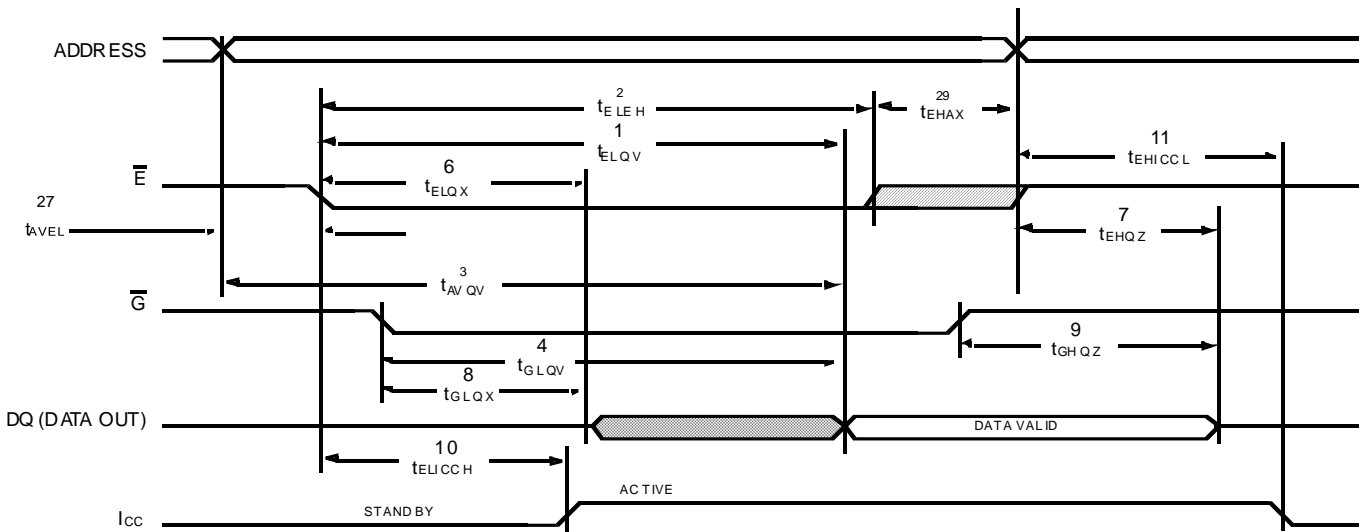
| NO. | SYMBOLS | | | PARAMETER | STK14EC8-15 | | STK14EC8-25 | | STK14EC8-45 | | UNITS |
|-----|--------------|----------------|-----------|---|-------------|-----|-------------|-----|-------------|-----|-------|
| | #1 | #2 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | | t_{ELQV} | t_{ACS} | Chip Enable Access Time | | 15 | | 25 | | 45 | ns |
| 2 | t_{AVAV}^c | t_{ELEH}^c | t_{RC} | Read Cycle Time | 15 | | 25 | | 45 | | ns |
| 3 | t_{AVQV}^d | t_{AVQV}^d | t_{AA} | Address Access Time | | 15 | | 25 | | 45 | ns |
| 4 | | t_{GLQV} | t_{OE} | Output Enable to Data Valid | | 10 | | 12 | | 20 | ns |
| 5 | t_{AXQX}^d | t_{AXQX}^d | t_{OH} | Output Hold after Address Change | 3 | | 3 | | 3 | | ns |
| 6 | | t_{ELQX} | t_{LZ} | Address Change or Chip Enable to Output Active | 3 | | 3 | | 3 | | ns |
| 7 | | t_{EHQZ}^e | t_{HZ} | Address Change or Chip Disable to Output Inactive | | 7 | | 10 | | 15 | ns |
| 8 | | t_{GLQX} | t_{OLZ} | Output Enable to Output Active | 0 | | 0 | | 0 | | ns |
| 9 | | t_{GHQZ}^e | t_{OHZ} | Output Disable to Output Inactive | | 7 | | 10 | | 15 | ns |
| 10 | | t_{ELICCH}^b | t_{PA} | Chip Enable to Power Active | 0 | | 0 | | 0 | | ns |
| 11 | | t_{EHICCL}^b | t_{PS} | Chip Disable to Power Standby | | 15 | | 25 | | 45 | ns |

Note c: \bar{W} must be high during SRAM READ cycles.
 Note d: Device is continuously selected with \bar{E} and \bar{G} both low
 Note e: Measured $\pm 200mV$ from steady state output voltage.
 Note f: HSB must remain high during READ and WRITE cycles.

SRAM READ CYCLE #1: Address Controlled^{c,d,f}



SRAM READ CYCLE #2: \bar{E} and \bar{G} Controlled^{c,f}



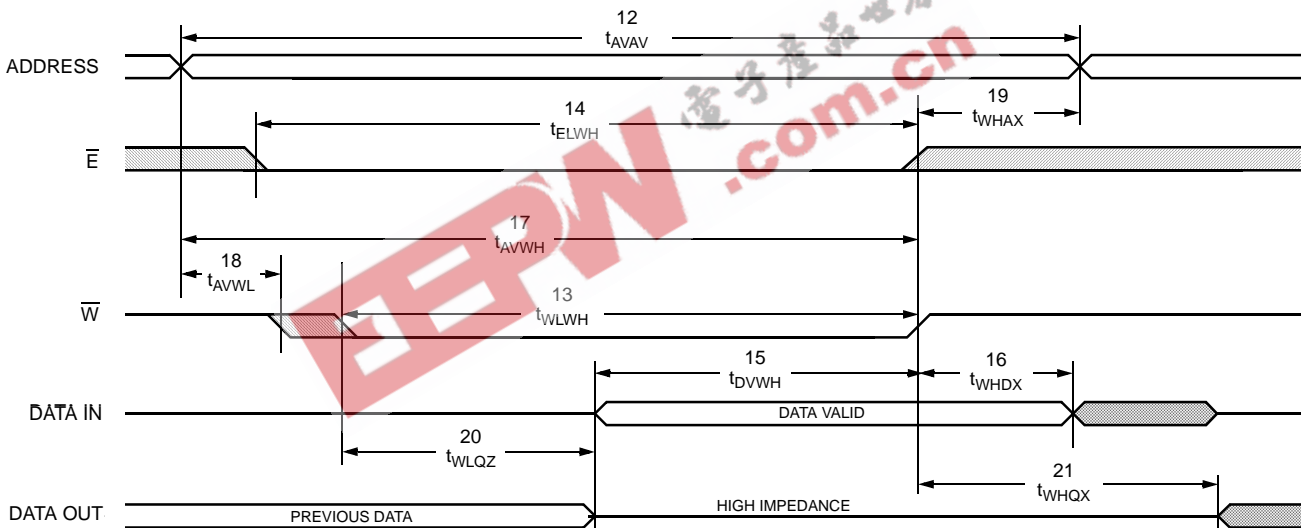
SRAM WRITE CYCLES #1 & #2

| NO. | SYMBOLS | | | PARAMETER | STK14EC8-15 | | STK14EC8-25 | | STK14EC8-45 | | UNITS |
|-----|------------------|------------|----------|----------------------------------|-------------|-----|-------------|-----|-------------|-----|-------|
| | #1 | #2 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 12 | t_{AVAV} | t_{AVAV} | t_{WC} | Write Cycle Time | 15 | | 25 | | 45 | | ns |
| 13 | t_{WLWH} | t_{WLEH} | t_{WP} | Write Pulse Width | 10 | | 20 | | 30 | | ns |
| 14 | t_{ELWH} | t_{ELEH} | t_{CW} | Chip Enable to End of Write | 15 | | 20 | | 30 | | ns |
| 15 | t_{DVWH} | t_{DVEH} | t_{DW} | Data Set-up to End of Write | 5 | | 10 | | 15 | | ns |
| 16 | t_{WHDX} | t_{EHDX} | t_{DH} | Data Hold after End of Write | 0 | | 0 | | 0 | | ns |
| 17 | t_{AVWH} | t_{AVEH} | t_{AW} | Address Set-up to End of Write | 10 | | 20 | | 30 | | ns |
| 18 | t_{AVWL} | t_{AVEL} | t_{AS} | Address Set-up to Start of Write | 0 | | 0 | | 0 | | ns |
| 19 | t_{WHAX} | t_{EHAX} | t_{WR} | Address Hold after End of Write | 0 | | 0 | | 0 | | ns |
| 20 | $t_{WLQZ}^{e,9}$ | | t_{WZ} | Write Enable to Output Disable | | 7 | | 10 | | 15 | ns |
| 21 | t_{WHQX} | | t_{OW} | Output Active after End of Write | 3 | | 3 | | 3 | | ns |

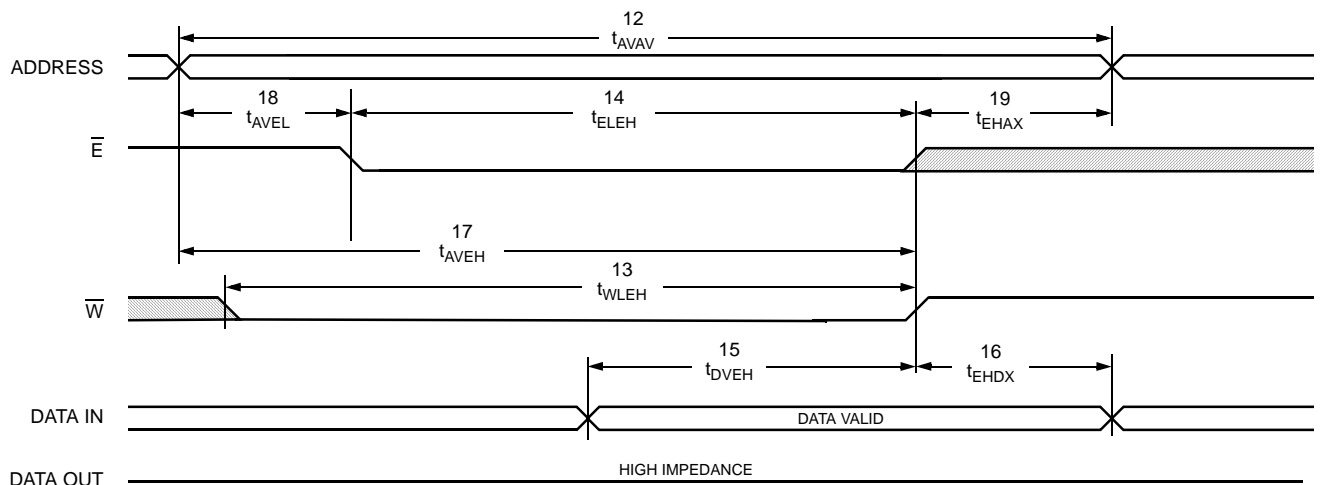
Note g: If \bar{W} is low when \bar{E} goes low, the outputs remain in the high-impedance state.

Note h: \bar{E} or \bar{W} must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: \bar{W} Controlled^{g,h}



SRAM WRITE CYCLE #2: \bar{E} Controlled^{g,h}



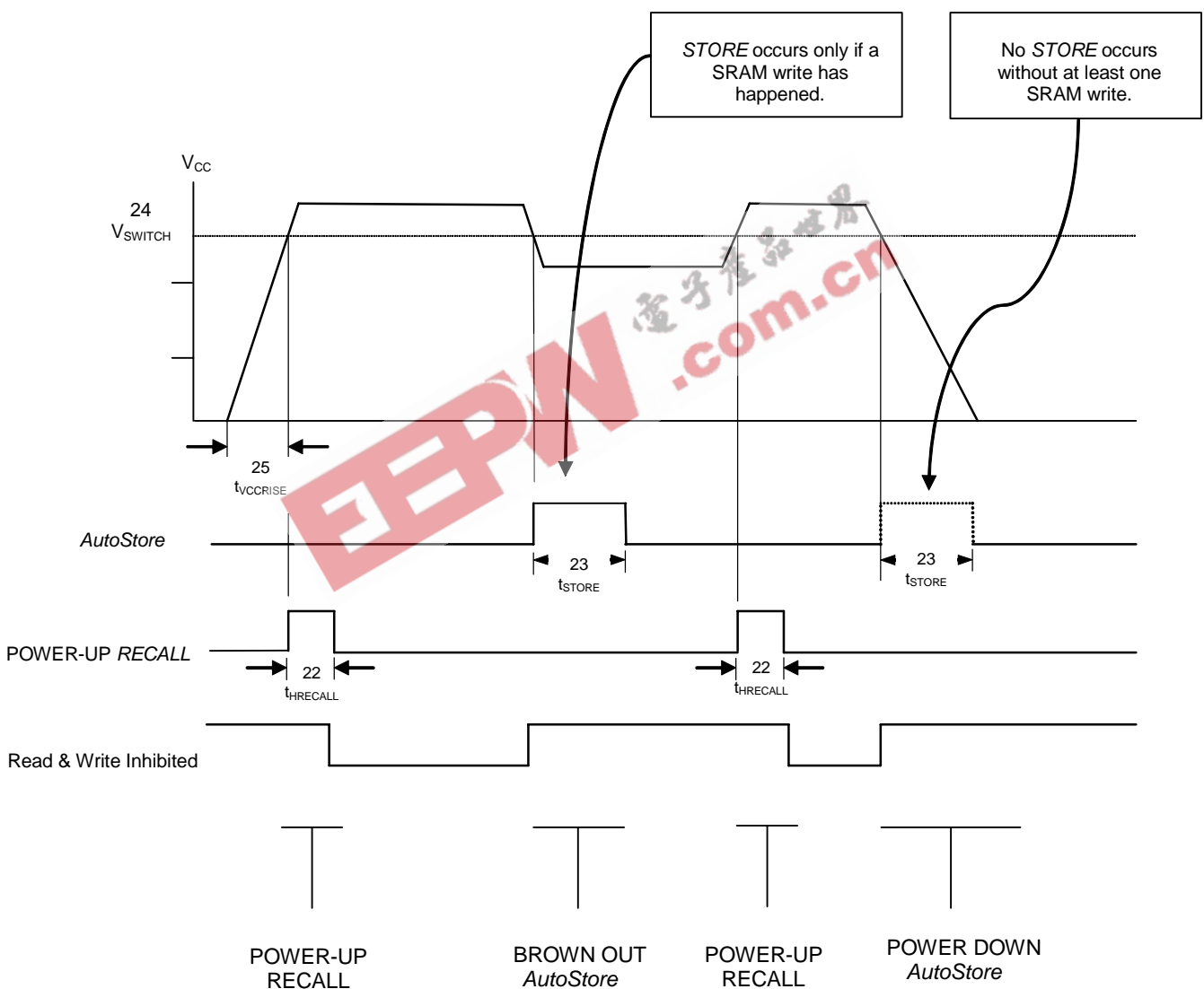
AutoStore™/POWER-UP RECALL

| NO. | SYMBOLS | | PARAMETER | STK14EC8 | | UNITS | NOTES |
|-----|---------------|------------|---------------------------------|----------|------|---------|-------|
| | Standard | Alternate | | MIN | MAX | | |
| 22 | $t_{HRECALL}$ | | Power-up <i>RECALL</i> Duration | | 20 | ms | i |
| 23 | t_{STORE} | t_{HLHZ} | <i>STORE</i> Cycle Duration | | 12.5 | ms | j |
| 24 | V_{SWITCH} | | Low Voltage Trigger Level | | 2.65 | V | |
| 25 | V_{CCRISE} | | V_{CC} Rise Time | 150 | | μ s | |

Note i: $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}

Note j: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place

AutoStore™/POWER-UP RECALL



Note: Read and Write cycles will be ignored during *STORE*, *RECALL* and while V_{CC} is below V_{SWITCH}

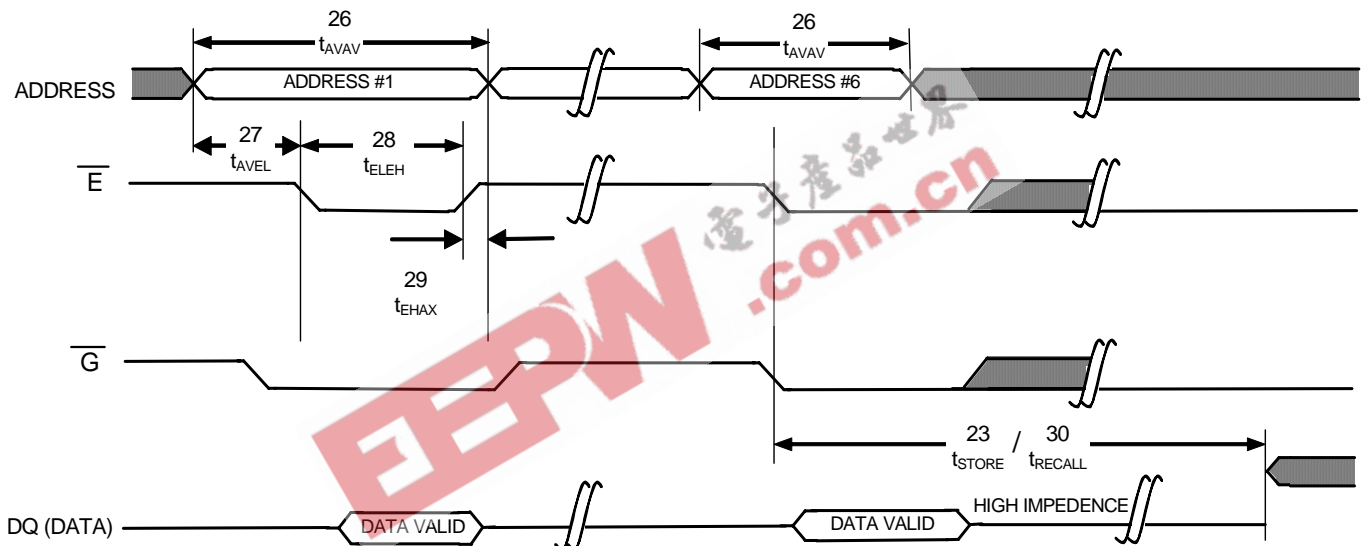
SOFTWARE-CONTROLLED STORE/RECALL CYCLE^{k,l}

| NO. | Symbols | | | PARAMETER | STK14EC8-15 | | STK14EC8-25 | | STK14EC8-45 | | UNITS | NOTES |
|-----|-----------------------------|-----------------------------|-----------|------------------------------------|-------------|-----|-------------|-----|-------------|-----|---------|-------|
| | \bar{E} Cont ^k | \bar{G} Cont ^k | Alternate | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| 26 | t_{AVAV} | t_{AVAV} | t_{RC} | STORE/RECALL Initiation Cycle Time | 15 | | 25 | | 45 | | ns | |
| 27 | t_{AVEL} | t_{AVGL} | t_{AS} | Address Set-up Time | 0 | | 0 | | 0 | | ns | |
| 28 | t_{ELEH} | t_{GLGH} | t_{CW} | Clock Pulse Width | 12 | | 20 | | 30 | | ns | |
| 29 | t_{EHAX} | t_{GHAX} | | Address Hold Time | 1 | | 1 | | 1 | | ns | l |
| 30 | t_{RECALL} | t_{RECALL} | | RECALL Duration | | 150 | | 150 | | 150 | μ s | |

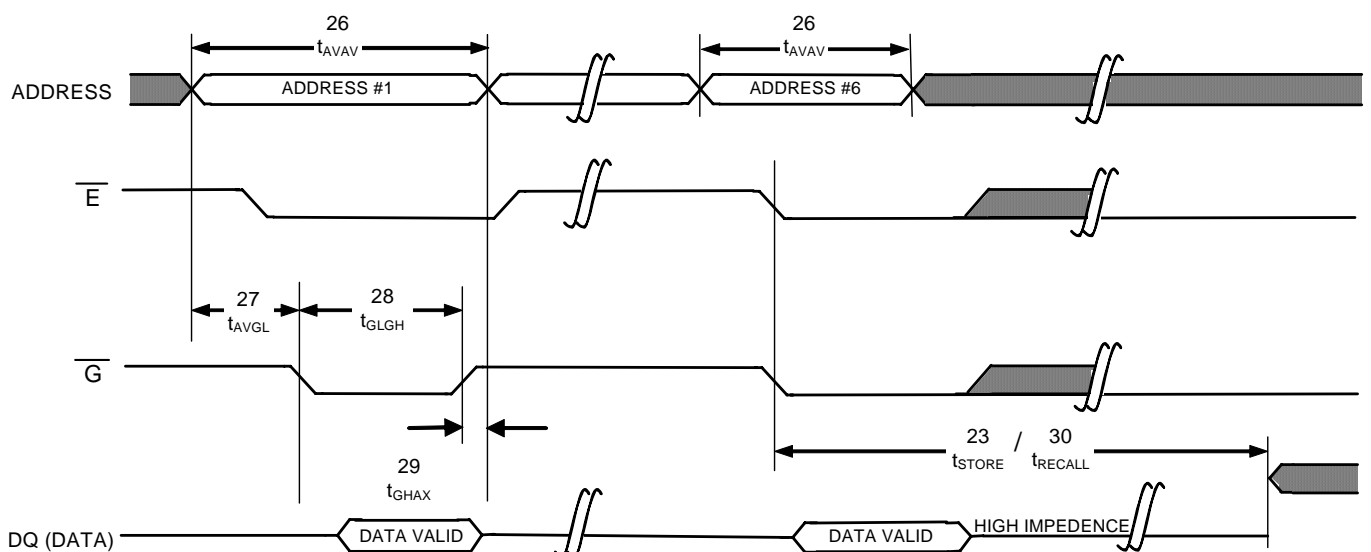
Note k: The software sequence is clocked on the falling edge of \bar{E} controlled READs or \bar{G} controlled READs

Note l: The six consecutive addresses must be read in the order listed in the Software STORE/RECALL Mode Selection Table. \bar{W} must be high during all six consecutive \bar{E} or \bar{G} controlled cycles.

SOFTWARE STORE/RECALL CYCLE: \bar{E} CONTROLLED^l



SOFTWARE STORE/RECALL CYCLE: \bar{G} CONTROLLED^l

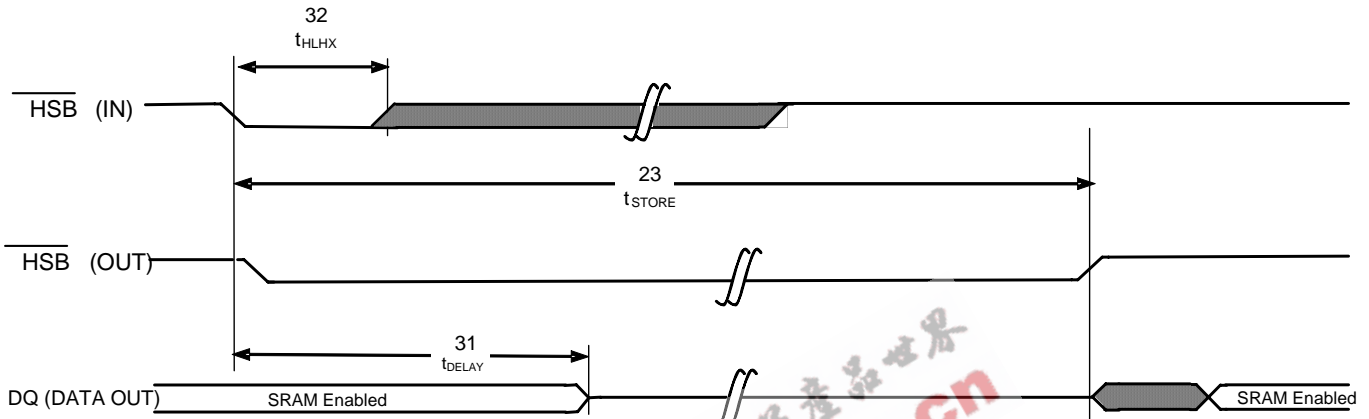


HARDWARE STORE CYCLE

| | SYMBOLS | | PARAMETER | STK14EC8 | | UNITS | NOTES |
|----|-------------|------------|---------------------------------|----------|-----|---------|-------|
| | Standard | Alternate | | MIN | MAX | | |
| 31 | t_{DELAY} | t_{HLQZ} | Hardware STORE to SRAM Disabled | .05 | 70 | μ s | m |
| 32 | t_{HLHX} | | Hardware STORE Pulse Width | 15 | | ns | |

Note m: On a hardware STORE initiation, SRAM operation continues to be enabled for time t_{DELAY} to allow read/write cycles to complete

HARDWARE STORE CYCLE

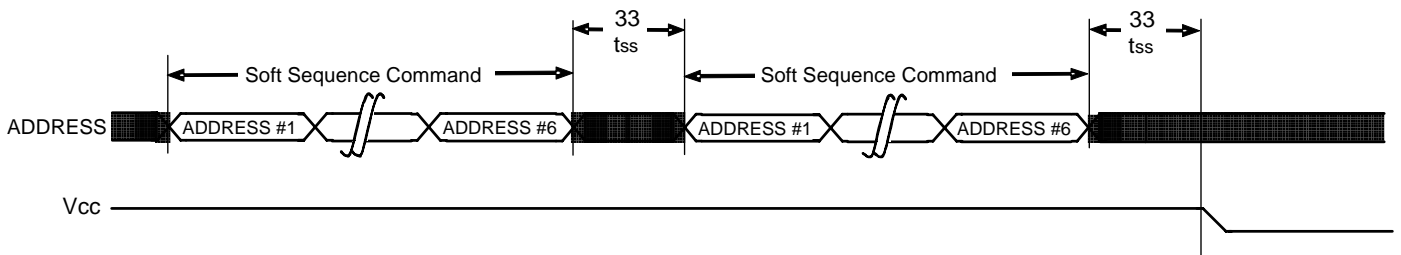


Soft Sequence Commands

| NO. | SYMBOLS | | PARAMETER | STK14EC8 | | UNITS | NOTES |
|-----|----------|--|-------------------------------|----------|-----|---------|-------|
| | Standard | | | MIN | MAX | | |
| 33 | t_{SS} | | Soft Sequence Processing Time | | 70 | μ s | n,o |

Note n: This is the amount of time that it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.

Note o: Commands like Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.



MODE SELECTION

| \bar{E} | \bar{W} | \bar{G} | A ₁₈ -A ₀ | Mode | I/O | Power | Notes |
|-----------|-----------|-----------|--|---|--|----------------------------|-------|
| H | X | X | X | Not Selected | Output High Z | Standby | |
| L | H | L | X | Read SRAM | Output Data | Active | |
| L | L | X | X | Write SRAM | Input Data | Active | |
| L | H | L | 0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08B45 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable | Output Data Output Data Output Data Output Data Output Data Output Data | Active | q,r,s |
| L | H | L | 0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04B46 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable | Output Data Output Data Output Data Output Data Output Data Output Data | Active | q,r,s |
| L | H | L | 0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08FC0 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store | Output Data Output Data Output Data Output Data Output Data Output High Z | Active I _{CC2} | q,r,s |
| L | H | L | 0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04C63 | Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall | Output Data Output Data Output Data Output Data Output Data Output High Z | Active | q,r,s |

Note q: The six consecutive addresses must be in the order listed. \bar{W} must be high during all six consecutive cycles to enable a nonvolatile cycle.

Note r: While there are 19 addresses on the STK14EC8, only the lower 16 are used to control software modes

Note s: I/O state depends on the state of \bar{G} . The I/O table shown assumes \bar{G} low

nvSRAM OPERATION

nvSRAM

The STK14EC8 nvSRAM is made up of two functional components paired in the same physical cell. These are the SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates like a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The STK14EC8 supports unlimited read and writes like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

SRAM READ

The STK14EC8 performs a READ cycle whenever \bar{E} and \bar{G} are low while \bar{W} and HSB are high. The address specified on pins A_{0-18} determine which of the 524,288 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by \bar{E} and \bar{G} , the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until \bar{E} or \bar{G} is brought high, or \bar{W} and HSB is brought low.

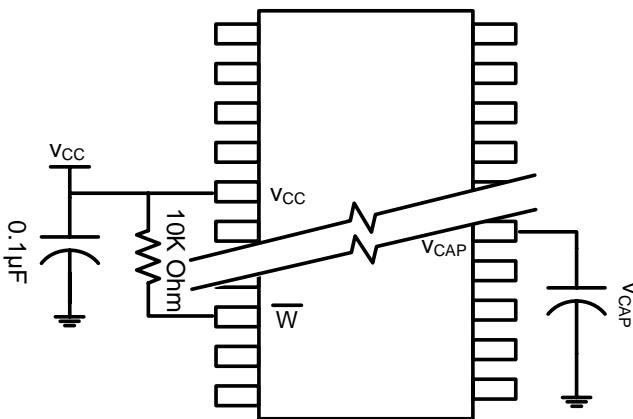


Figure 3: AutoStore Mode

SRAM WRITE

A WRITE cycle is performed whenever \bar{E} and \bar{W} are low and HSB is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either \bar{E} or \bar{W} goes high at the end of the cycle. The data on the common I/O pins DQ0-7 will be written into memory if it is valid t_{DVWH} before the end of a \bar{W} controlled WRITE or t_{DVEH} before the end of an \bar{E} controlled WRITE.

It is recommended that \bar{G} be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If \bar{G} is left low, internal circuitry will turn off the output buffers t_{WLQZ} after \bar{W} goes low.

AutoStore OPERATION

The STK14EC8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store (activated by HSB), Software Store (activated by an address sequence), and AutoStore (on power down).

AutoStore operation is a unique feature of Simtek Quantum Trap technology that is enabled by default on the STK14EC8.

During normal operation, the device will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CC} . A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 3 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. The voltage on the V_{CAP} pin is driven to 3.6V by a regulator internal to the chip. Refer to the DC CHARACTERISTICS table for the size of the capacitor. A pull up should be placed on \bar{W} to hold it inactive during power up. This pull-up is only effective if the \bar{W} signal is tri-state during power up. Many MPU's will tri-state their controls on power up. This should be verified when using the pullup. When the nvSRAM comes out on power-on-recall, the MPU must be active or the \bar{W} held inactive until the MPU comes out of reset.

To reduce unneeded nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The HSB signal can be monitored by the system to detect an AutoStore cycle is in progress.

HARDWARE STORE (HSB) OPERATION

The STK14EC8 provides the $\overline{\text{HSB}}$ pin for controlling and acknowledging the STORE operations. The $\overline{\text{HSB}}$ pin can be used to request a hardware STORE cycle. When the $\overline{\text{HSB}}$ pin is driven low, the STK14EC8 will conditionally initiate a STORE operation after t_{DELAY} . An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{\text{HSB}}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations that are in progress when $\overline{\text{HSB}}$ is driven low or when V_{CC} falls below V_{switch} are given time to complete before the STORE operation is initiated. After AUTOSTORE or $\overline{\text{HSB}}$ goes low, the STK14EC8 will continue to allow SRAM operations for t_{DELAY} . During t_{DELAY} , multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{\text{HSB}}$ is pulled low, it will be allowed a time, t_{DELAY} , to complete. However, any SRAM WRITE cycles requested after $\overline{\text{HSB}}$ goes low will be inhibited until HSB returns high.

If $\overline{\text{HSB}}$ is not used, it should be left unconnected.

HARDWARE RECALL (POWER-UP)

During power up or after any low-power condition ($V_{\text{CC}} < V_{\text{SWITCH}}$), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle will automatically be initiated and will take t_{HRECALL} to complete.

SOFTWARE STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK14EC8 software STORE cycle is initiated by executing sequential $\overline{\text{E}}$ controlled or $\overline{\text{G}}$ controlled

READ cycles from six specific address locations in exact order. During the STORE cycle, previous data is erased and then the new data is programmed into the nonvolatile elements. Once a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed.

To initiate the software STORE cycle, the following READ sequence must be performed:

- | | | | |
|---|--------------|--------|----------------------|
| 1 | Read Address | 0x4E38 | Valid READ |
| 2 | Read Address | 0xB1C7 | Valid READ |
| 3 | Read Address | 0x83E0 | Valid READ |
| 4 | Read Address | 0x7C1F | Valid READ |
| 5 | Read Address | 0x703F | Valid READ |
| 6 | Read Address | 0x8FC0 | Initiate STORE Cycle |

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence and that $\overline{\text{G}}$ is active. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{\text{E}}$ controlled or $\overline{\text{G}}$ controlled READ operations must be performed:

- | | | | |
|---|--------------|--------|-----------------------|
| 1 | Read Address | 0x4E38 | Valid READ |
| 2 | Read Address | 0xB1C7 | Valid READ |
| 3 | Read Address | 0x83E0 | Valid READ |
| 4 | Read Address | 0x7C1F | Valid READ |
| 5 | Read Address | 0x703F | Valid READ |
| 6 | Read Address | 0x4C63 | Initiate RECALL Cycle |

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM will once again be ready for READ or WRITE operations. The RECALL operation in no way alters the data in the nonvolatile storage elements. Care must be taken so the controlling falling edge is glitch and ring free so as not to double clock the read address.

DATA PROTECTION

The STK14EC8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low-voltage condition is detected when $V_{CC} < V_{SWITCH}$.

If the STK14EC8 is in a WRITE mode (both \overline{E} and \overline{W} low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on \overline{E} or \overline{W} is detected. This protects against inadvertent writes during power up or brown out conditions.

NOISE CONSIDERATIONS

The STK14EC8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 μF connected between V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals will reduce circuit noise.

BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in this nvSRAM product are delivered from Simtek with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (i.e., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (autostore enabled, etc.). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently

(program bugs, incoming inspection routines, etc.).

- The autostore enabled/disabled feature will reset to "autostore enabled" on every power down event captured by the nvSRAM. The application firmware should disable autostore on each reset sequence that this behavior is desired.
- The V_{cap} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the nvSRAM internal algorithm calculates V_{cap} charge time based on this max V_{cap} value. Customers that want to use a larger V_{cap} value to make sure there is extra store charge and store time should discuss their V_{cap} size selection with Simtek to understand any impact on the V_{cap} voltage level at the end of a t_{RECALL} period.

LOW AVERAGE ACTIVE POWER

CMOS technology provides the STK14EC8 with the benefit of power supply current that scales with cycle time. Less current will be drawn as the memory cycle time becomes longer than 50 ns. Figure 4 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, $V_{CC}=3.6\text{V}$, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14EC8 depends on the following items:

- 1 The duty cycle of chip enable
- 2 The overall cycle rate for operations
- 3 The ratio of READs to WRITEs
- 4 The operating temperature
- 5 The V_{CC} Level
- 6 I/O Loading

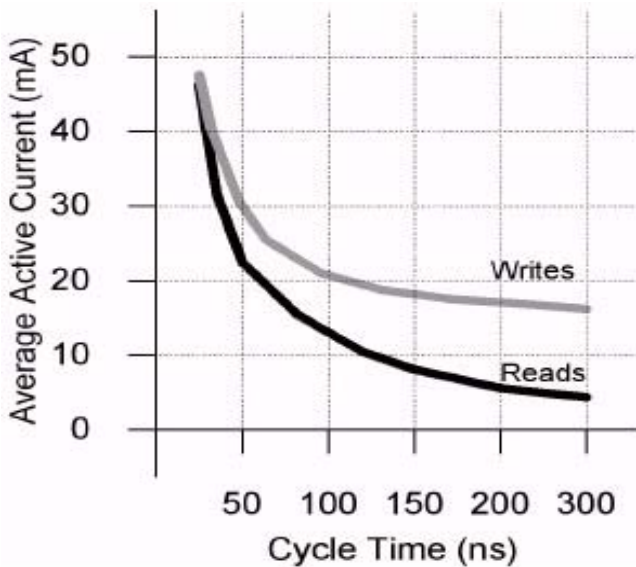


Figure 4 - Current vs Cycle Time

PREVENTING AUTOSTORE

The AutoStore function can be disabled by initiating an *AutoStore Disable* sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the *AutoStore Disable* sequence, the following sequence of \bar{E} controlled or \bar{G} controlled READ operations must be performed:

- 1 Read Address 0x4E38 Valid READ
- 2 Read Address 0xB1C7 Valid READ
- 3 Read Address 0x83E0 Valid READ
- 4 Read Address 0x7C1F Valid READ
- 5 Read Address 0x703F Valid READ
- 6 Read Address 0x8B45 AutoStore Disable

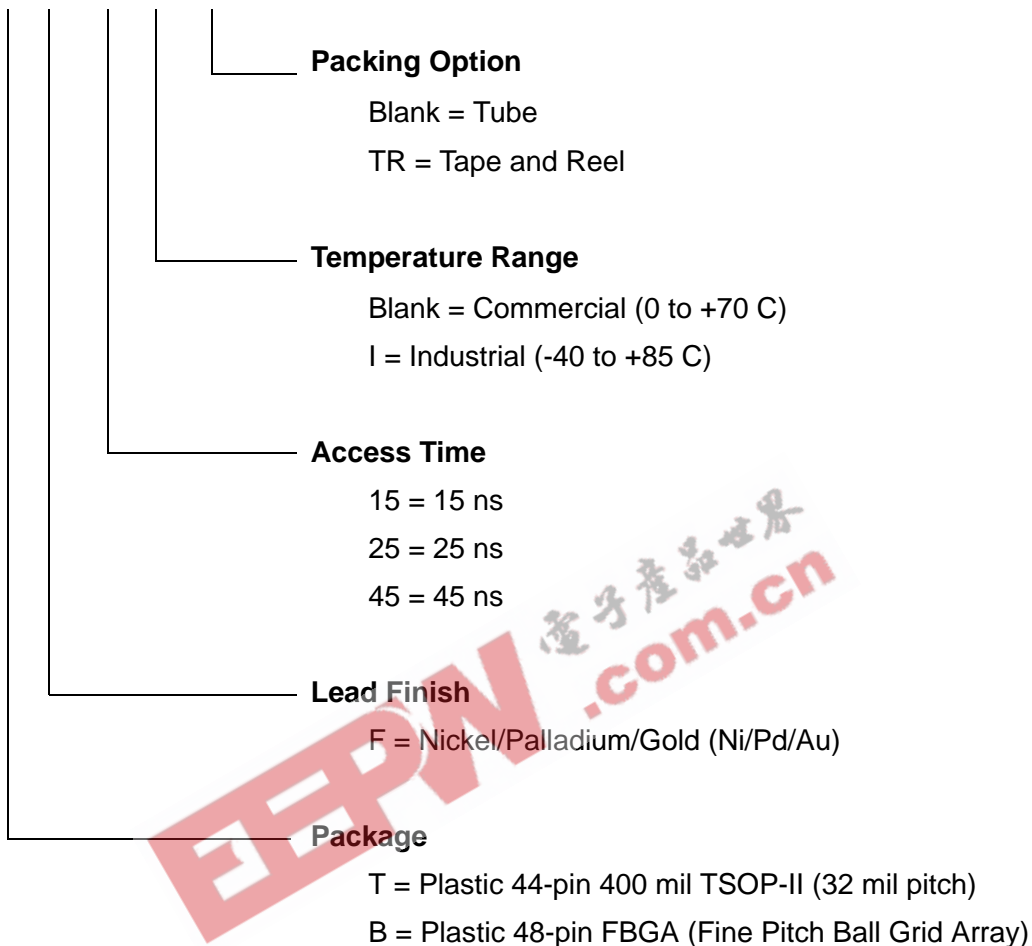
The AutoStore can be re-enabled by initiating an *AutoStore Enable* sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Enable* sequence, the following sequence of \bar{E} controlled or \bar{G} controlled READ operations must be performed:

- 1 Read Address 0x4E38 Valid READ
- 2 Read Address 0xB1C7 Valid READ
- 3 Read Address 0x83E0 Valid READ
- 4 Read Address 0x7C1F Valid READ
- 5 Read Address 0x703F Valid READ
- 6 Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) needs to be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled, but best design practice is to set the enable or disable state during each power-up sequence and not depend on this factory default condition. Simtek recommends users configure the part completely for the specific application.

ORDERING INFORMATION

STK14EC8-T F 45 I TR

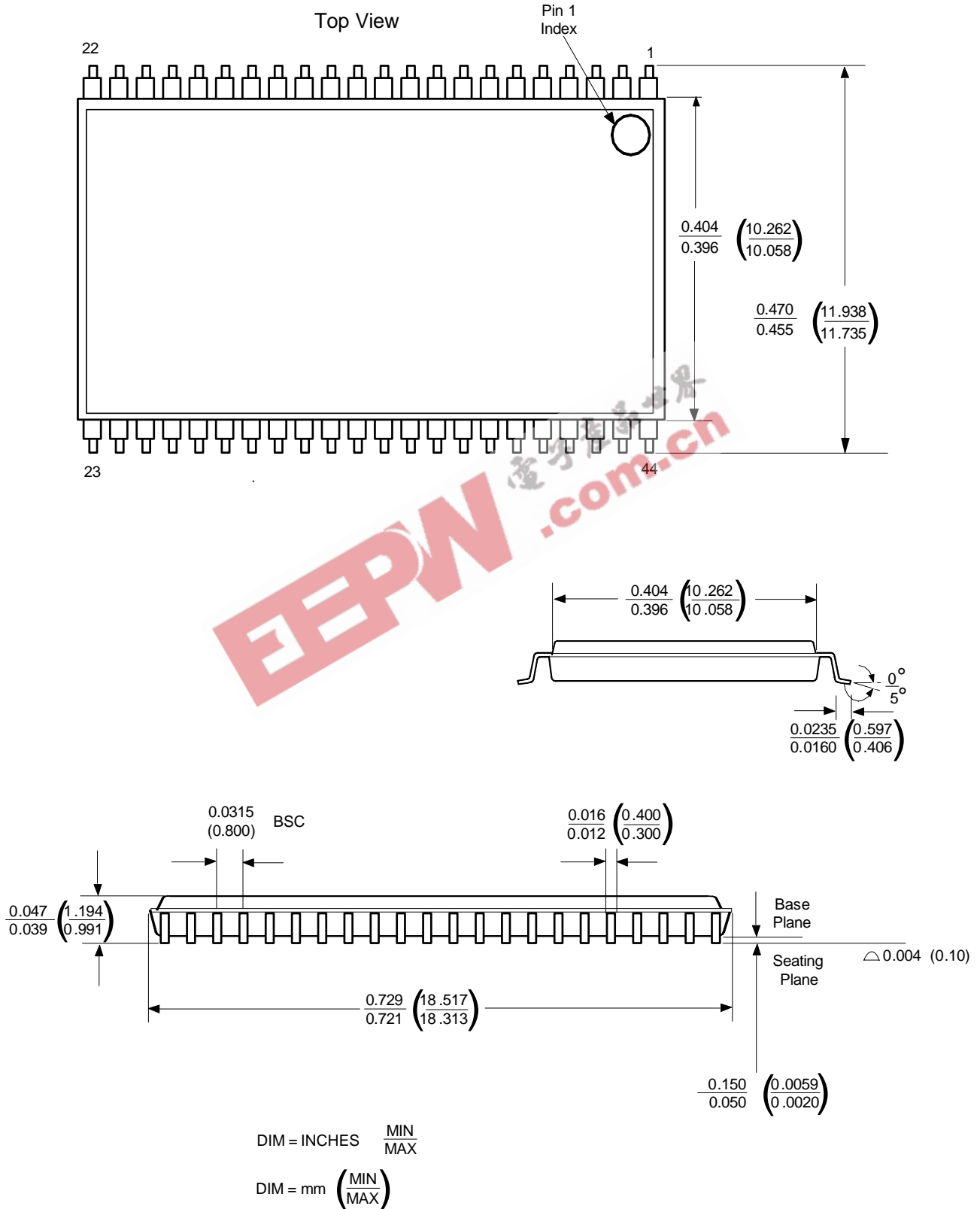


Ordering Codes

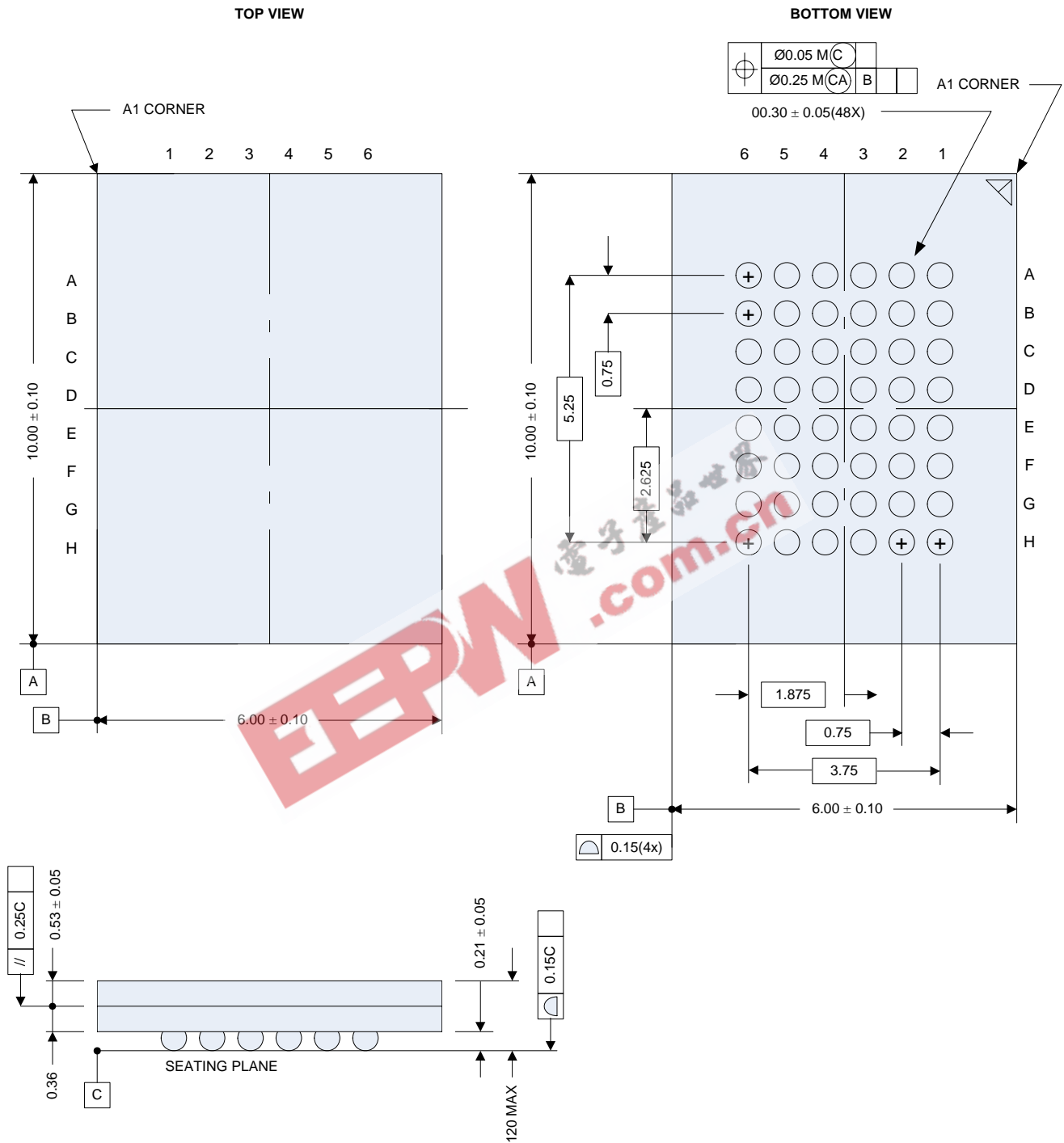
| Part Number | Description | Access Times | Temperature |
|------------------|---------------------------------------|-------------------|-------------|
| STK14EC8-TF15 | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 15 ns access time | Commercial |
| STK14EC8-TF25 | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 25 ns access time | Commercial |
| STK14EC8-TF45 | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 45 ns access time | Commercial |
| STK14EC8-TF15TR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 15 ns access time | Commercial |
| STK14EC8-TF25TR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 25 ns access time | Commercial |
| STK14EC8-TF45TR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 45 ns access time | Commercial |
| STK14EC8-TF15I | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 15 ns access time | Industrial |
| STK14EC8-TF25I | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 25 ns access time | Industrial |
| STK14EC8-TF45I | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 45 ns access time | Industrial |
| STK14EC8-TF15ITR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 15 ns access time | Industrial |
| STK14EC8-TF25ITR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 25 ns access time | Industrial |
| STK14EC8-TF45ITR | 3V 512Kx8 AutoStore nvSRAM TSOP44-400 | 45 ns access time | Industrial |
| STK14EC8-BF15 | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 15 ns access time | Commercial |
| STK14EC8-BF25 | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 25 ns access time | Commercial |
| STK14EC8-BF45 | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 45 ns access time | Commercial |
| STK14EC8-BF15TR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 15 ns access time | Commercial |
| STK14EC8-BF25TR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 25 ns access time | Commercial |
| STK14EC8-BF45TR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 45 ns access time | Commercial |
| STK14EC8-BF15I | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 15 ns access time | Industrial |
| STK14EC8-BF25I | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 25 ns access time | Industrial |
| STK14EC8-BF45I | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 45 ns access time | Industrial |
| STK14EC8-BF15ITR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 15 ns access time | Industrial |
| STK14EC8-BF25ITR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 25 ns access time | Industrial |
| STK14EC8-BF45ITR | 3V 512Kx8 AutoStore nvSRAM FBGA48 | 45 ns access time | Industrial |

PACKAGE DIAGRAMS

44-Pin TSOPII



48-Ball FBGA



Document Revision History

| Rev | Date | Change |
|-----|--------------|---|
| 1.0 | April 2007 | <p>Moved to Preliminary from Advance Information</p> <ul style="list-style-type: none"> – made clear that nominal supply is 3.3V, not 3.0V (range 2.7V to 3.6V) – modified language on pin description of HSB and NC. – changed ISB from 1mA to 2mA. – changed Icc3 from 8mA to 13mA – clarified description language of Figure 3 – clarified description language of Software Recall – clarified description language of Preventing Autostore – corrected typo on Industrial temp range: -45 to -40 |
| 1.1 | January 2008 | <p>Made the following changes to the document</p> <ul style="list-style-type: none"> – page 1: revised block diagram – page 2: added new 48 FBGA information and added pin descriptions for pins \bar{E} and \bar{W}. – page 3: added thermal characteristics. In the DC Characteristics table, revised values for I_{CC2}, I_{CC4}, I_{SB}, V_{IH}, V_{CC}, and V_{CAP}; and changed Industrial Max Value of V_{CAP} to 180 and revised V_{CAP} notes. Added "(except HSB)" to notes for Output Logic "1" Voltage. – page 5: in SRAM Read Cycles #1 & #2 table, revised parameter description for t_{ELQX} and t_{EHQZ} and changed Symbol #2 to t_{ELEH} for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram and changed title to add G controlled. – page 7: in AutoStore/Power-Up Recall table, changed max value for #23 (t_{STORE}) to 12.5. – page 8: in Software-Controlled Store/Recall Cycle table, revised values for t_{RECALL}; revised the notes below the Software-Controlled Store/Recall Cycle diagram. – page 10: in Mode Selection table, changed column to A₁₈-A₀; in the values in this column, added a zero after each instance of "0x"; changed AutoStore Enable value to 0x04B46. – page 11: in Auto-Store Operation, deleted line about V_{CAP} pin being driven to 5V by a charge pump internal to the chip. Also, added Stefan's revised text (italics show revision): "Refer to the DC CHARACTERISTICS table for the size of the capacitor." – page 12: under Hardware Store (\bar{HSB}) Operation, revised first paragraph to read "The HSB pin has a very resistive pullup..." – page 13: added best practices section. – page 15: in Ordering Information, Lead Finish, replaced "Sn (Matte Tin) RoHS Compliant" with "Nickel/Palladium/Gold (Ni/Pd/Au)";, added "B = Plastic 48-pin FBGA (Fine Pitch Ball Grid Array)" to Finish. – page 16: in Ordering Codes, added ordering information for 48 FBGA and added access times column. |

SIMTEK STK14EC8 Datasheet, January 2008

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