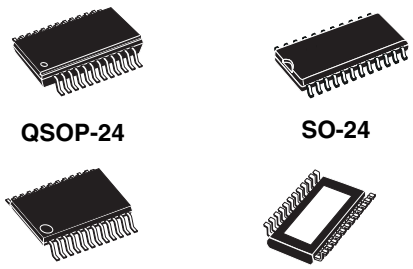
STP16DP05

Low voltage 16-bit constant current LED sink driver with outputs error detection

Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial Data IN/Parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM, 200 V MM



QSOP-24 | SO-24 | TSSOP24 | TSSOP24 (exposed pad)

Description

The STP16DP05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bitD-type storage register. In the output stage, sixteen regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs.

The STP16DP05 features open and short LED detections on the outputs.The STP16DP05 is backward compatible with STP16C/L596.The detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to V_O or open line.

The data detection results are loaded in the shift register and shifted out via the serial line output.

The detection functionality is implemented without increasing the pin count number, through a secondary function of the output enable and latch pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave from detection mode. Through an external resistor, users can adjust the STP16DP05 output current, controlling in this way the light intensity of LEDs, in addition, user can adjust LED's brightness intensity from 0 % to 100 % via $\overline{OE}$/DM2 pin.

The STP16DP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is well useful for applications that interface any 3.3V micro. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Table 1. Device summary

Order codes	Package	Packaging
STP16DP05MTR	SO-24 (tape and reel)	1000 parts per reel
STP16DP05TTR	TSSOP24 (tape and reel)	2500 parts per reel
STP16DP05XTTR	TSSOP24 exposed pad (tape and reel)	2500 parts per reel
STP16DP05PTR	QSOP-24	2500 parts per reel

Contents

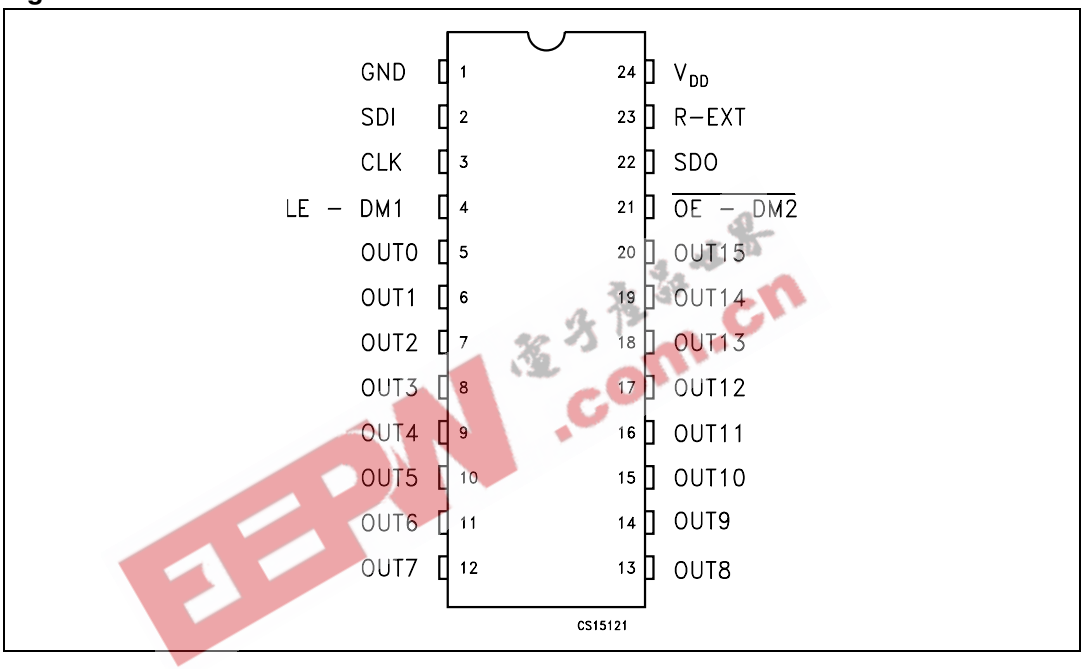
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	±1.5 %	±5 %	20 to 100 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1. Pin connection



Note: The exposed pad is electrically not connected

Table 3. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE-DM1	Latch input terminal - Detect mode 1 (see operation principle)
5-20	OUT 0-15	Output terminal
21	$\overline{\text{OE}}$-DM2	Input terminal of output enable (active low) - Detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJC}	Thermal resistance junction-case	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24(1) Exposed Pad	37.5	°C/W
		QSOP-24	72	°C/W

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	5		100	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
V_{IL}	Input voltage		-0.3		$0.3V_{DD}$	V
t_{wLAT}	LE\DM1 pulse width	V_{DD} = 3.0 V to 5.0 V	20			ns
t_{wCLK}	CLK pulse width		20			ns
t_{wEN}	$\overline{OE}$\DM2 pulse width		200			ns
$t_{SETUP(D)}$	Setup time for DATA		20			ns
$t_{HOLD(D)}$	Hold time for DATA		15			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

Table 7. Electrical characteristics
(V_{DD} = 3.3 V to 5 V, T = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		0.7V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20 V			10	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1 mA	V_{OH} -V_{DD} = -0.4 V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 3.9 kΩ	4.25	5	5.75	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 970 Ω	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 190 Ω	96	100	104	
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.3 VR_{EXT} = 3.9 kΩ		± 5	± 8	%
ΔI_{OL2}		V_O = 0.3 VR_{EXT} = 970 Ω		± 1.5	± 3	
ΔI_{OL3}		V_O = 1.3 VR_{EXT} =190 Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	KΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	KΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = 970 OUT 0 to 15 = OFF		4	5	mA
$I_{DD(OFF2)}$		R_{EXT} = 240 OUT 0 to 15 = OFF		11.2	13.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 970 OUT 0 to 15 = ON		4.5	5	
$I_{DD(ON2)}$		R_{EXT} = 240 OUT 0 to 15 = ON		11.7	13.5	
Thermal	Thermal protection (1)			170		°C

1. Guaranteed by desing (not tested)
The thermal protection switches OFF only the outputs current

Table 8. Switching characteristics (V_{DD} = 5 V, T = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions			Min	Typ	Max	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUTn}$, LE\DM1 = H, $\overline{OE}$\DM2 = L	V_{DD} = 3.3 V V_{IL} = GND I_O = 20 mA R_{EXT} = 1 KΩ	V_{IH} = V_{DD} C_L = 10 pF V_L = 3.0 V R_L = 60 Ω	V_{DD} = 3.3 V		70	105	ns
				V_{DD} = 5 V		45	65	
t_{PLH2}	Propagation delay time, LE\DM1 -$\overline{OUTn}$, $\overline{OE}$\DM2 = L			V_{DD} = 3.3 V		61	90	ns
				V_{DD} = 5 V		41	60	
t_{PLH3}	Propagation delay time, $\overline{OE}$\DM2-$\overline{OUTn}$, LE\DM1 = H			V_{DD} = 3.3 V		69	105	ns
				V_{DD} = 5 V		50	70	
t_{PLH}	Propagation delay time, CLK-SDO			V_{DD} = 3.3 V		14	20	ns
				V_{DD} = 5 V		8	12	
t_{PHL1}	Propagation delay time, CLK-$\overline{OUTn}$, LE\DM1 = H, $\overline{OE}$\DM2 = L			V_{DD} = 3.3 V		34	50	ns
				V_{DD} = 5 V		23	35	
t_{PHL2}	Propagation delay time, LE\DM1 -$\overline{OUTn}$, $\overline{OE}$\DM2 = L			V_{DD} = 3.3 V		27	40	ns
				V_{DD} = 5 V		22	32	
t_{PHL3}	Propagation delay time, $\overline{OE}$\DM2-$\overline{OUTn}$, LE\DM1 = H			V_{DD} = 3.3 V		23	35	ns
				V_{DD} = 5 V		20	30	
t_{PHL}	Propagation delay time, CLK-SDO			V_{DD} = 3.3 V		15	25	ns
				V_{DD} = 5 V		9	15	
t_{ON}	Output rise time 10~90% of voltage waveform			V_{DD} = 3.3 V		42	65	ns
				V_{DD} = 5 V		35	55	
t_{OFF}	Output fall time 90~10% of voltage waveform			V_{DD} = 3.3 V		10	16	ns
				V_{DD} = 5 V		9	14	
t_r	CLK rise time (1)						5000	ns
t_f	CLK fall time (1)						5000	ns

1. In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2. $\overline{\text{OE}}$\DM2 terminal

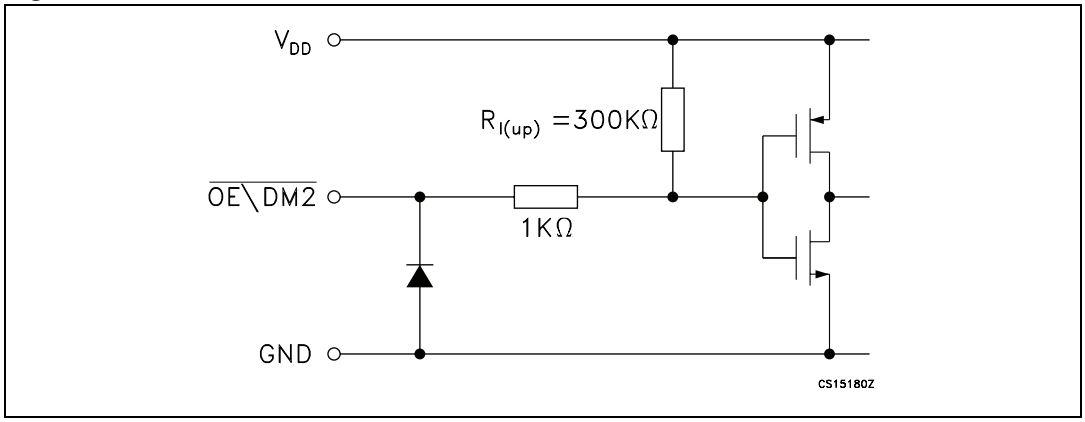


Figure 3. LE\DM1 terminal

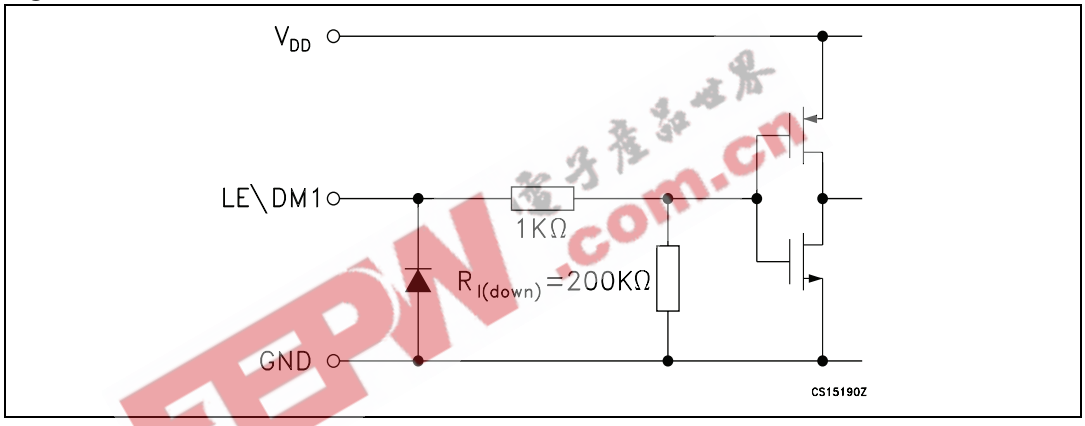


Figure 4. CLK, SDI terminal

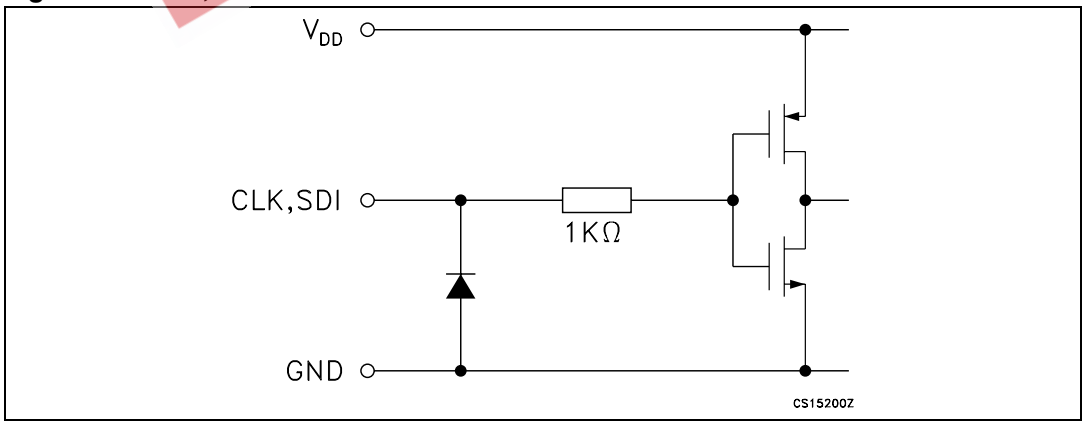


Figure 5. SDO terminal

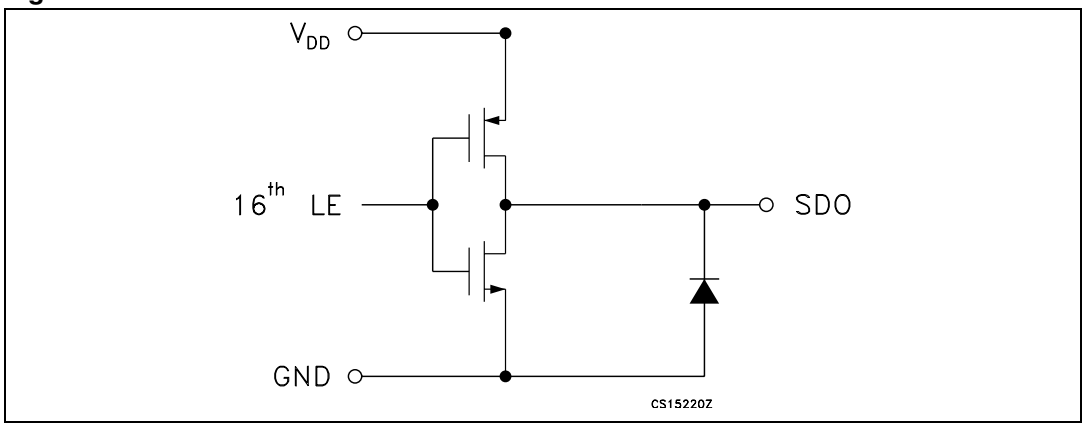
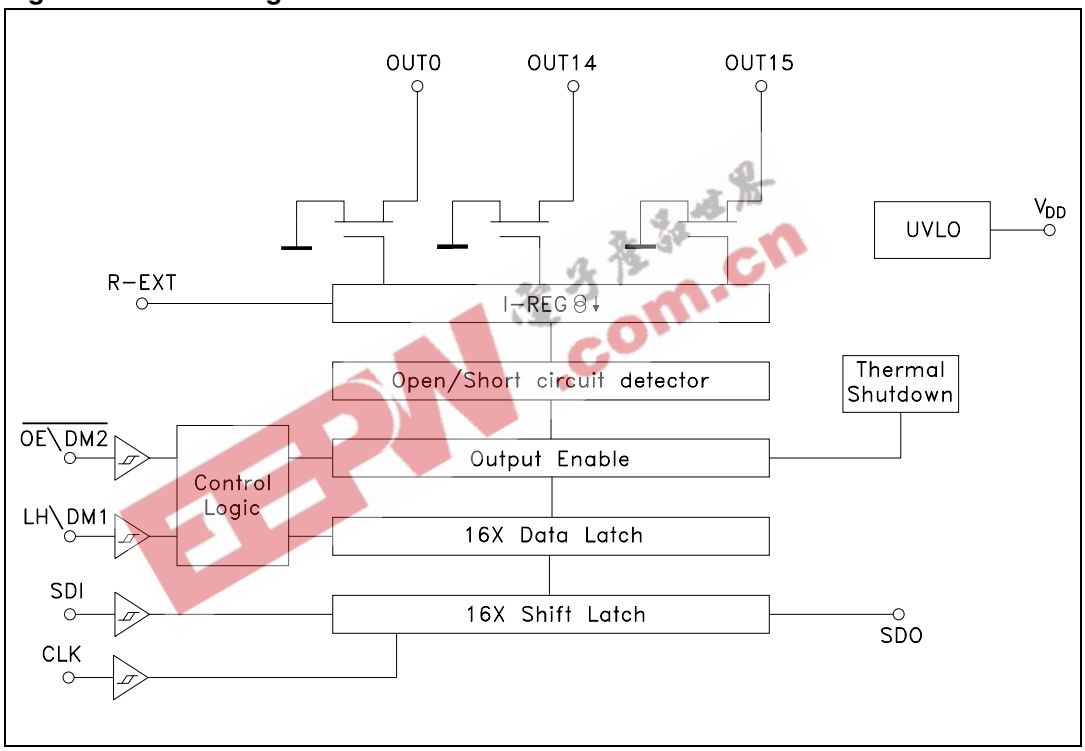


Figure 6. Block diagram



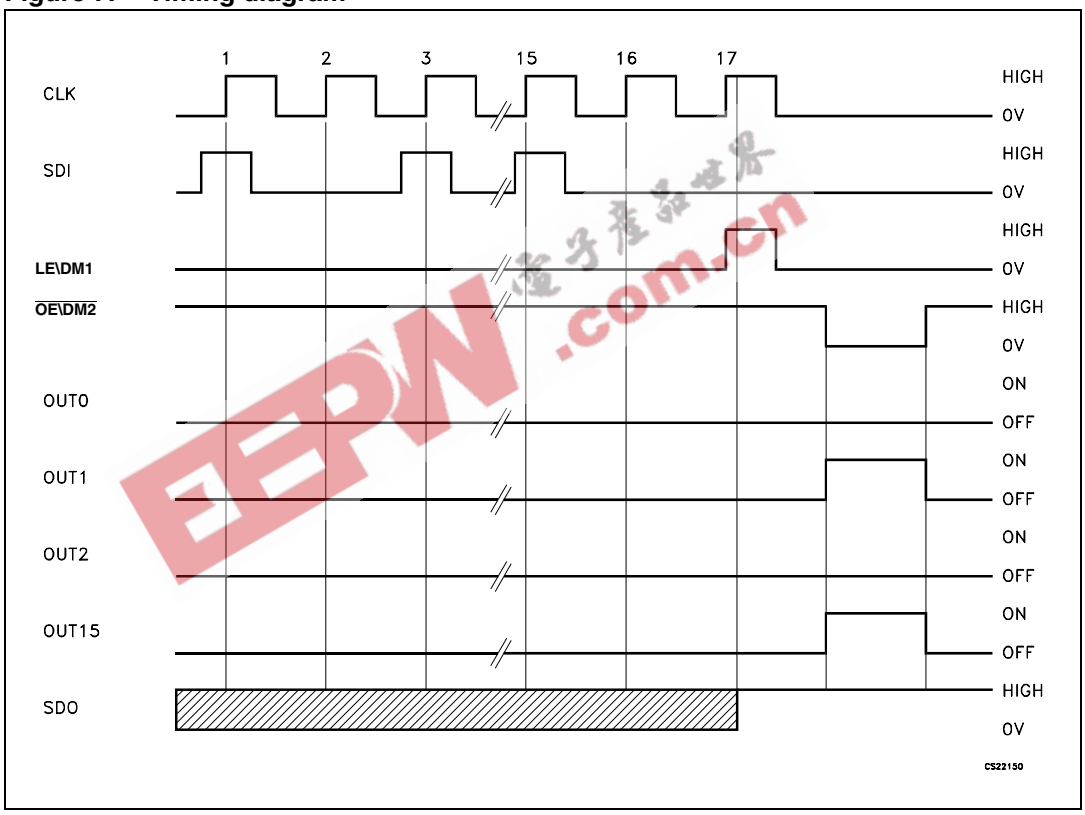
5 Timing diagrams

Table 9. Truth table

CLOCK	LE\DM1	$\overline{OE}$\DM2	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
⎍	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
⎍	L	L	Dn + 1	No change	Dn - 14
⎍	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎏	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎏	X	H	Dn + 3	OFF	Dn - 13

Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L

Figure 7. Timing diagram



Note: The latches circuit holds data when the LE\DM1 terminal is Low.

1. *When LE\DM1 terminal is at High level, latch circuit hold the data it passes from the input to the output.*
2. *When $\overline{OE}$\DM2 terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.*
3. *When $\overline{OE}$\DM2 terminal is at High level, it switches off all the data on the output terminal.*

Figure 8. Clock, serial-in, serial-out

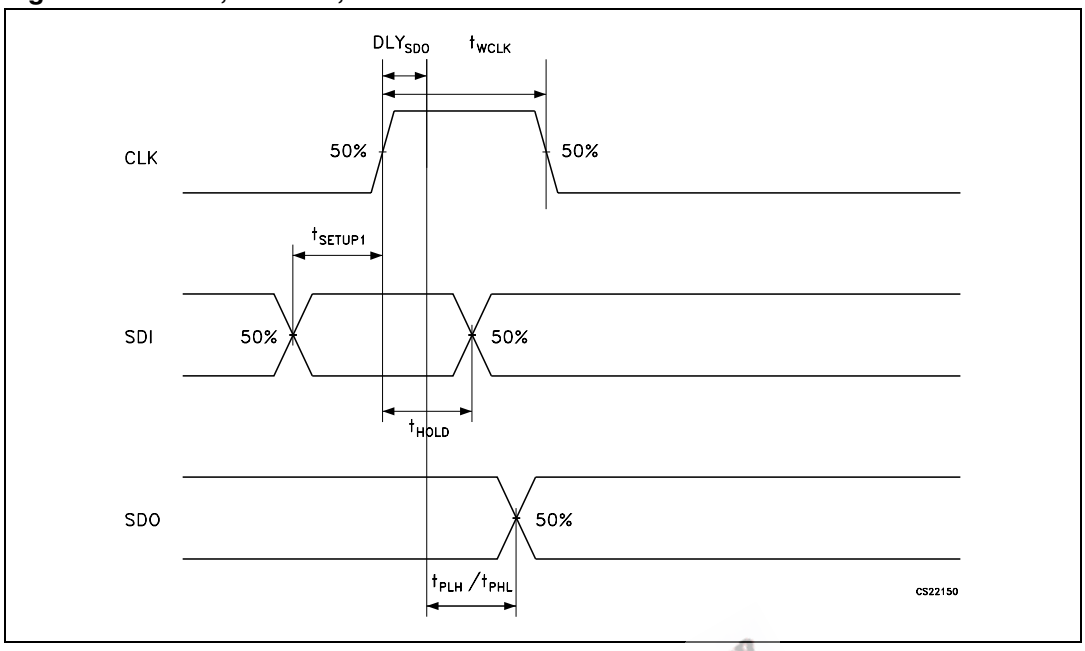


Figure 9. Clock, serial-in, latch, enable, outputs

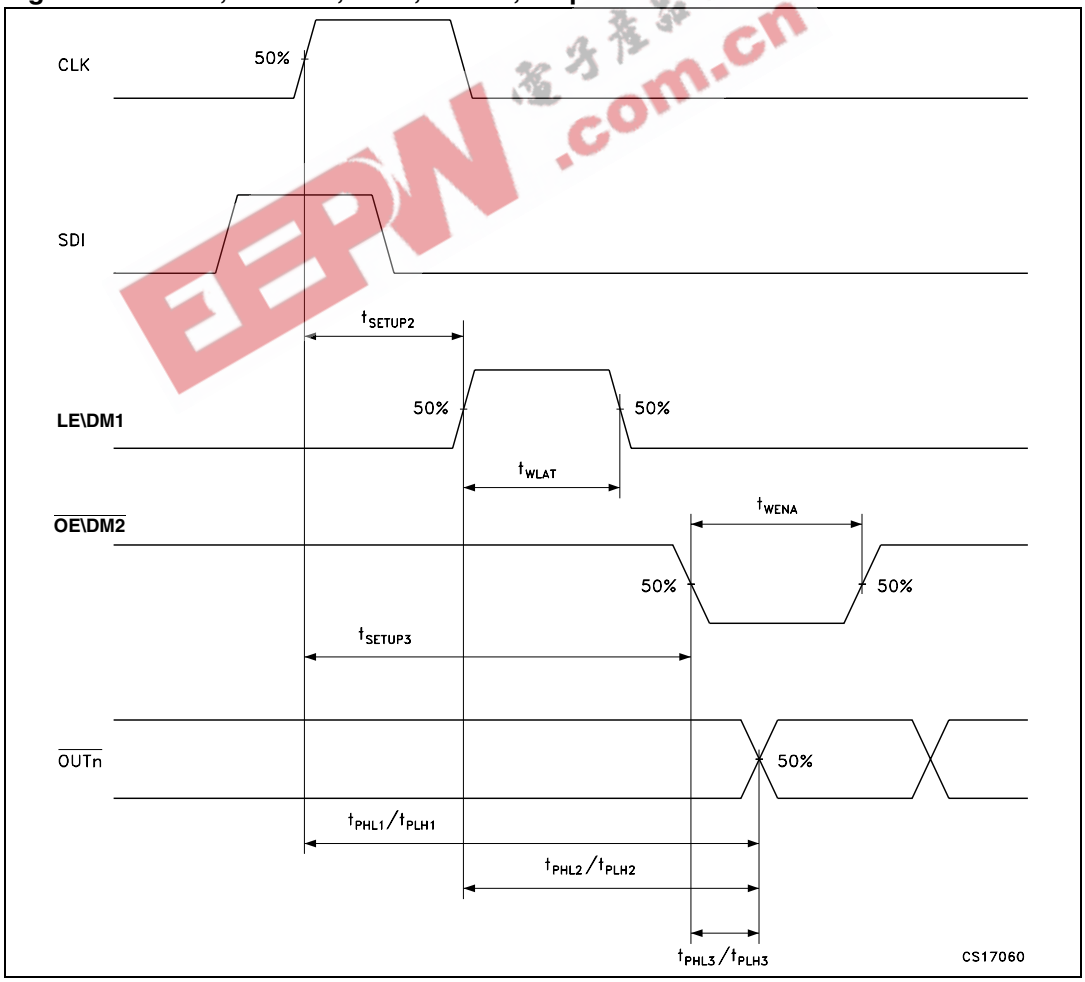
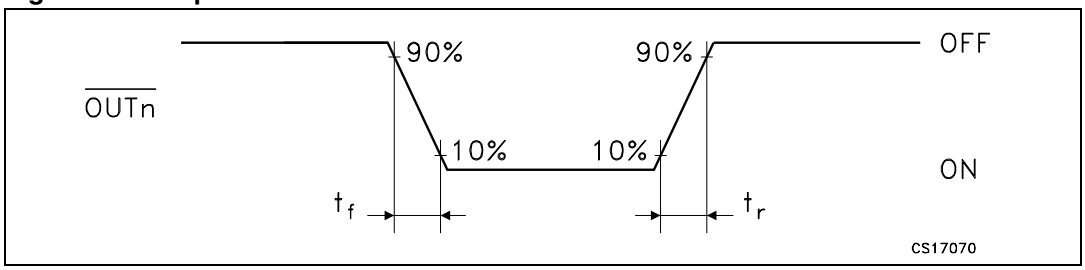


Figure 10. Outputs



6 Typical characteristics

Figure 11. Output current-R_{EXT} resistor

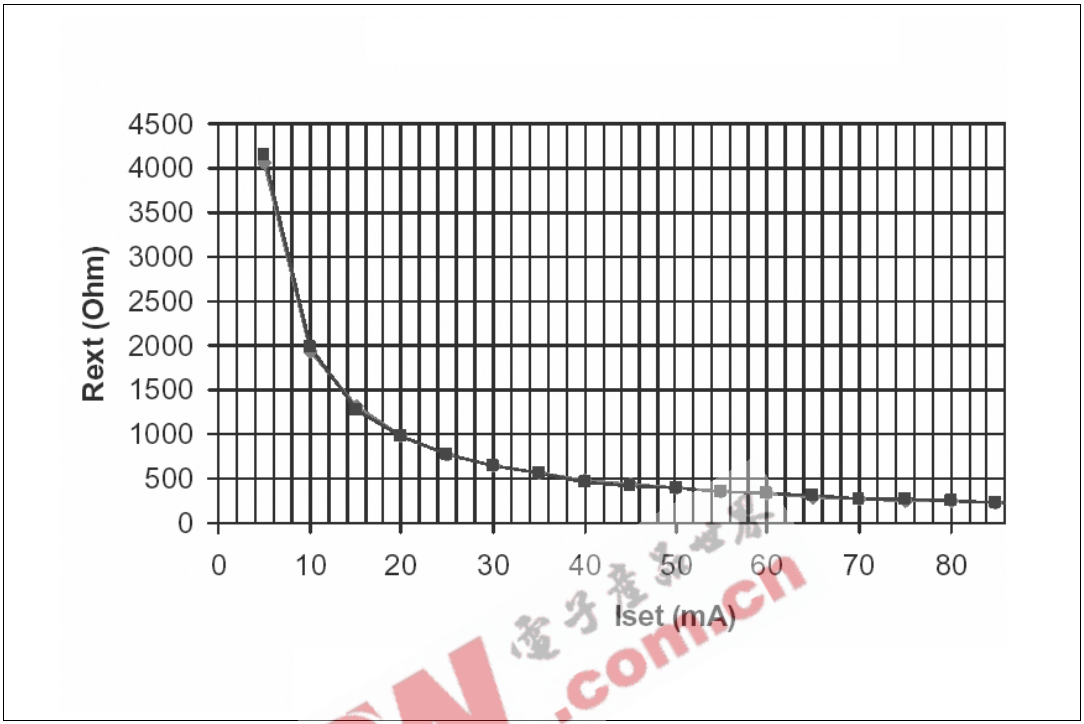


Table 10. Output current-R_{EXT} resistor

Rext (Ω)	Output current (mA)
976	20
780	25
652	30
560	35
488	40
433	45
389	50
354	55
325	60
300	65
278	70
259	75
241	80
229	85
215	90

Conditions:
Temperature = 25 °C, V_{DD} = 3.3 V; 5.0 V, I_{SET} = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 80 mA.

Figure 12. I_{SET} vs drop out voltage (V_{drop})

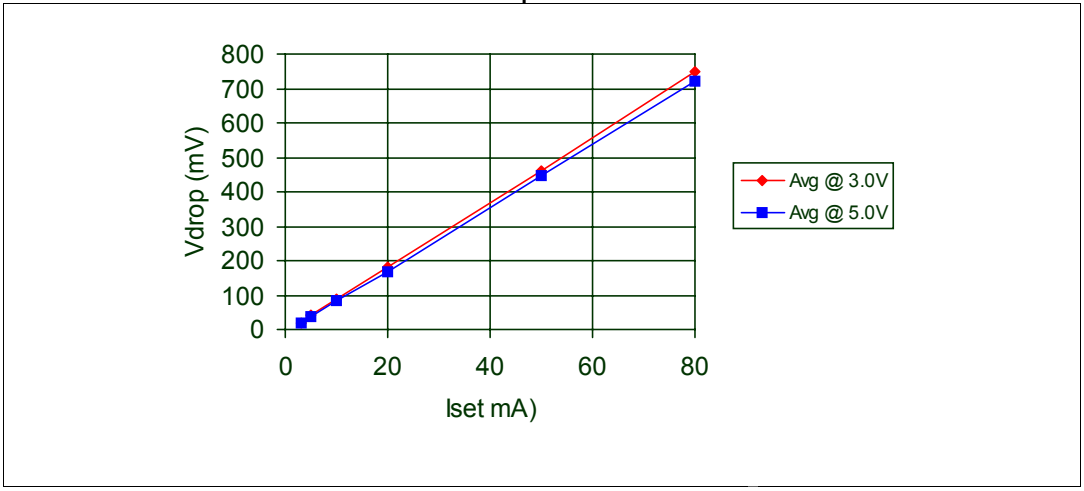


Table 11. I_{SET} vs drop out voltage (V_{drop})

Iout (mA)	Avg @ 3.0 V	Avg @ 5.0 V
3	19.33	22.66
5	36.67	40.33
10	77.33	80
20	158.67	157.33
50	406	406
80	692	668

Figure 13. I_{DD} ON\OFF

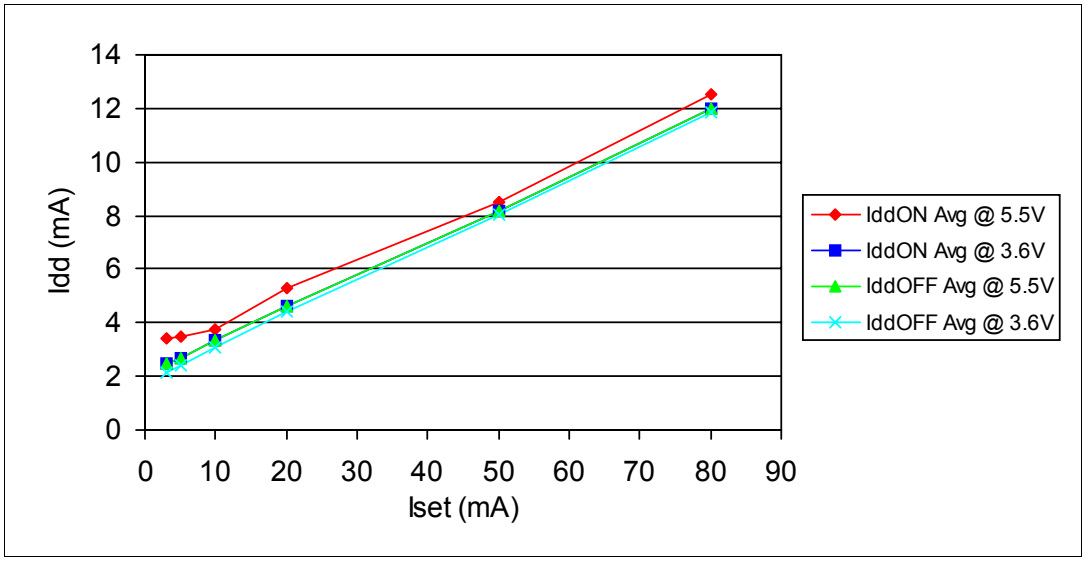
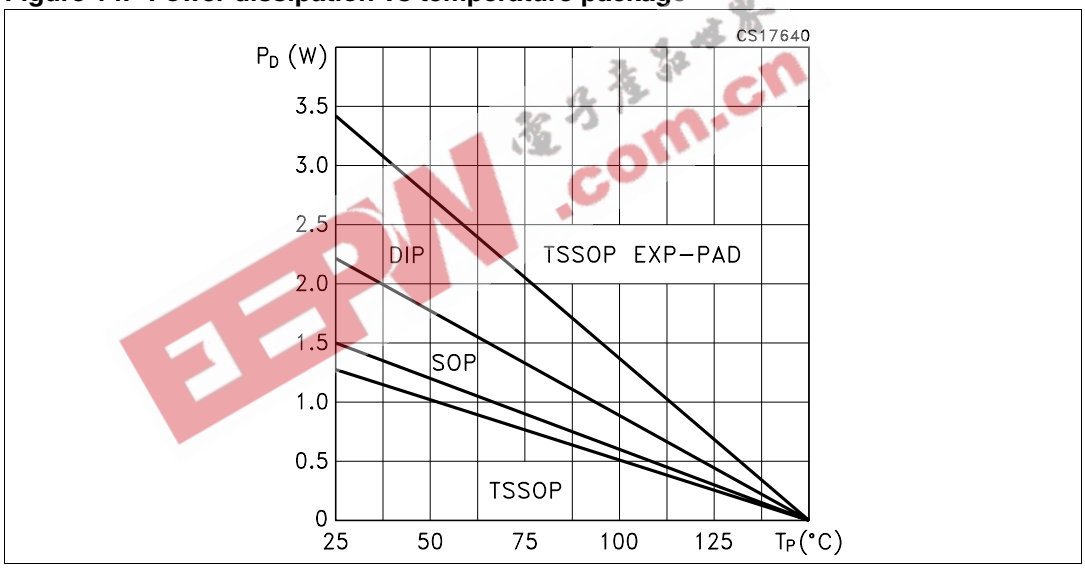


Figure 14. Power dissipation vs temperature package



Note: The exposed pad should be soldered to the PBC to realize the thermal benefits.

7 Detection mode functionality

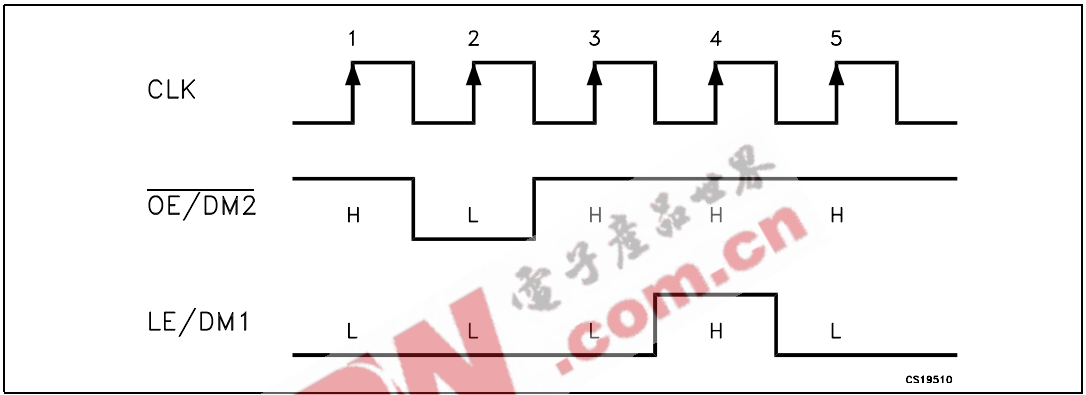
7.1 Phase one: “entering in detection mode“

From the “normal mode” condition the device can switch to the “error mode“ by a logic sequence on the *OE\DM2* and LE/DM1 pins as showed in the following table and diagram:

Table 12. Entering in detection truth table

CLK	1°	2°	3°	4°	5°
OE/DM2	H	L	H	H	H
LE/DM1	L	L	L	H	L

Figure 15. Entering in detection timing diagram

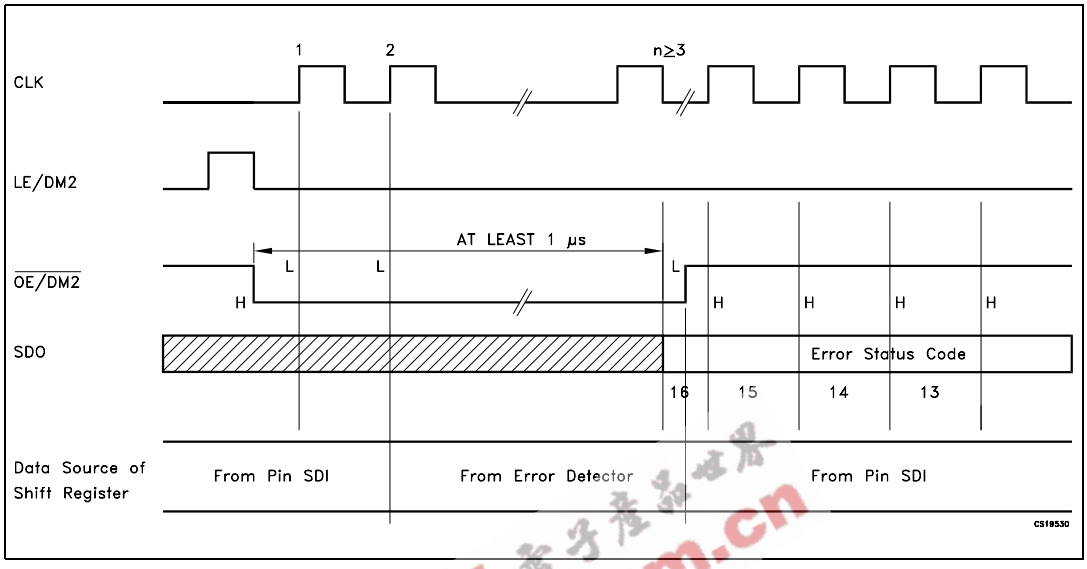


After these five CLK cycles the device goes into the “error detection mode“ and at the 6th rise front of CLK the SDI data are ready for the sampling.

7.2 Phase two: “error detection”

The 16 data bits must be set “1“ in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the Micro controller switches the $\overline{OE}$\DM2 to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

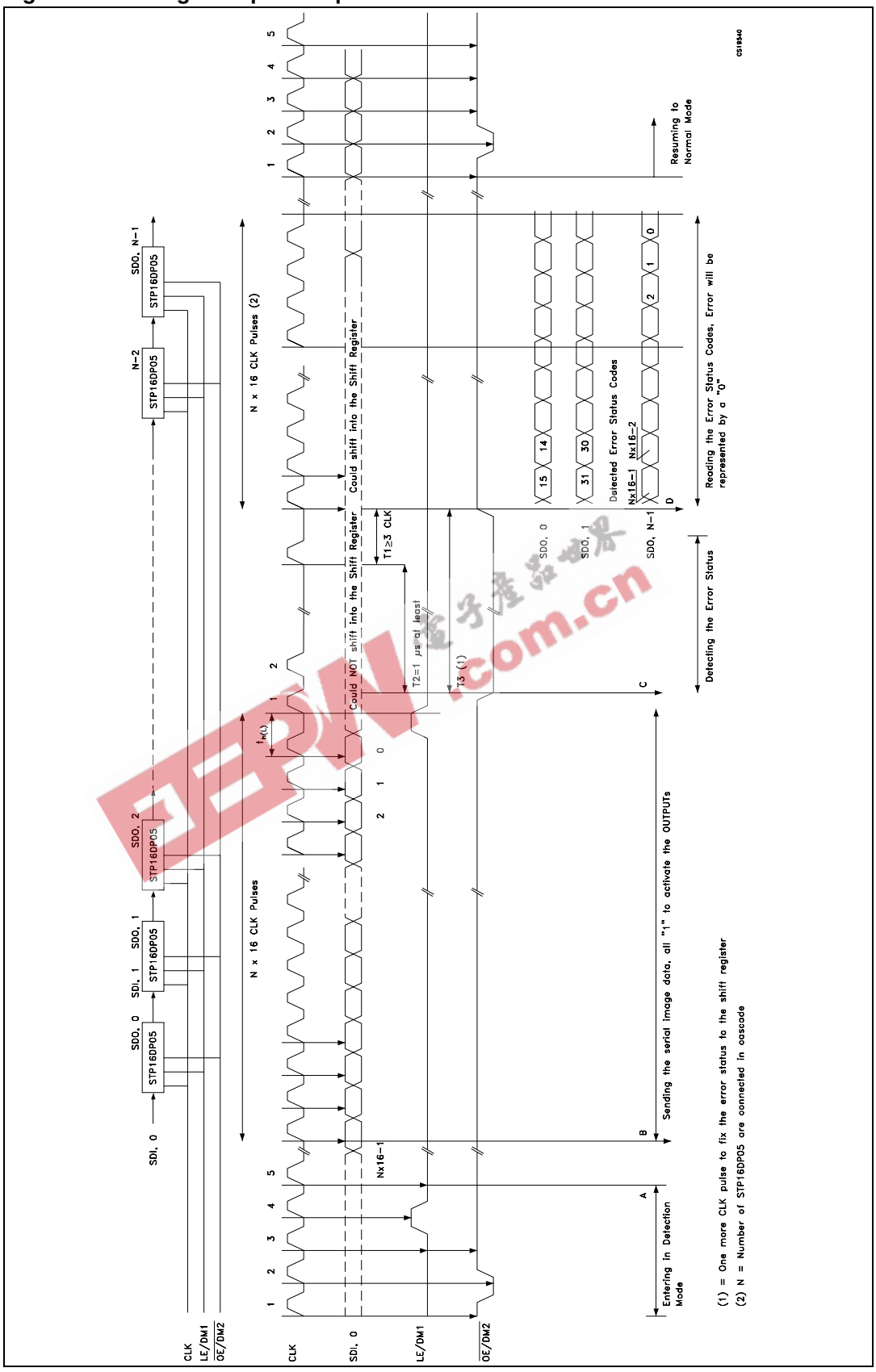
Figure 16. Detection diagram



The LEDs status will be detected at least in 1 microsecond and after this time the microcontroller sets $\overline{OE}$\DM2 in HIGH state and the output data detection result will go to the microprocessor via SDO.

Detection mode and normal mode use both the same format data. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status the device must go back in normal mode and re-entering in error detection mode .

Figure 17. Timing example for open and/or short detection



7.3 Phase three: “resuming to normal mode”

The sequence for re-entering in normal mode is showed in the following Table and diagram:

Figure 18. Resuming to normal mode timing diagram

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE/DM2}}$	H	L	H	H	H
LE/DM1	L	L	L	L	L

Note: For proper device operation the "Entering in detection" sequence must be follow by a "Resume Mode" sequence, it is not possible to insert consecutive equal sequence.

7.4 Error detection conditions

Table 13. Detection conditions (V_{DD} = 3.3 to 5 V temperature range -40 to 125 °C)

SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$	No error detected	==> $I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.4$ V	No error detected	==> $V_O \leq 2.2$ V

Note: Where: I_O = the output current programmed by the R_{EXT}, I_{ODEC} = the detected output current in detection mode

Figure 19. Detection circuit

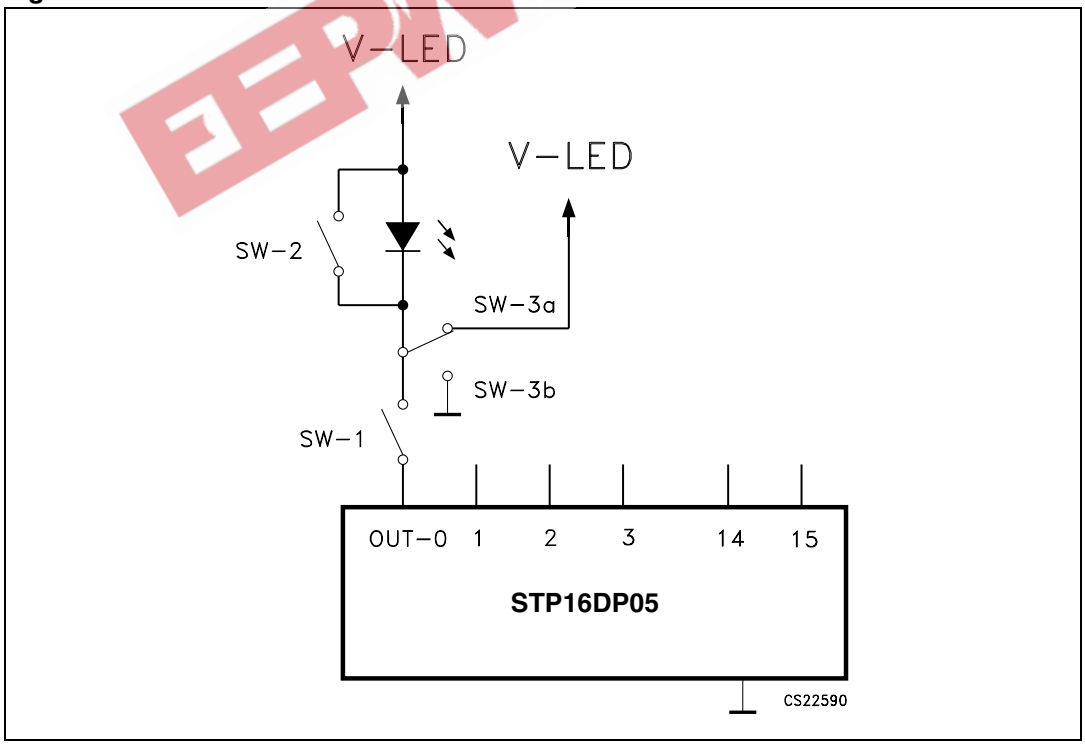
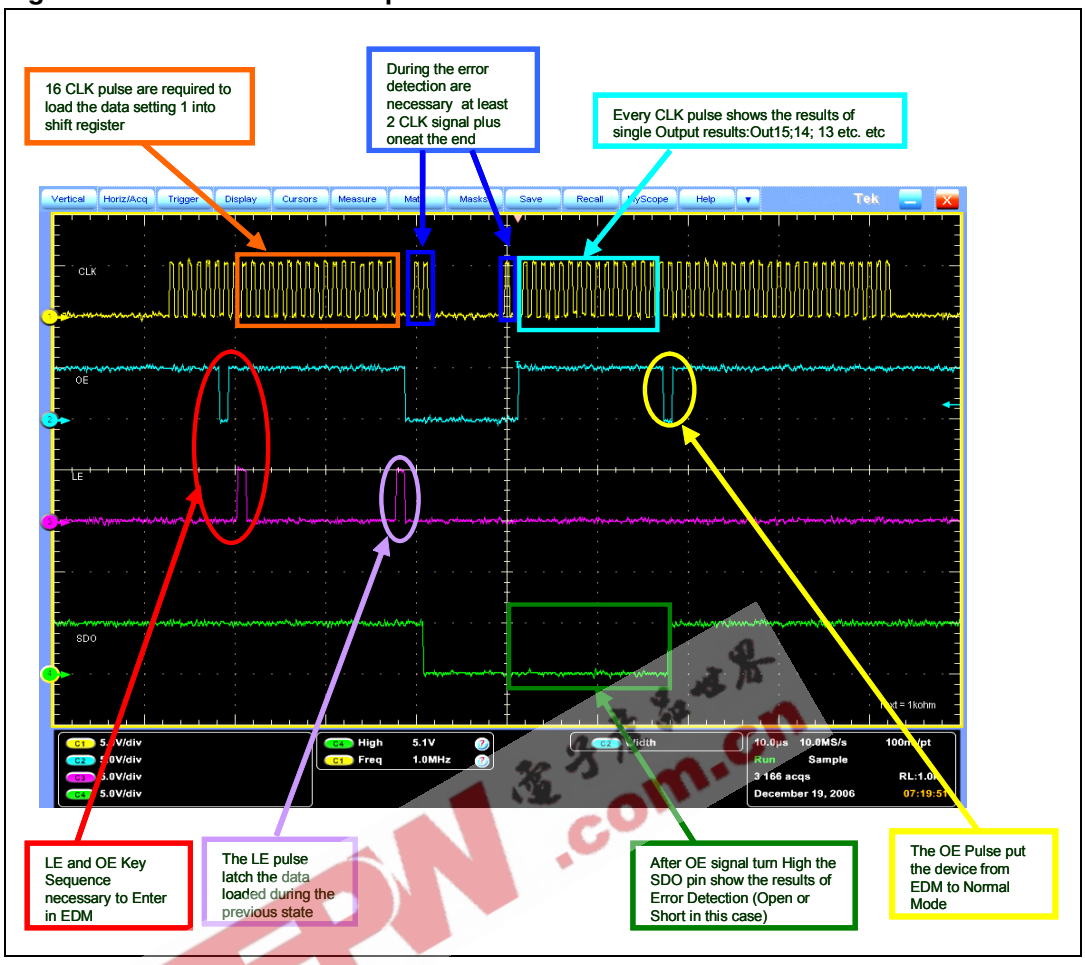


Figure 20. Error detection sequence



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 14. QSOP-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
c	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
e		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

Figure 21. QSOP-24 package dimensions

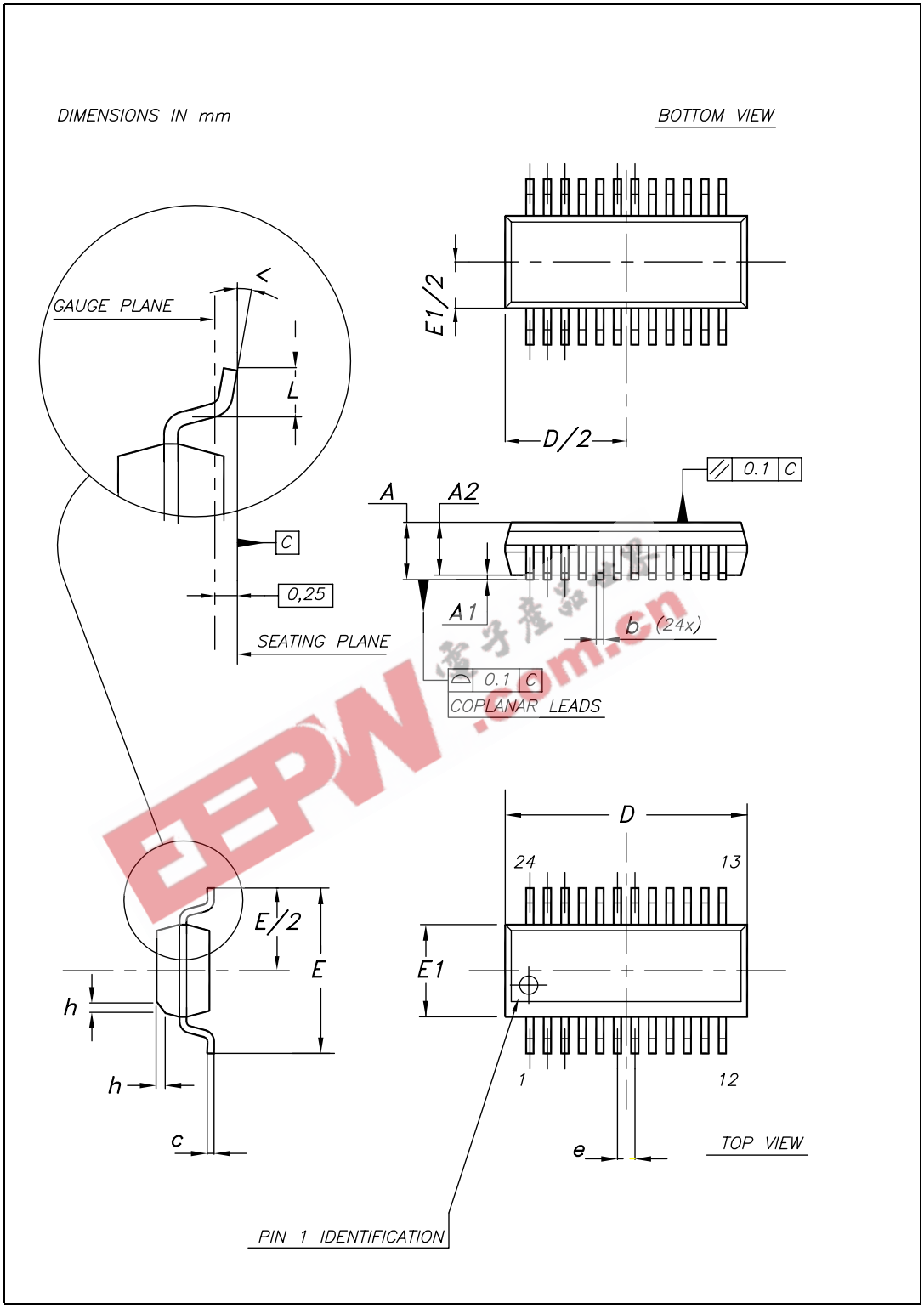


Table 15. TSSOP24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 22. TSSOP24 package dimensions

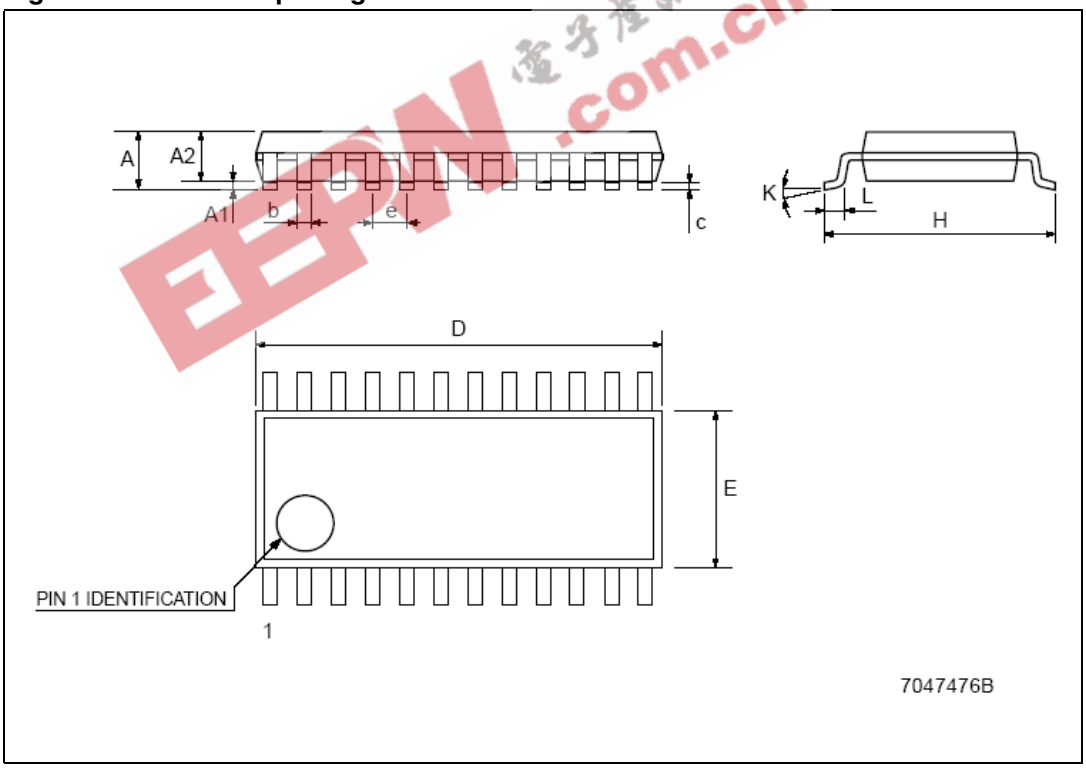


Table 16. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 23. Reel dimensions

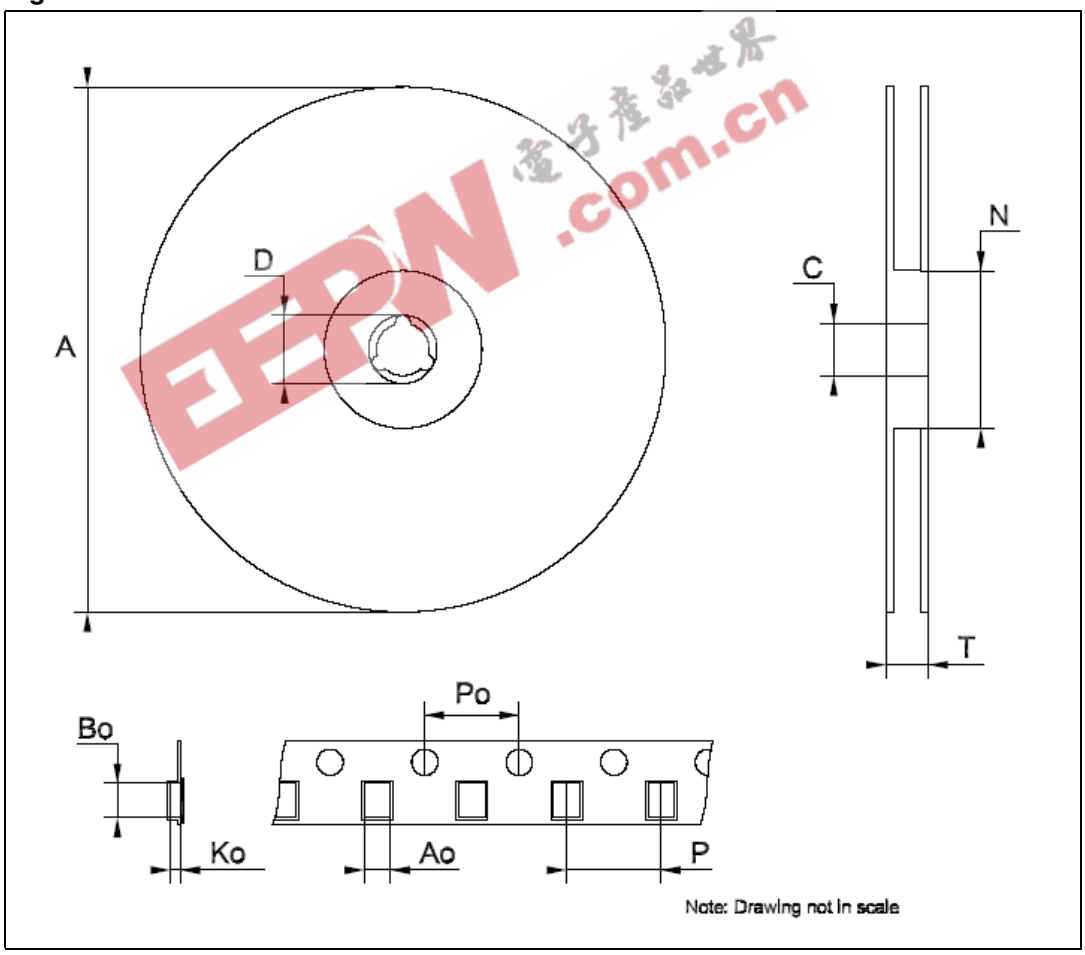


Table 17. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 24. SO-24 package dimensions

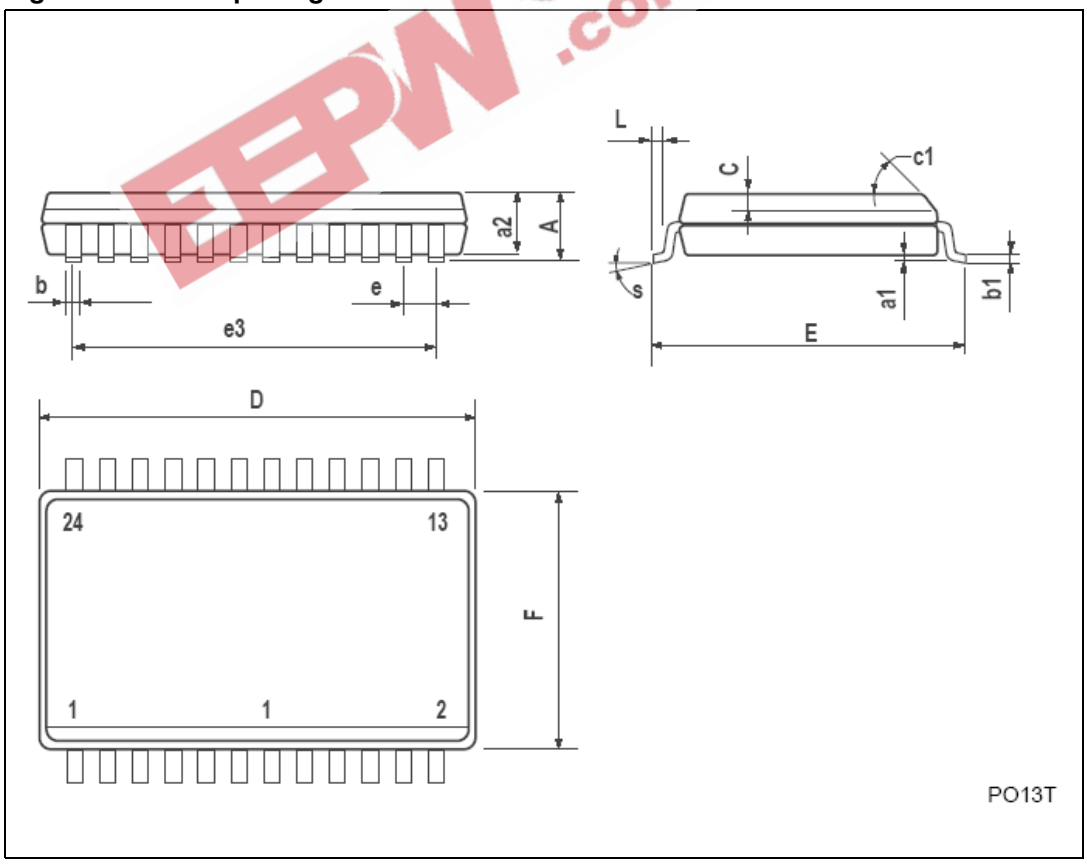


Table 18. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 25. Reel dimensions

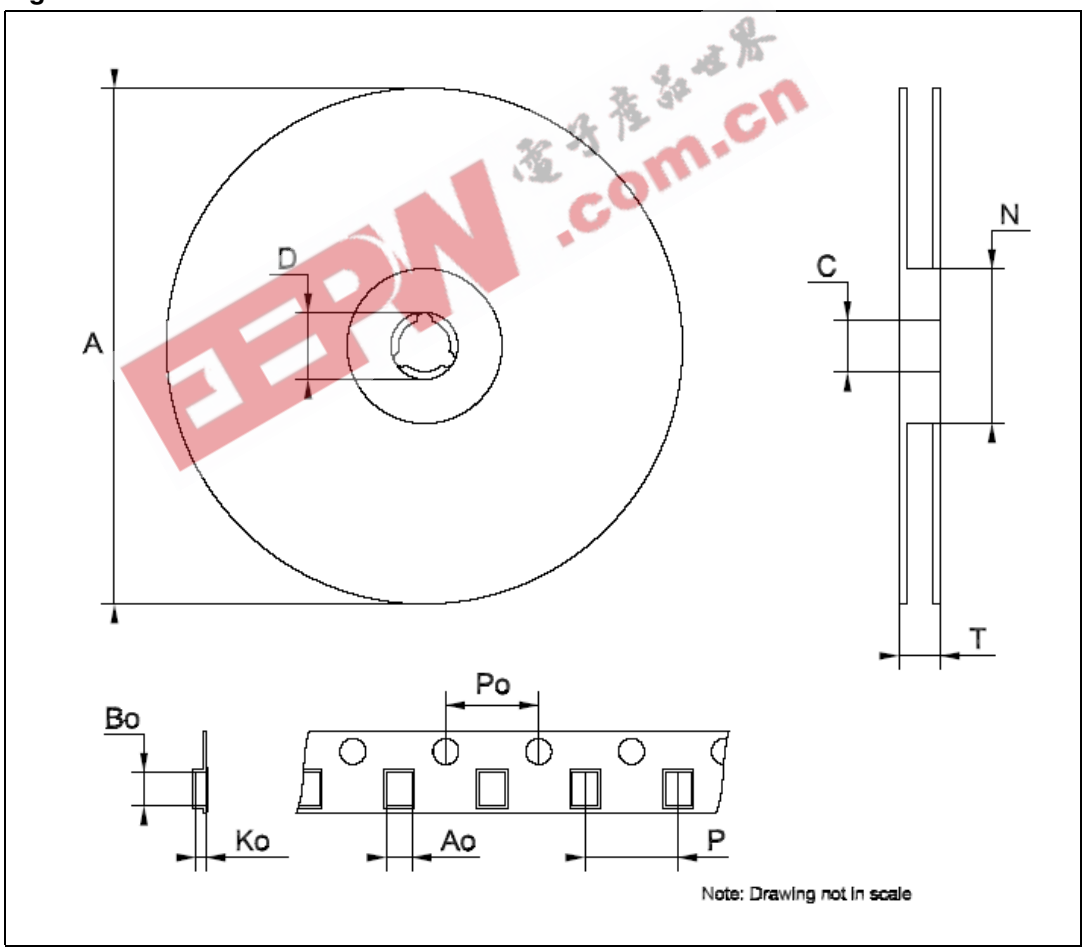
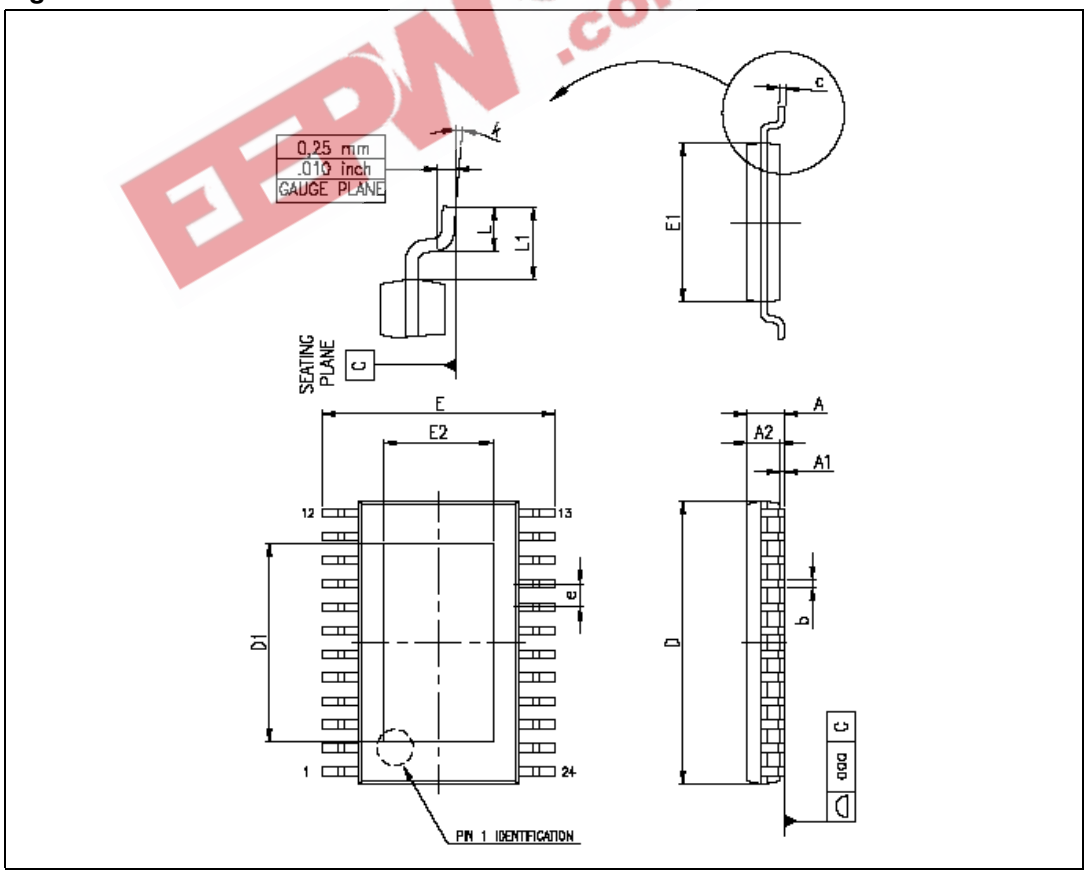


Table 19. TSSOP24 exposed pad

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 26. TSSOP24 dimensions



9 Revision history

Table 20. Document revision history

Date	Revision	Changes
9-Jan-2007	1	First release
21-May-2007	2	Updated *Table 7 on page 6*
10-Jul-2007	3	Updated *Table 9: Truth table on page 10*
28-Feb-2008	4	Updated *Table 15: TSSOP24 exposed-pad on page 23* Added QSOP-24 package information *Table 14* and *Figure 21 on page 22*

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