

Features

- No External Components Except PIN Diode
- Supply-voltage Range: 4.5 V to 5.5 V
- Automatic Sensitivity Adaptation (AGC)
- Automatic Strong Signal Adaptation (ATC)
- Enhanced Immunity Against Ambient Light Disturbances
- Available for Carrier Frequencies between 30 kHz to 76 kHz; Adjusted by Zener Diode Fusing
- TTL and CMOS Compatible
- Suitable Minimum Burst Length ≥ 6 or 10 Pulses/Burst

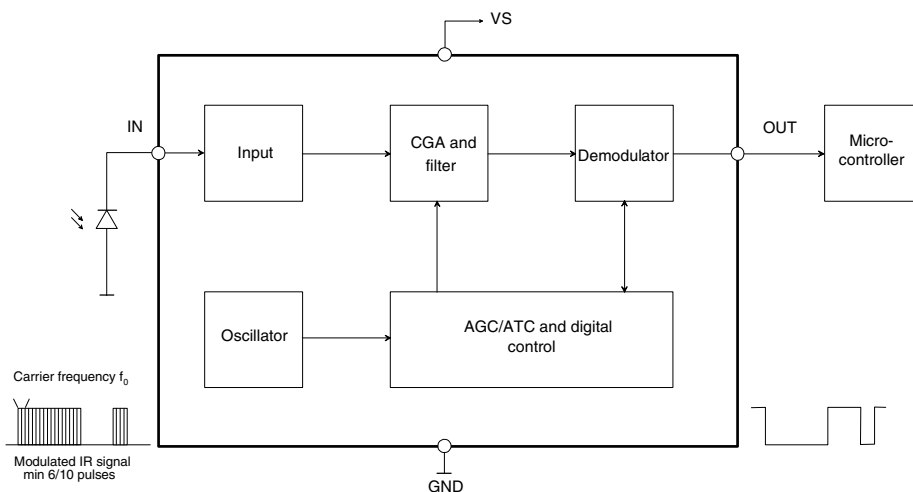
Applications

- Audio Video Applications
- Home Appliances
- Remote Control Equipment

Description

The IC T2525 is a complete IR receiver for data communication developed and optimized for use in carrier-frequency-modulated transmission applications. Its function can be described using the block diagram (see Figure 1). The input stage meets two main functions. First, it provides a suitable bias voltage for the PIN diode. Secondly, the pulsed photo-current signals are transformed into a voltage by a special circuit which is optimized for low-noise applications. After amplification by a Controlled Gain Amplifier (CGA), the signals have to pass a tuned integrated narrow bandpass filter with a center frequency f_0 which is equivalent to the chosen carrier frequency of the input signal. The demodulator is used to convert the input burst signal into a digital envelope output pulse and to evaluate the signal information quality, i.e., unwanted pulses will be suppressed at the output pin. All this is done by means of an integrated dynamic feedback circuit which varies the gain as a function of the present environmental condition (ambient light, modulated lamps etc.). Other special features are used to adapt to the current application to secure best transmission quality. The T2525 operates in a supply-voltage range of 4.5 V to 5.5 V.

Figure 1. Block Diagram



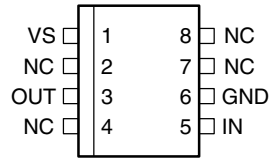
IR Receiver
ASSP

T2525



Pin Configuration

Figure 2. Pinning SO8 and TSSOP8



Pin Description

| Pin | Symbol | Function |
|-----|--------|-----------------|
| 1 | VS | Supply voltage |
| 2 | NC | Not connected |
| 3 | OUT | Data output |
| 4 | NC | Not connected |
| 5 | IN | Input PIN diode |
| 6 | GND | Ground |
| 7 | NC | Not connected |
| 8 | NC | Not connected |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---|-----------|---------------|------|
| Supply voltage | V_S | -0.3 to +6 | V |
| Supply current | I_S | 3 | mA |
| Input voltage | V_{IN} | -0.3 to V_S | V |
| Input DC current at $V_S = 5\text{ V}$ | I_{IN} | 0.75 | mA |
| Output voltage | V_O | -0.3 to V_S | V |
| Output current | I_O | 10 | mA |
| Operating temperature | T_{amb} | -25 to +85 | °C |
| Storage temperature | T_{stg} | -40 to +125 | °C |
| Power dissipation at $T_{amb} = 25^\circ\text{C}$ | P_{tot} | 30 | mW |

Thermal Resistance

| Parameter | Symbol | Value | Unit |
|-------------------------|------------|-------|------|
| Junction ambient SO8 | R_{thJA} | 130 | K/W |
| Junction ambient TSSOP8 | R_{thJA} | TBD | K/W |

Electrical Characteristics

$T_{amb} = 25^{\circ}\text{C}$, $V_S = 5\text{ V}$ unless otherwise specified.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|--|-----|-----------------|--------------|-------|-------|---------------|-------|
| 1 | Supply | | | | | | | | |
| 1.1 | Supply-voltage range | | 1 | V_S | 4.5 | 5 | 5.5 | V | C |
| 1.2 | Supply current | $I_{IN} = 0$ | 1 | I_S | 0.8 | 1.1 | 1.4 | mA | B |
| 2 | Output | | | | | | | | |
| 2.1 | Internal pull-up resistor ⁽¹⁾ | $T_{amb} = 25^{\circ}\text{C}$; see Figure 9 on page 7 | 1,3 | R_{PU} | | 30/40 | | k Ω | A |
| 2.2 | Output voltage low | $I_L = 2\text{ mA}$; see Figure 9 on page 7 | 3,6 | V_{OL} | | | 250 | mV | B |
| 2.3 | Output voltage high | | 3,1 | V_{OH} | $V_S - 0.25$ | | V_S | V | B |
| 2.4 | Output current clamping | $R_2 = 0$; see Figure 9 on page 7 | 3,6 | I_{OCL} | | 8 | | mA | B |
| 3 | Input | | | | | | | | |
| 3.1 | Input DC current | $V_{IN} = 0$; see Figure 9 on page 7 | 5 | I_{IN_DCMAX} | -85 | | | μA | C |
| 3.2 | Input DC current; Figure 4 on page 5 | $V_{IN} = 0$; $V_S = 5\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$ | 5 | I_{IN_DCMAX} | -530 | -960 | | μA | B |
| 3.3 | Minimum detection threshold current; Figure 3 on page 5 | Test signal: see Figure 8 on page 7 $V_S = 5\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $I_{IN_DC} = 1\text{ }\mu\text{A}$; square pp, burst $N = 16$, $f = f_0$; $t_{PER} = 10\text{ ms}$, Figure 8 on page 7; $BER = 50^{(2)}$ | 3 | I_{Eemin} | | -520 | | μA | B |
| 3.4 | Minimum detection threshold current with AC current disturbance $I_{IN_AC100} = 3\text{ }\mu\text{A}$ at 100 Hz | Test signal: see Figure 8 on page 7 $V_S = 5\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $I_{IN_DC} = 1\text{ }\mu\text{A}$; square pp, burst $N = 16$, $f = f_0$; $t_{PER} = 10\text{ ms}$, Figure 8 on page 7; $BER = 50\%^{(2)}$ | 3 | I_{Eemin} | | -800 | | μA | C |

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Depending on version, see "Ordering Information"
 2. BER = Bit Error Rate; e.g., BER = 5% means that with $P = 20$ at the input pin 19..21 pulses can appear at the pin OUT
 3. After transformation of input current into voltage

Electrical Characteristics (Continued)

$T_{amb} = 25^{\circ}\text{C}$, $V_S = 5\text{ V}$ unless otherwise specified.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|--|-----|---------------|------|-------|------|---------------|-------|
| 3.5 | Maximum detection threshold current with $V_{IN} > 0\text{V}$ | Test signal: see Figure 8 on page 7 $V_S = 5\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $I_{IN_DC} = 1\ \mu\text{A}$; square pp, burst $N = 16$, $f = f_0$; $t_{PER} = 10\text{ ms}$, Figure 8 on page 7; $BER = 5\%^{(2)}$ | 3 | I_{Eemax} | -400 | | | μA | D |
| 4 | Controlled Amplifier and Filter | | | | | | | | |
| 4.1 | Maximum value of variable gain (CGA) | | | G_{VARMAX} | | 51 | | dB | D |
| 4.2 | Minimum value of variable gain (CGA) | | | G_{VARMIN} | | -5 | | dB | D |
| 4.3 | Total internal amplification ⁽³⁾ | | | G_{MAX} | | 71 | | dB | D |
| 4.4 | Center frequency fusing accuracy of bandpass | $V_S = 5\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$ | | f_{0_FUZE} | -3 | f_0 | +3 | % | A |
| 4.5 | Overall accuracy center frequency of bandpass | | | f_0 | -6.7 | f_0 | +4.1 | % | C |
| 4.6 | BPF bandwidth: type N0 - N3 | -3 dB; $f_0 = 38\text{ kHz}$; see Figure 6 on page 6 | | B | | 3.5 | | kHz | C |
| | BPF bandwidth: type N6, N7 | -3 dB; $f_0 = 38\text{ kHz}$; see Figure 6 on page 6 | | B | | 5.4 | | kHz | C |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Depending on version, see "Ordering Information"
 2. BER = Bit Error Rate; e.g., BER = 5% means that with $P = 20$ at the input pin 19...21 pulses can appear at the pin OUT
 3. After transformation of input current into voltage

ESD All pins \Rightarrow 2000V HBM; 200V MM, MIL-STD-883C, Method 3015.7

Reliability Electrical qualification (1000h) in molded SO8 plastic package

Typical Electrical Curves at $T_{amb} = 25^{\circ}\text{C}$

Figure 3. I_{Eemin} versus I_{IN_DC} , $V_S = 5\text{ V}$

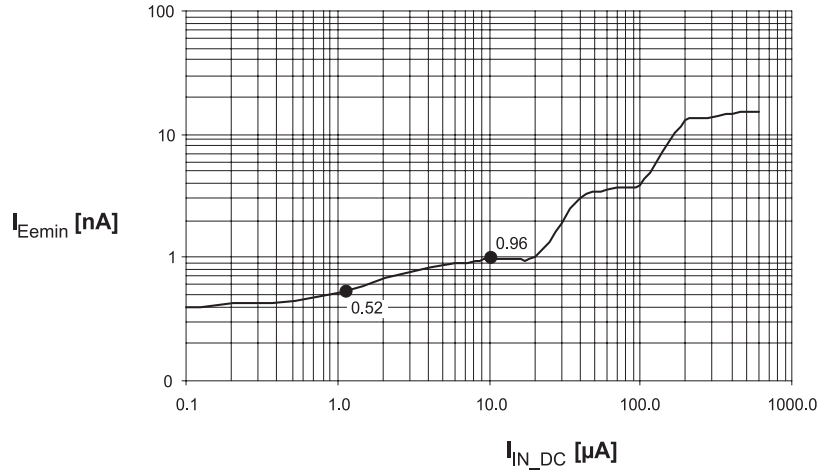


Figure 4. V_{IN} versus I_{IN_DC} , $V_S = 5\text{ V}$

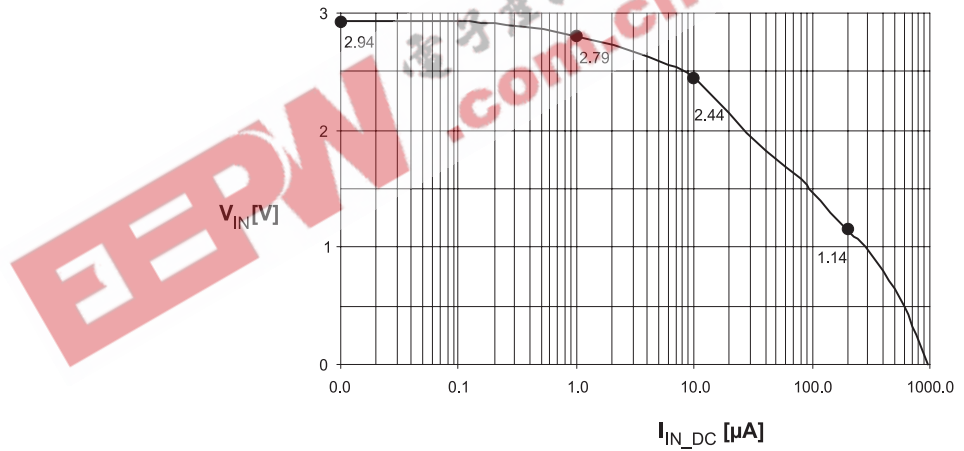


Figure 5. Data Transmission Rate, $V_S = 5\text{ V}$

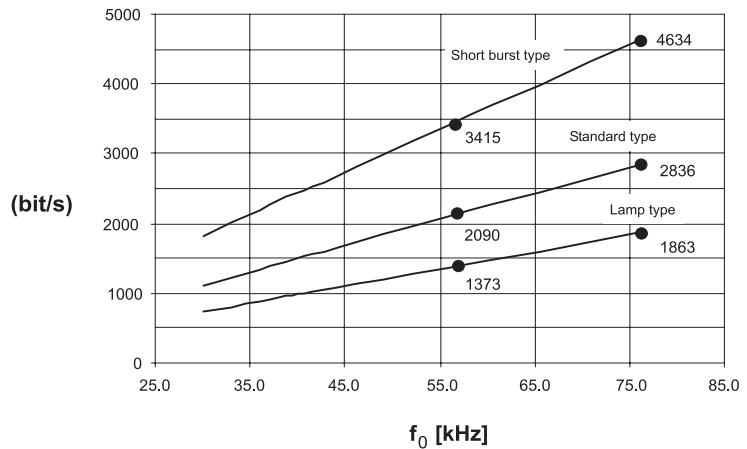
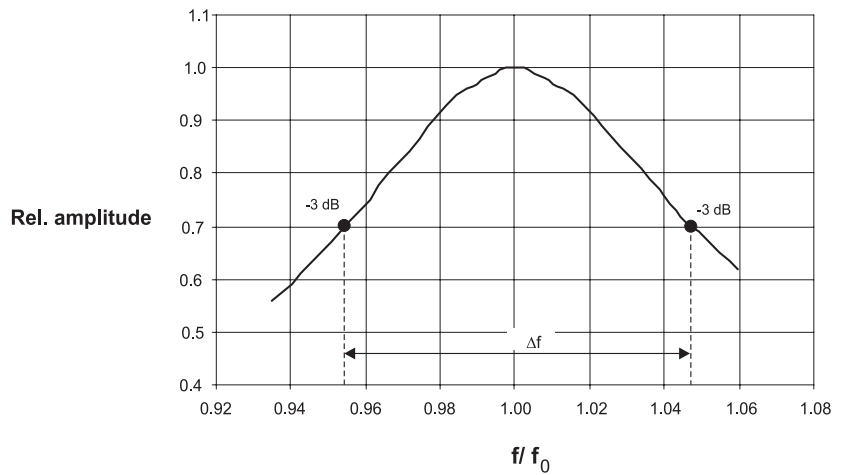
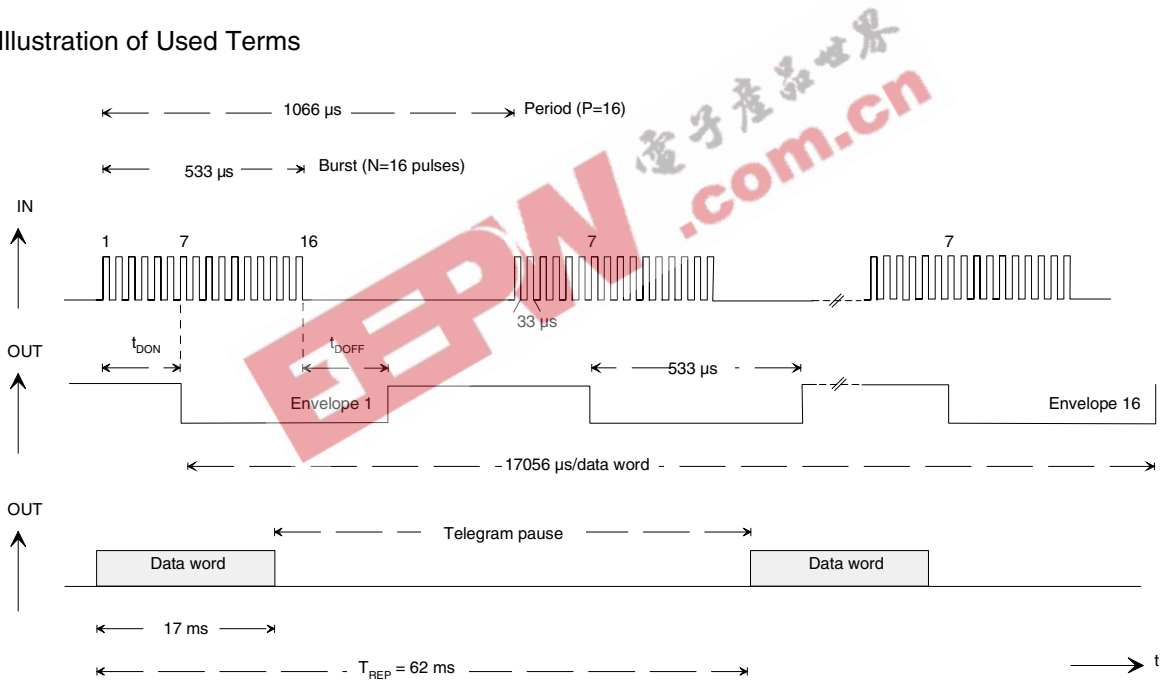


Figure 6. Typical Bandpass Curve



$Q = f_0/\Delta f$; $\Delta f = -3 \text{ dB values}$. Example: $Q = 1/(1.047 - 0.954) = 11$

Figure 7. Illustration of Used Terms



Example: $f = 30 \text{ kHz}$, burst with 16 pulses, 16 periods

Figure 8. Test Circuit

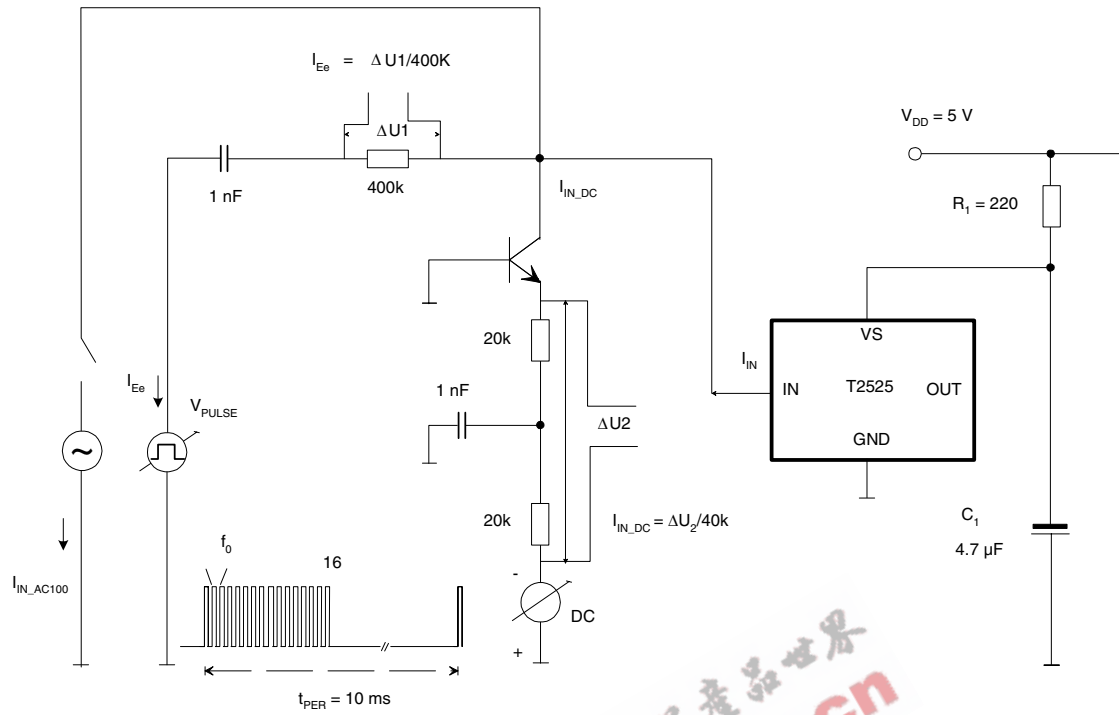
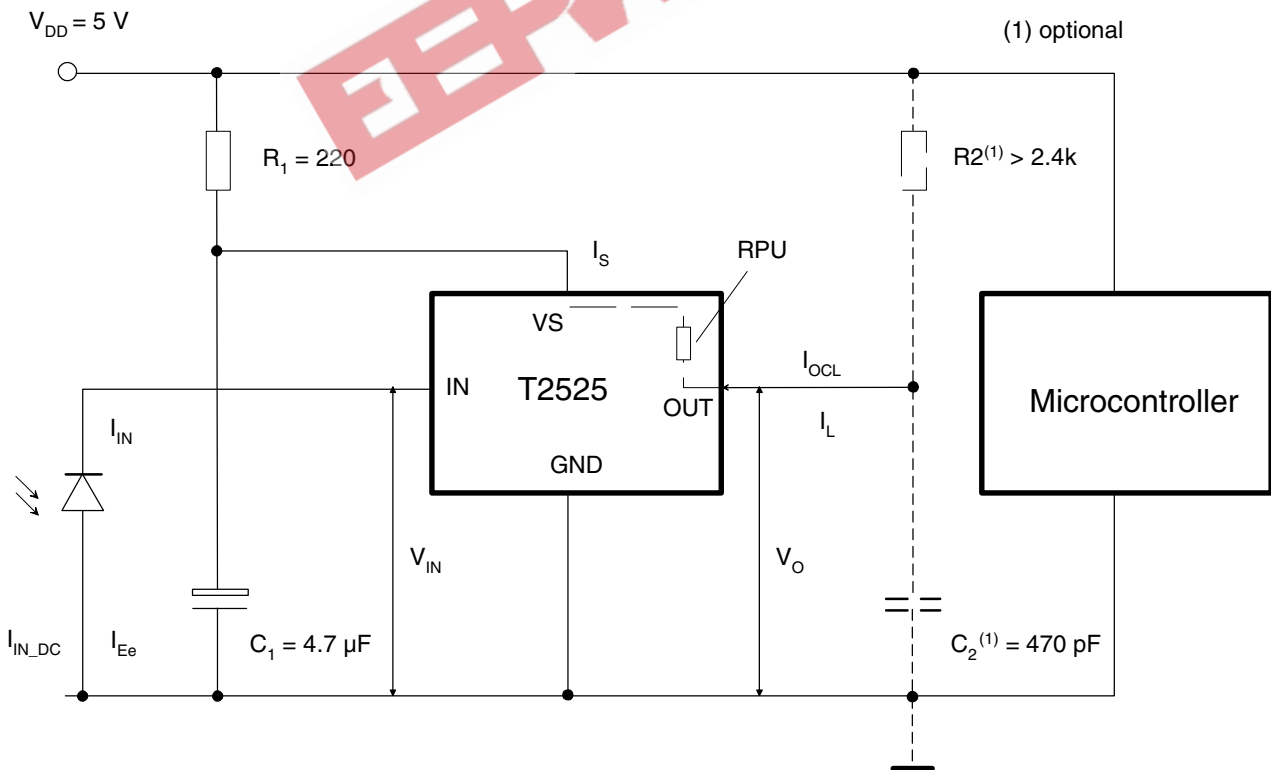
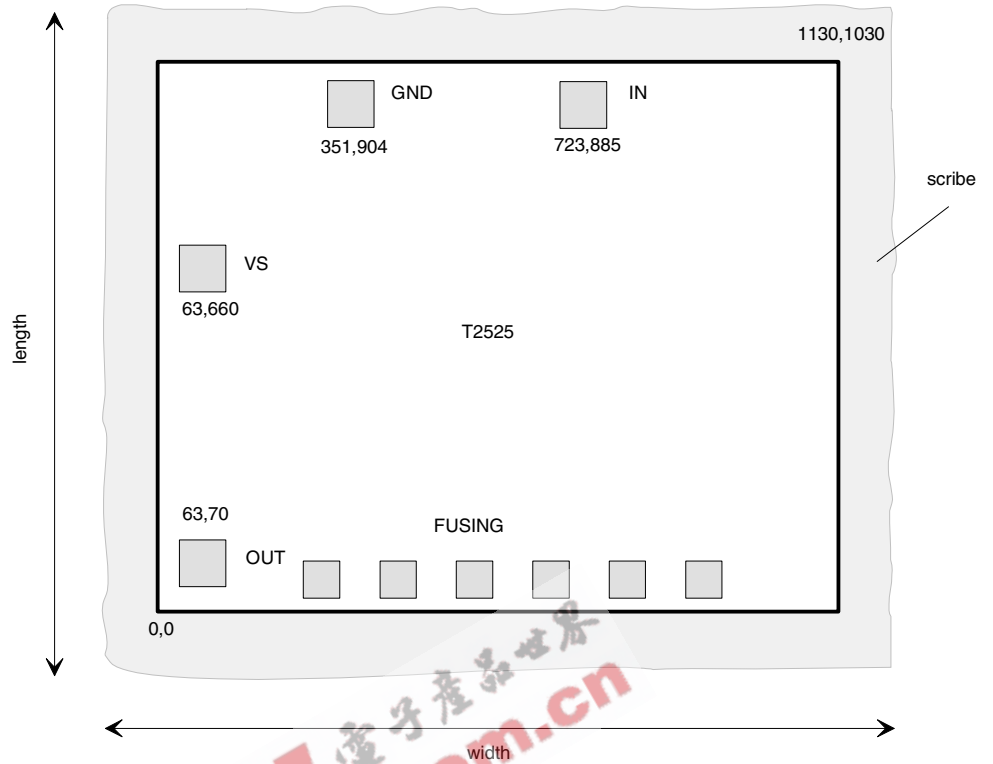


Figure 9. Application Circuit



Chip Dimensions

Figure 10. Chip Size in μm



Note: Pad coordinates are for lower left corner of the pad in μm from the origin 0,0

| | | |
|-----------------------|-------------------------|--------------------------------------|
| Dimensions | Length inclusive scribe | 1.15 mm |
| | Width inclusive scribe | 1.29 mm |
| | Thickness | $290 \mu \pm 5\%$ |
| Pad metallurgy | Pads | $90 \mu \times 90 \mu$ |
| | Fusing pads | $70 \mu \times 70 \mu$ |
| | Material | $\text{AlCu/AlSiTi}^{(1)}$ |
| Finish | Thickness | $0.8 \mu\text{m}$ |
| | Material | $\text{Si}_3\text{N}_4/\text{SiO}_2$ |
| | Thickness | $0.7/0.3 \mu\text{m}$ |

Note: 1. Value depends on manufacture location.

Ordering Information

| Extended Type Number | PL ⁽²⁾ | R _{PU} ⁽³⁾ | D ⁽⁴⁾ | Type |
|--|-------------------|--------------------------------|------------------|---|
| T2525N0xx ⁽¹⁾ -yyy ⁽⁵⁾ | 2 | 30 | 2090 | Standard type: ≥ 10 pulses, enhanced sensibility, high data rate |
| T2525N1xx ⁽¹⁾ -DDW | 1 | 30 | 2090 | Standard type: ≥ 10 pulses, enhanced sensibility, high data rate |
| T2525N2xx ⁽¹⁾ -yyy ⁽⁵⁾ | 2 | 40 | 1373 | Lamp type: ≥ 10 pulses, enhanced suppression of disturbances, secure data transmission |
| T2525N3xx ⁽¹⁾ -DDW | 1 | 40 | 1373 | Lamp type: ≥ 10 pulses, enhanced suppression of disturbances, secure data transmission |
| T2525N6xx ⁽¹⁾ -yyy ⁽⁵⁾ | 2 | 30 | 3415 | Short burst type: ≥ 6 pulses, enhanced data rate |
| T2525N7xx ⁽¹⁾ -DDW | 1 | 30 | 3415 | Short burst type: ≥ 6 pulses, enhanced data rate |

- Notes:
- xx means the used carrier frequency value f_0 30,33,36,38,40,44,56 kHz. (76 kHz type on request)
 - Two pad layout versions (see Figure 11 and Figure 12) available for different assembly demand
 - Integrated pull-up resistor at pin OUT (see “Electrical Characteristics”)
 - Typical data transmission rate up to bit/s with $f_0 = 56$ kHz, $V_S = 5$ V (see Figure 5 on page 5)
 - yyy means kind of packaging:
DDW -> unsawn wafers in box
6AQ -> (only on request, TSSOP8 taped and reeled)

Pad Layout

Figure 11. Pad Layout 1 (DDW only)

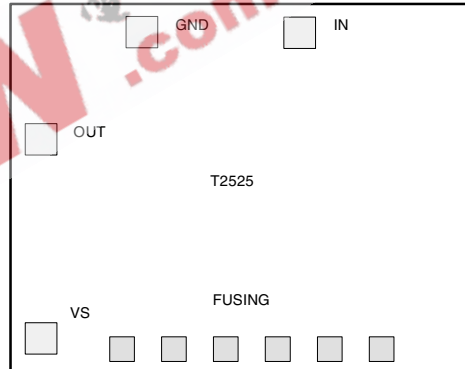
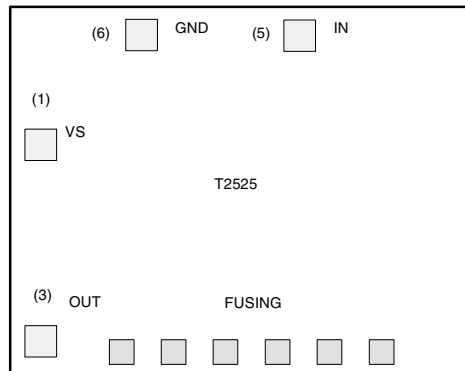


Figure 12. Pad Layout 2 (DDW, SO8 or TSSOP8)





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