

SRAM

512K X 16 LOW POWER CMOS STATIC RAM

FEATURES

- Low-power consumption
 - Active: 5mA (I_{CC1})
 - Stand-by: 2uA (CMOS input/output)
- 55/70/100 ns access time
- Equal access and cycle time
- Single +2.7V to 3.6V Power Supply
- TTL compatible , Tri-state output
- Common I/O capability
- Automatic power-down when deselected
- Available in 44-PIN TSOP-II and 48-pin CSP packages

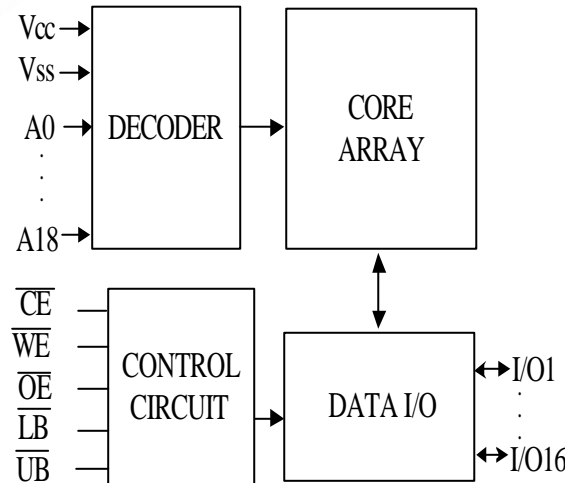
PART NUMBER EXAMPLES

| PART NO. | PACKAGE CODE |
|----------------|--------------|
| T15V8M16A-55S | S = TSOP-II |
| T15V8M16A-70C | C = CSP |
| T15V8M16A-100C | |

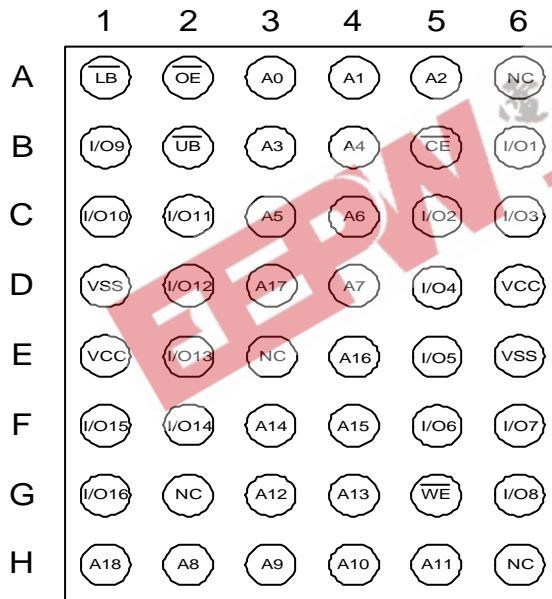
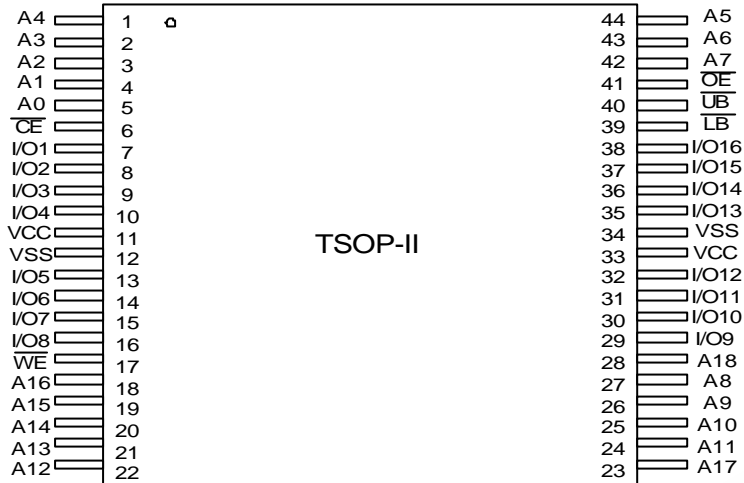
GENERAL DESCRIPTION

The T15V8M16A is a very Low Power CMOS Static RAM organized as 524,288 words by 16 bits. That operates on a wide voltage range from 2.7V to 3.6V power supply, Fabricated using high performance CMOS technology, Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. Data retention is guaranteed at a power supply voltage as low as 2V.

BLOCK DIAGRAM



PIN CONFIGURATIONS



48-Ball CSP TOP VIEW (Ball Down)

PIN DESCRIPTIONS

| SYMBOL | DESCRIPTIONS | SYMBOL | DESCRIPTIONS |
|------------------------|---------------------|------------------------|-----------------------|
| A0 ~ A18 | Address inputs | $\overline{\text{LB}}$ | Lower byte (I/O 1~8) |
| I/O0~I/O16 | Data inputs/outputs | $\overline{\text{UB}}$ | Upper byte (I/O 9~16) |
| $\overline{\text{CE}}$ | Chip enable | VCC | Power supply |
| $\overline{\text{WE}}$ | Write enable input | VSS | Ground |
| $\overline{\text{OE}}$ | Output enable input | NC | No connection |

ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYM | MIN. | MAX. | UNIT |
|------------------------------------|-------------------|------|--------|------|
| Voltage on Any Pin Relative to VSS | V _R | -0.2 | +3.6 V | V |
| Power Dissipation | P _D | - | 1.0 | W |
| Storage Temperature | T _{STG} | -55 | +150 | °C |
| Temperature Under Bias | I _{BIAS} | -40 | +85 | °C |

*Note: Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{UB} | I/O 1~8 | I/O 9~16 | MODE | Power |
|-----------------|-----------------|-----------------|-----------------|-----------------|----------|----------|------------------|---------|
| H | X* | X* | X* | X* | High-Z | High-Z | Deselected | Standby |
| X* | X* | X* | H | H | High-Z | High-Z | Deselected | Standby |
| L | H | H | L | X* | High-Z | High-Z | Output Disabled | Active |
| L | H | H | X* | L | High-Z | High-Z | Output Disabled | Active |
| L | L | H | L | H | Data Out | High-Z | Lower Byte Read | Active |
| L | L | H | H | L | High-Z | Data Out | Upper Byte Read | Active |
| L | L | H | L | L | Data Out | Data Out | Word Read | Active |
| L | X* | L | L | H | Data In | High-Z | Lower Byte Write | Active |
| L | X* | L | H | L | High-Z | Data In | Upper Byte Write | Active |
| L | X* | L | L | L | Data In | Data In | Word Write | Active |

*Note: X = Don't Care (Must be low or high state), L = Low, H = High

RECOMMENDED OPERATING CONDITIONS

(Ta = -40°C to 85°C**)

| PARAMETER | SYM | MIN | TYP | MAX | UNIT |
|----------------|-----------------|------|-----|----------------------|------|
| Supply Voltage | V _{CC} | 2.7 | 3.0 | 3.6 | V |
| | V _{SS} | 0.0 | 0.0 | 0.0 | V |
| Input Voltage | V _{IH} | 2.1 | - | V _{CC} +0.3 | V |
| | V _{IL} | -0.2 | - | 0.6 | V |

OPERATING CHARACTERISTICS

 (V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = -40°C to 85°C)

| PARAMETER | SYM. | TEST CONDITIONS | -55 | | -70 | | -100 | | UNIT |
|---|------------------|--|-----|-----|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | I _{LI} | V _{CC} = Max, V _{IN} = V _{SS} to V _{CC} | - | 1 | - | 1 | - | 1 | uA |
| Output Leakage Current | I _{LO} | $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ V _{IO} = V _{SS} to V _{CC} | - | 1 | - | 1 | - | 1 | uA |
| Operating Power Supply Current | I _{CC} | $\overline{\text{CE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$, $\overline{\text{OE}} = V_{IH}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA | - | 3 | - | 3 | - | 3 | mA |
| Average Operating Current | I _{CC1} | Cycle time = 1us, 100% duty, I _{IO} = 0mA, $\overline{\text{CE}} \leq 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | - | 5 | - | 5 | - | 5 | mA |
| | I _{CC2} | Cycle time = min, 100% duty, I _{IO} = 0mA, $\overline{\text{CE}} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} | - | 45 | - | 40 | - | 30 | mA |
| Standby Power Supply Current (TTL Level) | I _{SB} | $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{LB}} = \overline{\text{UB}} = V_{IH}$ other input = V _{IL} or V _{IH} | - | 0.3 | - | 0.3 | - | 0.3 | mA |
| Standby Power Supply Current (CMOS Level) | I _{SB1} | $\overline{\text{CE}} \geq V_{CC} - 0.2V$ or $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2V$, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} - 0.2V | - | 2 | - | 2 | - | 2 | uA |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1mA | - | 0.4 | - | 0.4 | - | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -1.0 mA | 2.2 | - | 2.2 | - | 2.2 | - | V |

CAPACITANCE

(f = 1 MHz, Ta = 25°C,)

| PARAMETER | SYMBOL | CONDITION | MAX. | UNIT |
|---------------------------|-----------|-------------------------|------|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0V$ | 8 | pF |
| Input/ Output Capacitance | $C_{I/O}$ | $V_{IN} = V_{OUT} = 0V$ | 10 | pF |

Note: This parameter is guaranteed by device characterization and is not production tested.

AC TEST CONDITIONS

| PARAMETER | CONDITIONS |
|---|---|
| Input Pulse Levels | 0.6V to 2.1V |
| Input Rise and Fall Times | 3.0 ns |
| Input and Output Timing Reference Level | 1.4V |
| Output Load | $C_L = 30pF + 1TTL$ Load(55ns/70ns) |
| | $C_L = 100pF + 1TTL$ Load(Load for 100ns) |

AC TEST LOADS AND WAVEFORM

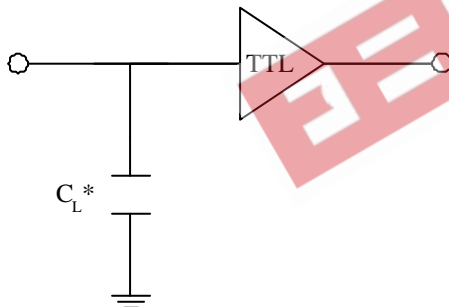


Fig.A * Including Scope and Jig Capacitance

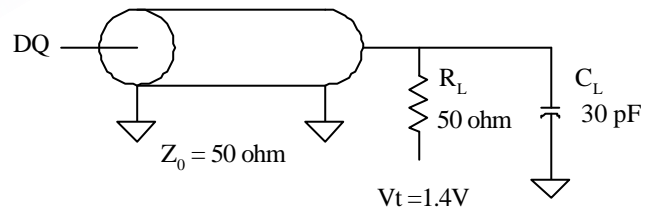


Fig.B Output Load Equivalent

AC CHARACTERISTICS($v_{cc}=2.7$ to $3.6V$, $v_{SS} = 0V$, $T_a = -40^{\circ}C$ to $85^{\circ}C$)

(1) READ CYCLE

| PARAMETER | SYM. | -55 | | -70 | | -100 | | UNIT |
|---|-----------|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t_{RC} | 55 | - | 70 | - | 100 | - | ns |
| Address Access Time | t_{AA} | - | 55 | - | 70 | - | 100 | ns |
| Chip Enable Access Time | t_{ACE} | - | 55 | - | 70 | - | 100 | ns |
| Output Enable Access Time | t_{OE} | - | 30 | - | 35 | - | 50 | ns |
| Output Hold from Address Change | t_{OH} | 10 | - | 10 | - | 10 | - | ns |
| Chip Enable to Output in Low-Z | t_{LZ} | 10 | - | 10 | - | 10 | - | ns |
| Chip Disable to Output in High-Z | t_{HZ} | - | 20 | - | 25 | - | 30 | ns |
| Output Enable to Output in Low-Z | t_{OLZ} | 5 | - | 5 | - | 5 | - | ns |
| Output Disable to Output in High-Z | t_{OHZ} | - | 20 | - | 25 | - | 30 | ns |
| \overline{LB} , \overline{UB} Access Time | t_{BA} | - | 30 | - | 35 | - | 50 | ns |
| \overline{LB} , \overline{UB} Enable to Output in Low-Z | t_{BLZ} | 5 | - | 5 | - | 5 | - | ns |
| \overline{LB} , \overline{UB} Disable to Output in High-Z | t_{BHZ} | - | 20 | - | 25 | - | 30 | ns |

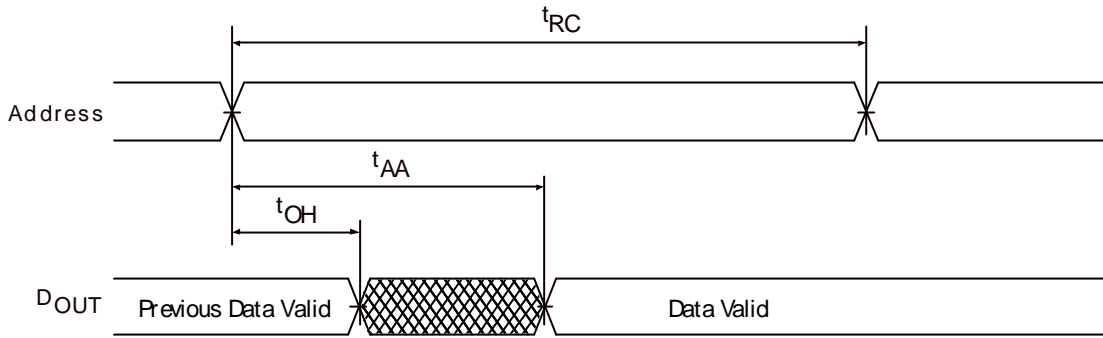
(2)WRITE CYCLE

| PARAMETER | SYM. | -55 | | -70 | | -100 | | UNIT |
|----------------------------------|-----------|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t_{WC} | 55 | - | 70 | - | 100 | - | ns |
| Chip Enable to Write End | t_{CW} | 50 | - | 60 | - | 80 | - | ns |
| Address Valid to Write End | t_{AW} | 50 | - | 60 | - | 80 | - | ns |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | t_{WP} | 45 | - | 50 | - | 70 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | 0 | - | ns |
| Data Valid to Write End | t_{DW} | 25 | - | 30 | - | 40 | - | ns |
| Data Hold Time | t_{DH} | 0 | - | 0 | - | 0 | - | ns |
| Write Enable to Output in High-Z | t_{WHZ} | - | 20 | - | 25 | - | 30 | ns |
| Output Active from Write End | t_{OW} | 5 | - | 5 | - | 5 | - | ns |

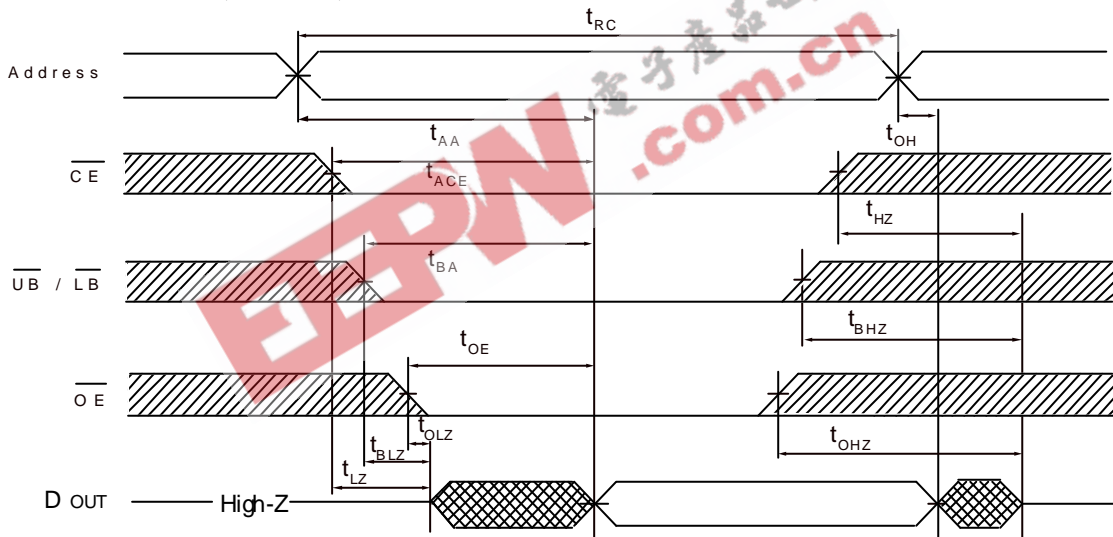
TIMING WAVEFORMS

READ CYCLE 1

(Address Controlled, $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{LB} or/and $\overline{UB} = V_{IL}$)



READ CYCLE 2 ($\overline{WE} = V_{IH}$)



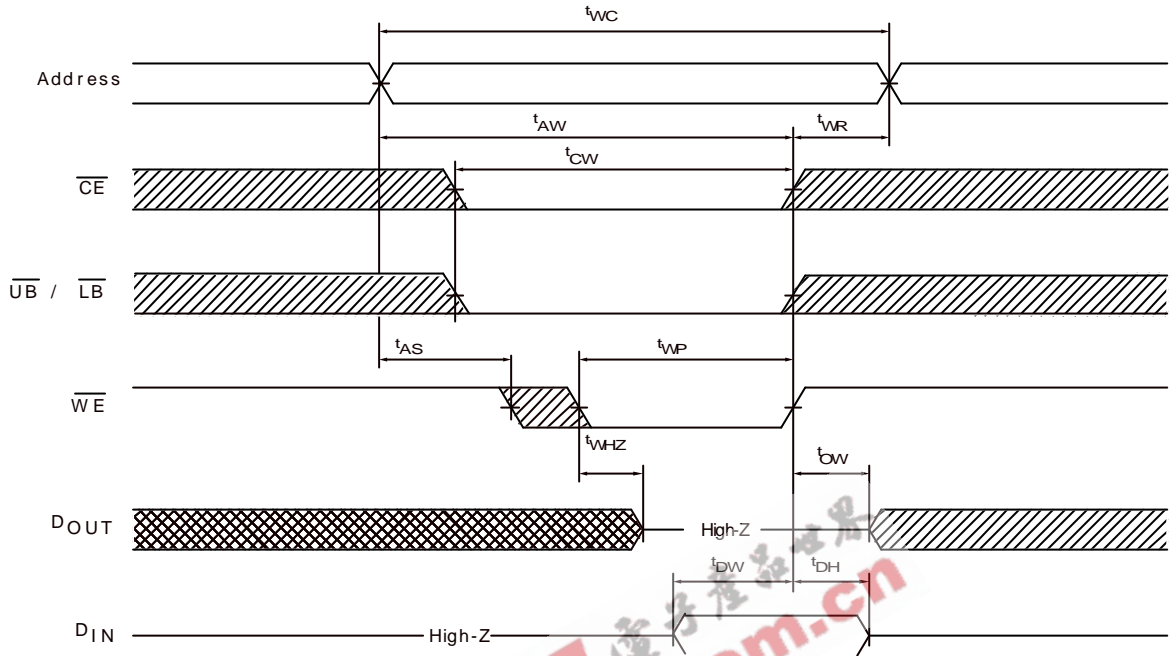
 DON'T CARE
 UNDEFINED

(Chip Enable Controlled)

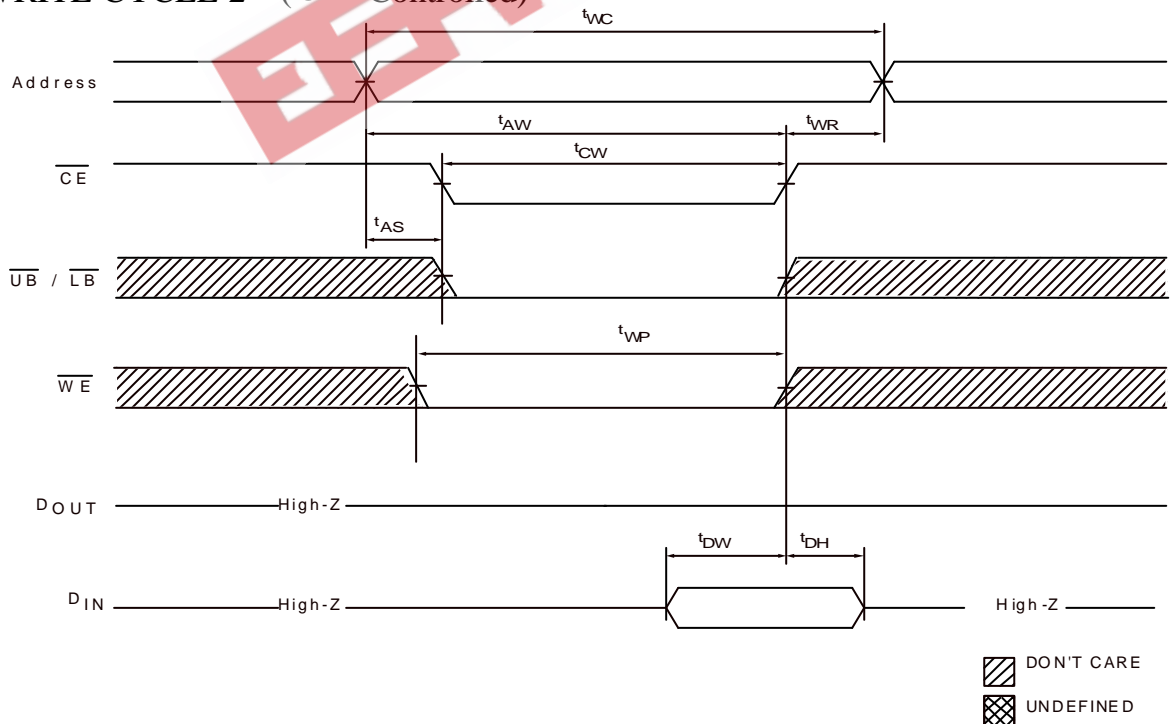
Notes (READ CYCLE) :

1. \overline{WE} are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition. t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device interconnection.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CE} = V_{IL}$.

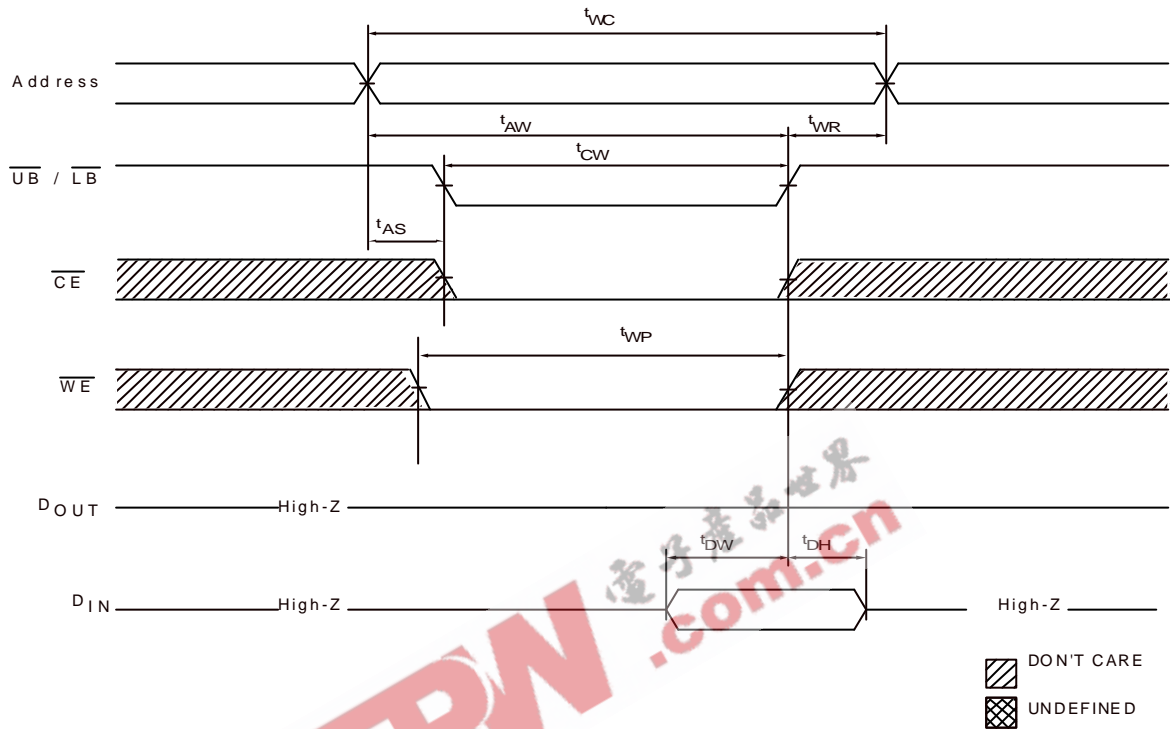
WRITE CYCLE 1 (\overline{WE} Controlled)



WRITE CYCLE 2 (\overline{CE} Controlled)



WRITE CYCLE 3 (UB, LB Controlled)



NOTES (WRITE CYCLE) :

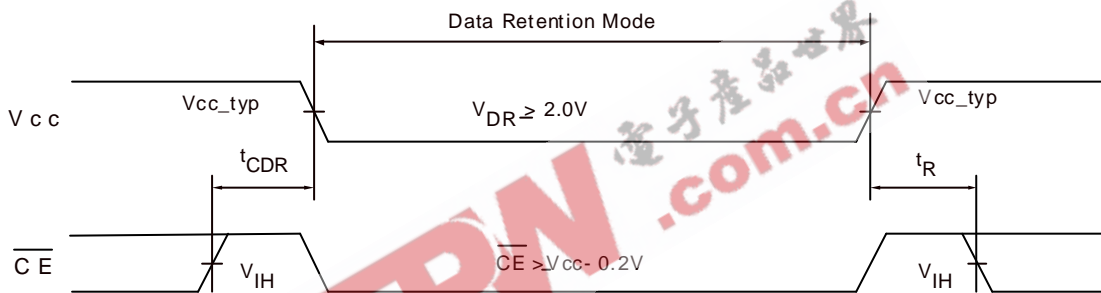
1. A write occurs during the overlap of a low \overline{CE} , a low \overline{WE} . A write begins at the latest transition among \overline{CE} goes low, \overline{WE} going low. A write end at the earliest transition among \overline{CE} going high, \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of \overline{CE} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.

DATA RETENTION CHARACTERISTICS

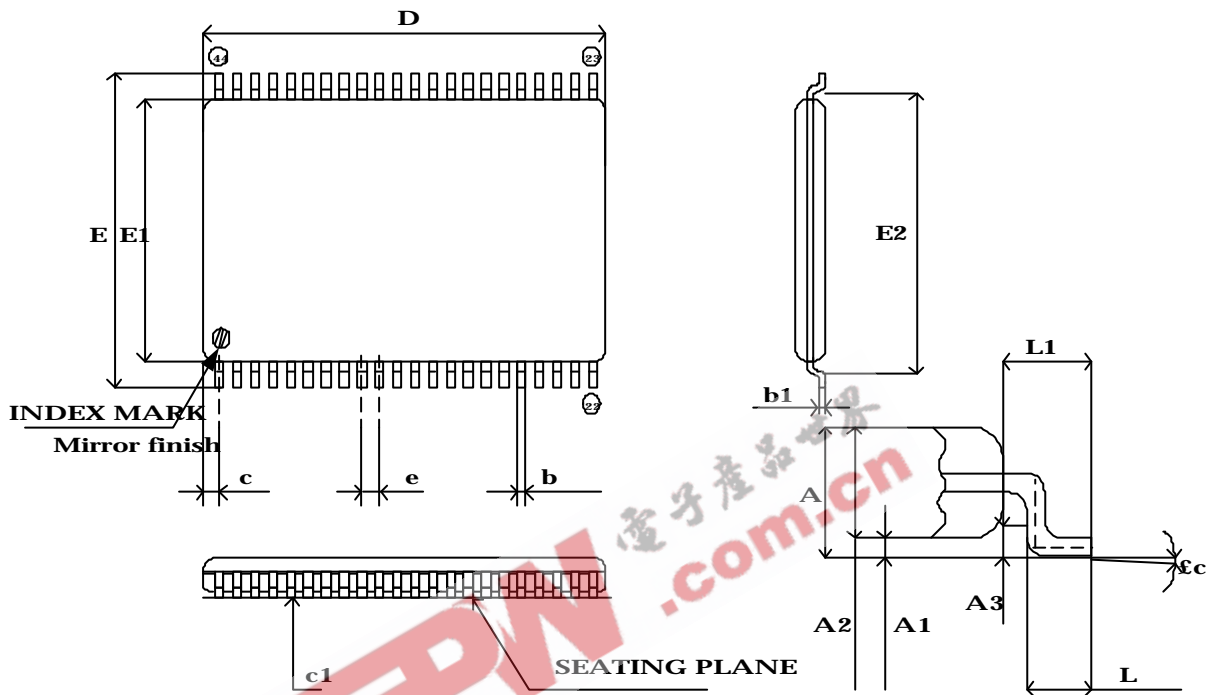
| PARAMETER | SYM. | TEST CONDITION | MIN. | MAX. | UNIT |
|--------------------------------------|-------------------|--|-----------------|------|------|
| V _{CC} for Data Retention | V _{DR} | $\overline{CE} \geq V_{CC} - 0.2V$ | 2.0 | - | V |
| Data Retention Current | I _{CCDR} | $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | - | 3 | uA |
| Chip Deselect to Data Retention Time | t _{CDR} | | 0 | - | ns |
| Operation Recovery Time | t _R | | t _{RC} | - | ns |

DATA RETENTION WAVEFORM

(T_a = -40°C to 85°C)



PACKAGE DIMENSIONS
44-LEAD TSOP-II



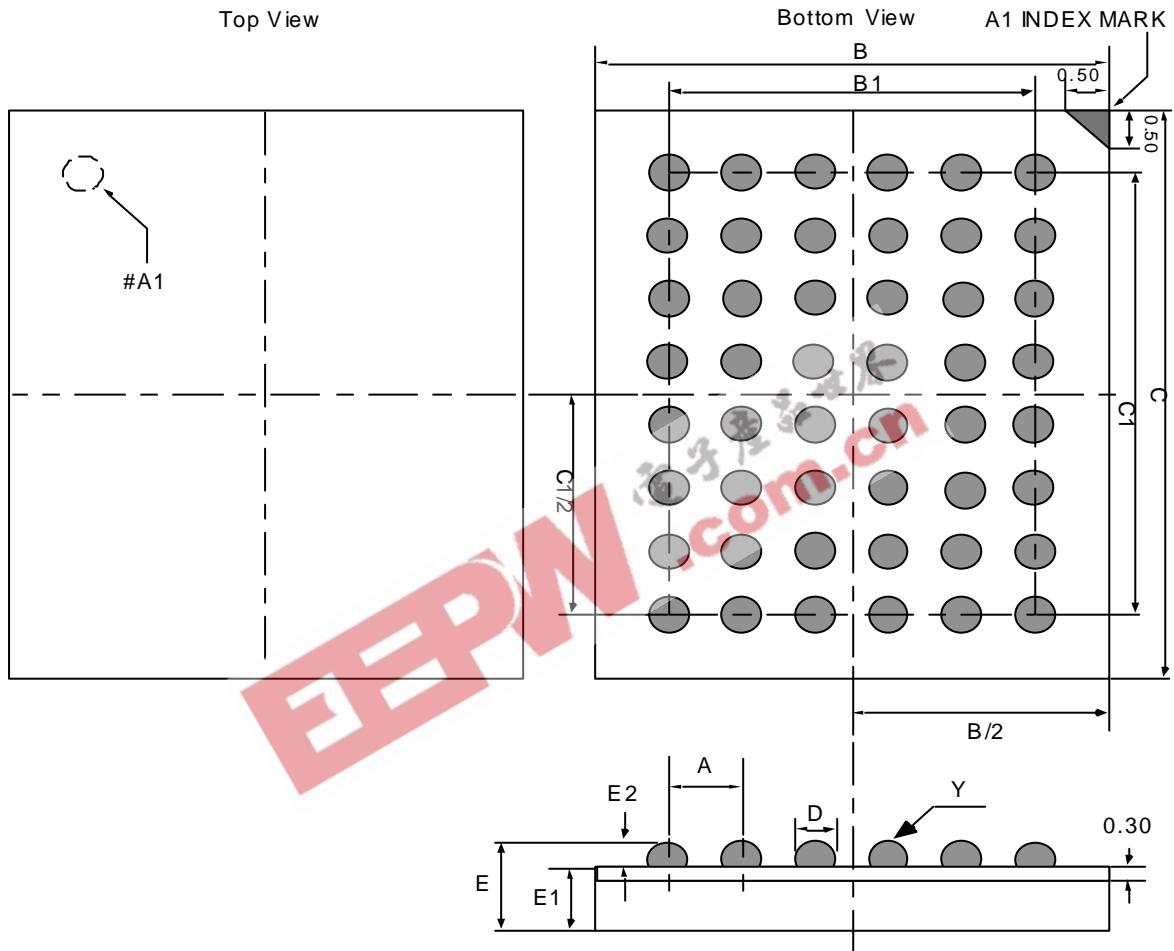
| Symbol | Dimension in mm | | | Dimension in inch | | |
|--------|-----------------|-----------|-------|-------------------|------------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 1.20 | - | - | 0.047 |
| A1 | 0.05 | - | 0.1 | 0.002 | - | 0.004 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| A3 | - | 0.25 | - | - | 0.010 | - |
| b | - | 0.35(typ) | - | - | 0.014(typ) | - |
| b1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| c | - | 0.805 | - | - | 0.032 | - |
| c1 | - | 0.10 | - | - | 0.004 | - |
| D | 18.31 | 18.41 | 18.51 | 0.721 | 0.725 | 0.729 |
| e | - | 0.80(typ) | - | - | 0.031(typ) | - |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.394 | 0.400 | 0.405 |
| E2 | - | 10.76 | - | - | 0.458 | - |
| L | 0.4 | 0.5 | 0.6 | 0.016 | 0.020 | 0.024 |
| L1 | - | 0.8(typ) | - | - | 0.032(typ) | - |
| θ | 0 | - | 8 | 0 | - | 8 |

PACKAGE DIMENSIONS

Units : millimeters

48-pin CSP (8 row x 6 column)

48 BALL FINE PITCH BGA (0.75mm ball pitch)



| Symbol | min | typ | max |
|--------|------|------|------|
| A | - | 0.75 | - |
| B | 5.95 | 6.00 | 6.05 |
| B1 | - | 3.75 | - |
| C | 7.95 | 8.00 | 8.05 |
| C1 | - | 5.25 | - |
| D | 0.25 | 0.30 | 0.35 |
| E | - | 1.10 | 1.20 |
| E1 | - | 0.95 | - |
| E2 | 0.20 | 0.25 | 0.30 |
| Y | - | - | 0.08 |

Notes :

1. Bump counts : 48 (8 row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75) typ.
3. All tolerance are ± 0.050 unless otherwise specified.
4. 'Y' is coplanarity : 0.08(max)
5. Units : mm