DRAM

64K x 16 DYNAMIC RAM

FAST PAGE MODE

FEATURES

- High speed access time : 25/30/35/40 ns
- Industry-standard x 16 pinouts and timing functions.
- Single 5V (±10%) power supply.
- All device pins are TTL- compatible.
- 256-cycle refresh in 4ms.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ BEFORE $\overline{RAS}$ (CBR) and HIDDEN.
- Conventional FAST PAGE MODE access cycle.
- BYTE WRITE and BYTE READ access cycles.

PART NUMBER EXAMPLES

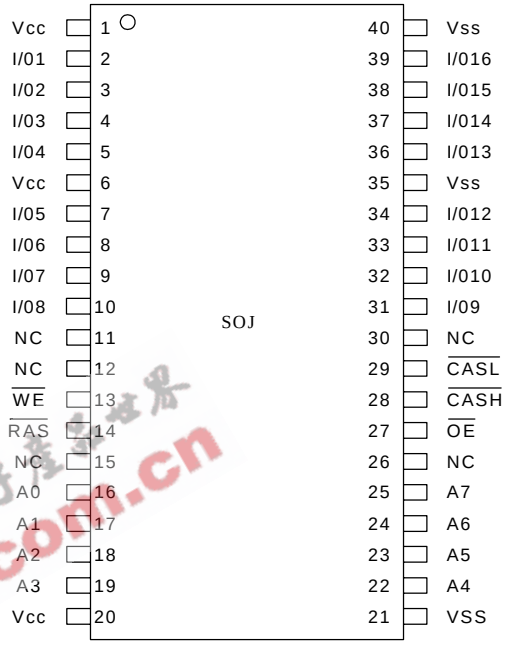
PART NUMBER	ACCESS TIME	PACKAGE
T221160A-30J	30ns	SOJ
T221160A-30S	30ns	TSOP-II
T221160A-35J	35ns	SOJ
T221160A-35S	35ns	TSOP-II

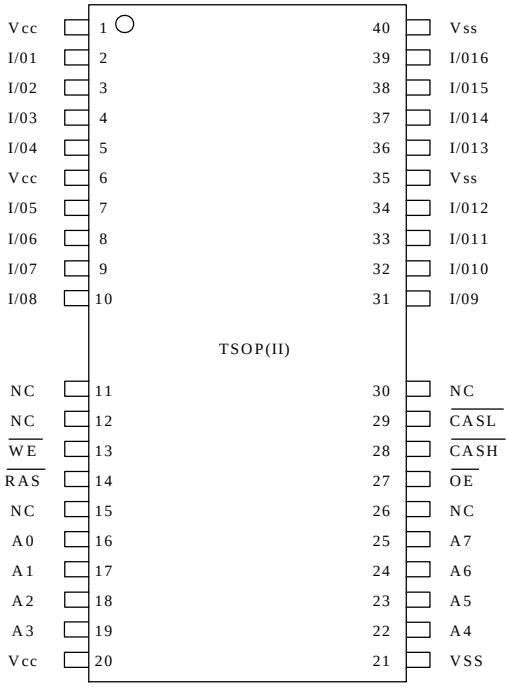
GENERAL DESCRIPTION

The T221160A is a randomly accessed solid state memory containing 1,048,551 bits organized in a x16 configuration. The T221160A has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. It offers Fast Page mode operation

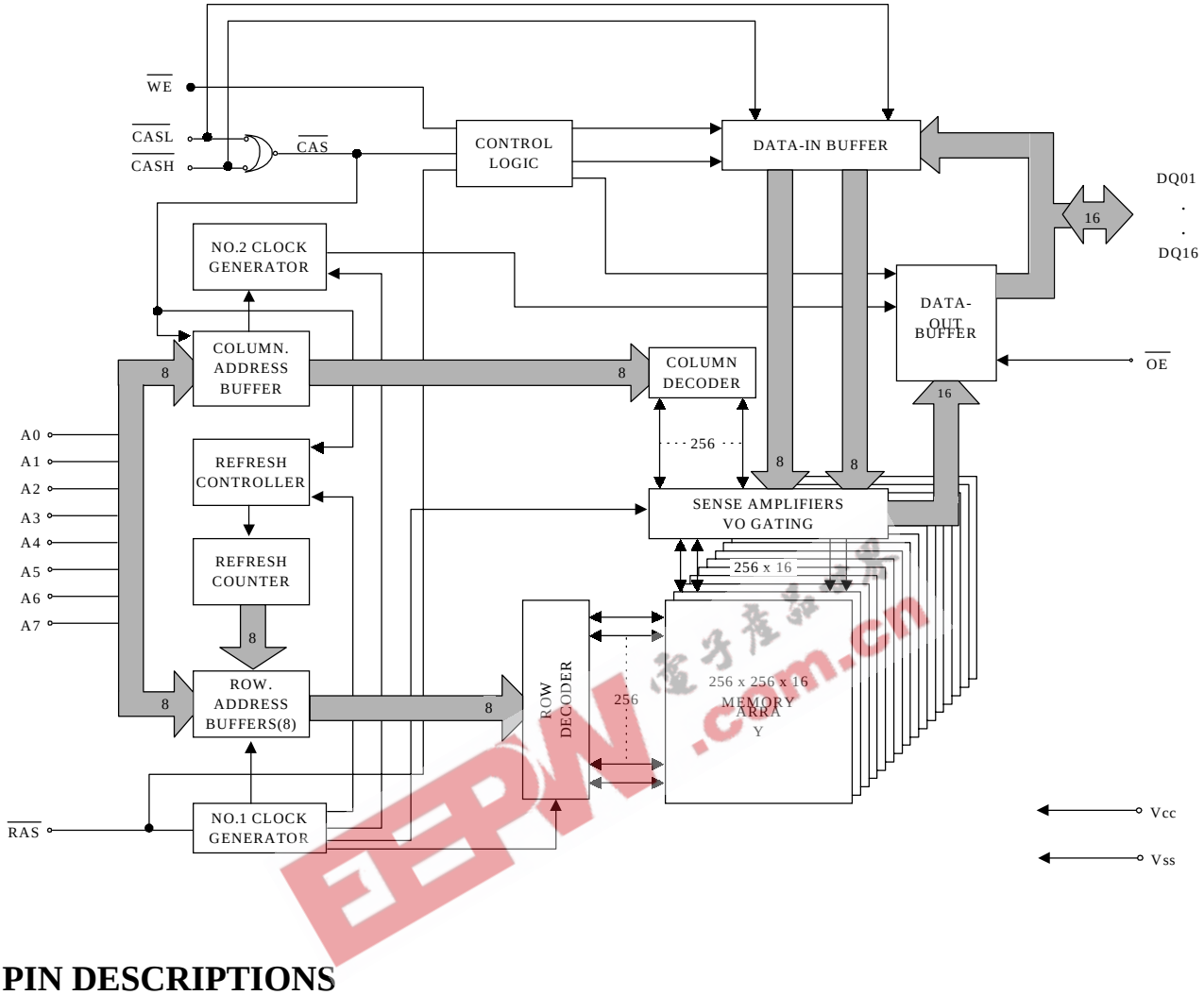
The T221160A $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ to transition low and by the last to transition back high. Use only one of the two $\overline{CAS}$ and leave the other staying high during WRITE will result in a BYTE WRITE. $\overline{CASL}$ transiting low in a WRITE cycle will write data into the lower byte (IO1~IO8), and $\overline{CASH}$ transiting low will write data into the upper byte (IO9~16).

PIN ASSIGNMENT (Top View)





FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~25	A0-A7	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe /Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe /Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,6~10,31~34,36~39	I/O1 - I/O16	Input/ Output	Data Input/ Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any pin Relative to VSS… … -1V to 7V

Operating Temperature, Ta (ambient)..0°C to +70°C

Storage Temperature (plastic)…..... -55°C to +150°C

Power Dissipation .....…..... 1.0W

Short Circuit Output Current.....…..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ Ta ≤ 70°C; VCC = 5V ± 10 % unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM.	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Supply Voltage		Vss	0	0	V	
Input High (Logic) voltage		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic) voltage		V_{IL}	-1.0	0.8	V	1
Input Leakage Current	$0V \le V_{IN} \le 7V$	I_{LI}	-10	10	uA	
Output Leakage Current	$0V \le V_{OUT} \le 7V$ Output(s) disabled	I_{LO}	-10	10	uA	
Output High Voltage	I_{OH} = -5 mA	V_{OH}	2.4	-	V	
Output Low Voltage	I_{OL} = 4.2 mA	V_{OL}	-	0.4	V	

Note: 1.All Voltages referenced to Vss

DC CHARACTERISTICS

(Ta = 0 to 70°C, Vcc = 5V ±10%, Vss = 0V)

Parameter	Symbol	-25		-30		-35		-40		Unit	Test Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating Current	Icc1	-	170	-	150	-	130	-	120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=min
Standby Current	Icc2	-	4	-	4	-	4	-	4	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ =V_{IH}, D_{OUT}=High-Z
Standby Current	Icc3	-	2	-	2	-	2	-	2	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ > Vcc-0.2V
Fast Page Mode Current	Icc4	-	170	-	150	-	130	-	120	mA	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling, t_{PC}= min
$\overline{RAS}$ -only refresh Current	Icc5	-	170	-	150	-	130	-	120	mA	$\overline{CAS}$ =VIH, $\overline{RAS}$ cycling, t_{RC}= min
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	Icc6	-	170	-	150	-	130	-	120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC}= min

Note: Icc depends on output load condition when the device is selected.
Icc max is specified at the output open condition, Icc is specified as an average current.

CAPACITANCE

(Ta =25°C, Vcc =5V, f = 1M HZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (address)	C_{I1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	-	7	pF
Output Capacitance (data-in/out)	$C_{I/O}$	-	10	pF

AC CHARACTERISTICS (note 1,2,3) (Ta = 0 to 70°C)

AC TEST CONDITIONS:
Vcc=5V ±10%, input pulse level = 0 to 3V
Input rise and fall times: 2ns
Output Load: 2TTL gate + C_L (50pF)

AC CHARACTERISTICS PARAMETER	SYM	-25		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t_{RC}	43		55		65		75		ns	
Read-Modify-Write Cycle Time	t_{RWC}	65		85		95		105		ns	
Fast-Page-Mode Read or Write Cycle Time	t_{PC}	15		20		23		25		ns	
Fast-Page-Mode Read-Write Cycle Time	t_{PCM}	37		42		49		52		ns	
Access Time From $\overline{RAS}$	t_{RAC}		25		30		35		40	ns	4
Access Time From $\overline{CAS}$	t_{CAC}		7		8		9		10	ns	5
Access Time From $\overline{OE}$	t_{OAC}		7		8		9		10	ns	13
Access Time From Column Address	t_{AA}		12		16		18		20	ns	8
Access Time From $\overline{CAS}$ Precharge	t_{ACP}		14		18		20		22	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	25	10K	30	10K	35	10K	40	10K	ns	
$\overline{RAS}$ Pulse Width	t_{RASC}	25	100K	30	100K	35	100K	40	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	7		8		9		10		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	15		20		23		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	4	10K	6	10K	8	10K	10	10K	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	21		26		30		35		ns	
$\overline{CAS}$ Precharge Time	t_{CP}	3		3		4		5		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	10	17	10	21	10	25	10	29	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	3		3		3		5		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	5		5		5		5		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	8	13	8	14	8	16	8	18	ns	8
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	4		4		4		5		ns	
Column Address Hold Time (Reference to $\overline{RAS}$)	t_{AR}	22		26		30		34		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	12		14		16		18		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	14
Read Command Hold Time Reference to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9,14
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	3		3		3		3		ns	
Output Buffer Turn-off Delay From $\overline{CAS}$ or $\overline{RAS}$	t_{OFF1}	3	15	3	15	3	15	3	15	ns	10,16

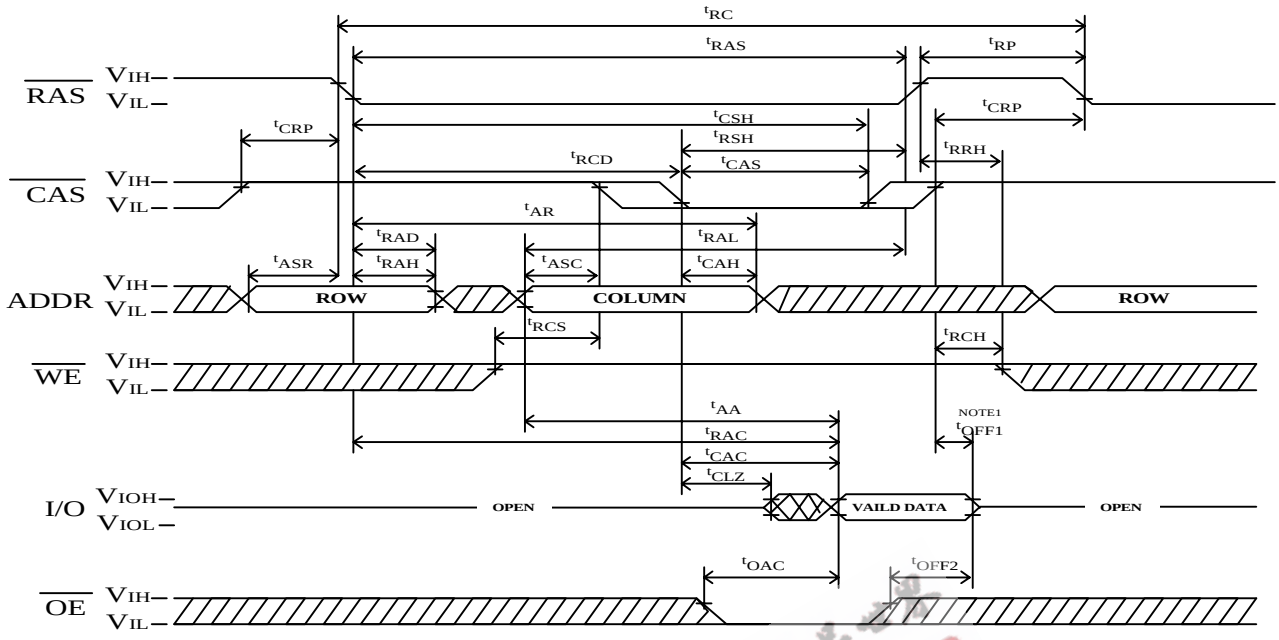
AC CHARACTERISTICS (continued)

AC CHARACTERISTICS PARAMETER	SYM	-25		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output Buffer Turn-off $\overline{OE}$ to	t_{OFF2}	-	6	-	8	-	8	-	8	ns	16
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	11,14
Write Command Hold Time	t_{WCH}	4		4		4		6		ns	
Write Command Hold Time (Reference to $\overline{RAS}$)	t_{WCR}	22		26		30		34		ns	14
Write Command Pulse Width	t_{WP}	4		4		4		6		ns	14
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	5		6		7		9		ns	14
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	5		6		7		8		ns	14
Data-in Setup Time	t_{DS}	0		0		0		0		ns	12
Data-in Hold Time	t_{DH}	4		4		4		5		ns	12
Data-in Hold Time (Reference to $\overline{RAS}$)	t_{DHR}	22		26		30		34		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	34		46		51		56		ns	11
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	21		29		31		35		ns	11
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	17		24		25		27		ns	11
Transition Time (rise or fall)	t_T	1.5	50	1.5	50	2.5	50	2.5	50	ns	2,3
Refresh Period (256 cycles)	t_{REF}		4		4		4		4	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	10		10		10		10		ns	
$\overline{CAS}$ Setup Time (CBR REFRESH)	t_{CSR}	5		10		10		10		ns	6
$\overline{CAS}$ Hold Time (CBR REFRESH)	t_{CHR}	7		10		10		10		ns	6
$\overline{OE}$ Hold Time From $\overline{WE}$ During Read-Modify-Write Cycle	t_{OEH}	4		4		4		5		ns	15
$\overline{OE}$ Setup Prior to $\overline{RAS}$ During Hidden Refresh Cycle	t_{ORD}	0		0		0		0		ns	

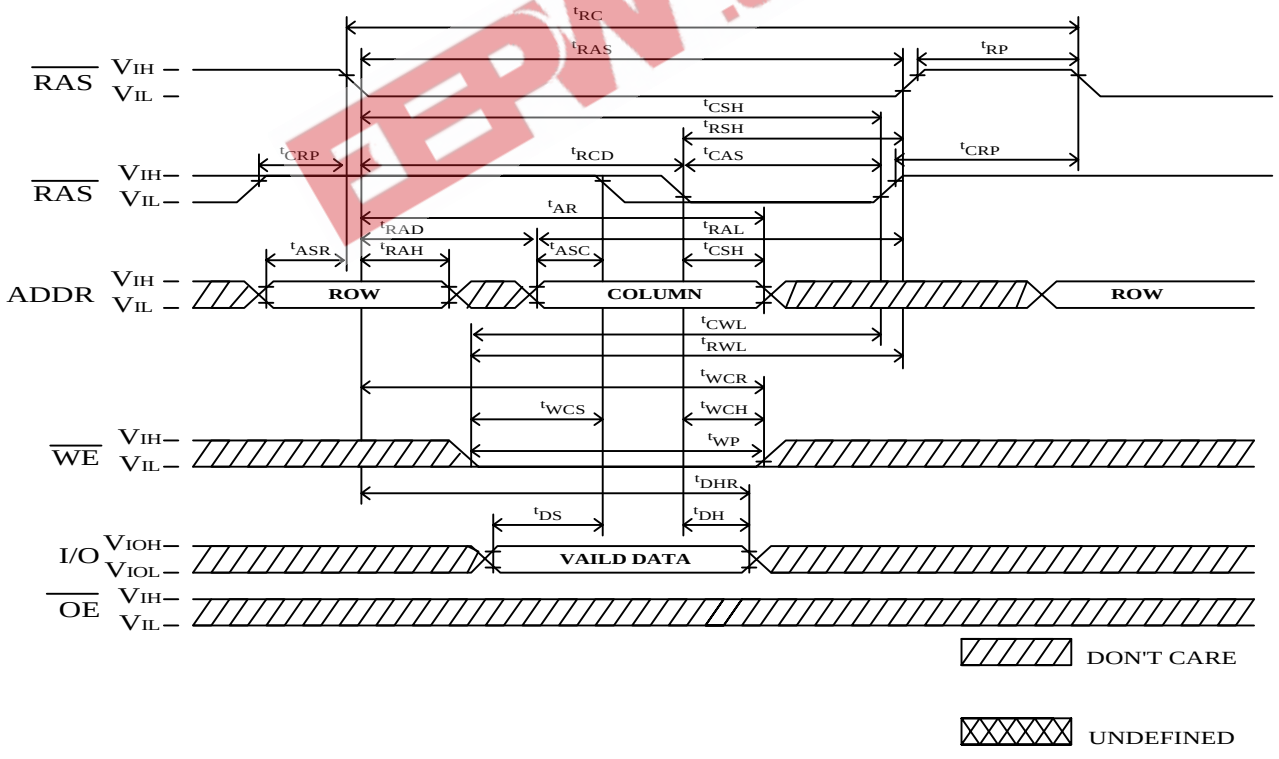
Notes:

1. An initial pause of 200us is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH}(2.4V) and V_{IL}(0.8V) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(2.4V) and V_{IL}(0.8V).
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD}$(max) .
6. Enables on-chip refresh and address counters.
7. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled by t_{CAC}.
8. Operation within the t_{RAD} limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is controlled by t_{AA}.
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. t_{OFF1}(max) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
11. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CWD} \geq t_{CWD}$(min), the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held high and $\overline{WE}$ taken low after $\overline{CAS}$ goes low result in a LATE WRITE ($\overline{OE}$ -controlled) cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if $\overline{OE}$ is low then taken HIGH before $\overline{CAS}$ goes high, I/O goes open, if $\overline{OE}$ is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. WRITE command is defined as $\overline{WE}$ going low.
15. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OFF2} and t_{OEH} met ($\overline{OE}$ high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
16. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.

READ CYCLE

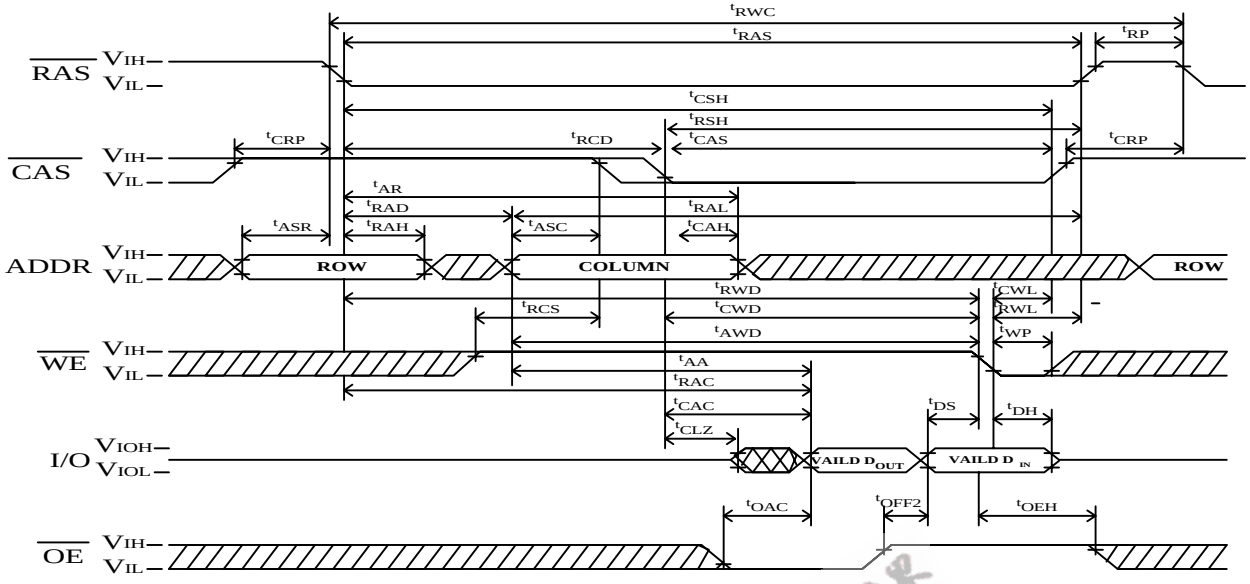


EARLY WRITE CYCLE

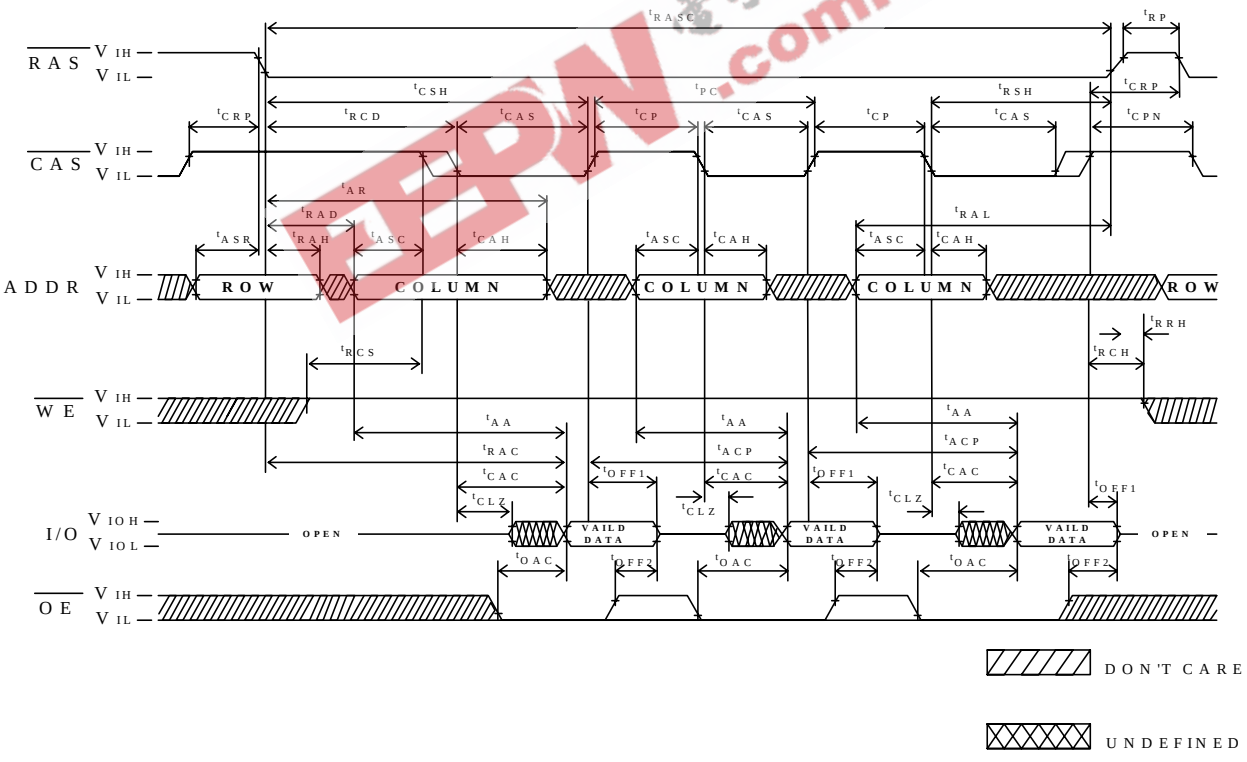


Note: t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



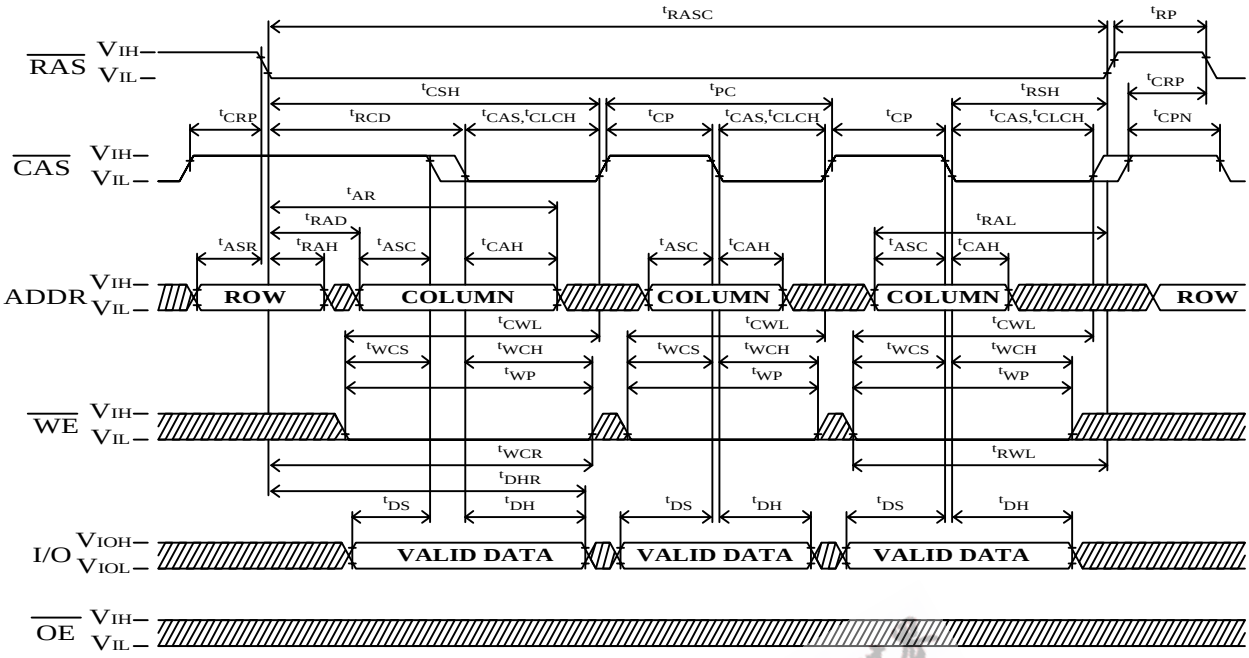
FAST-PAGE-MODE READ CYCLE



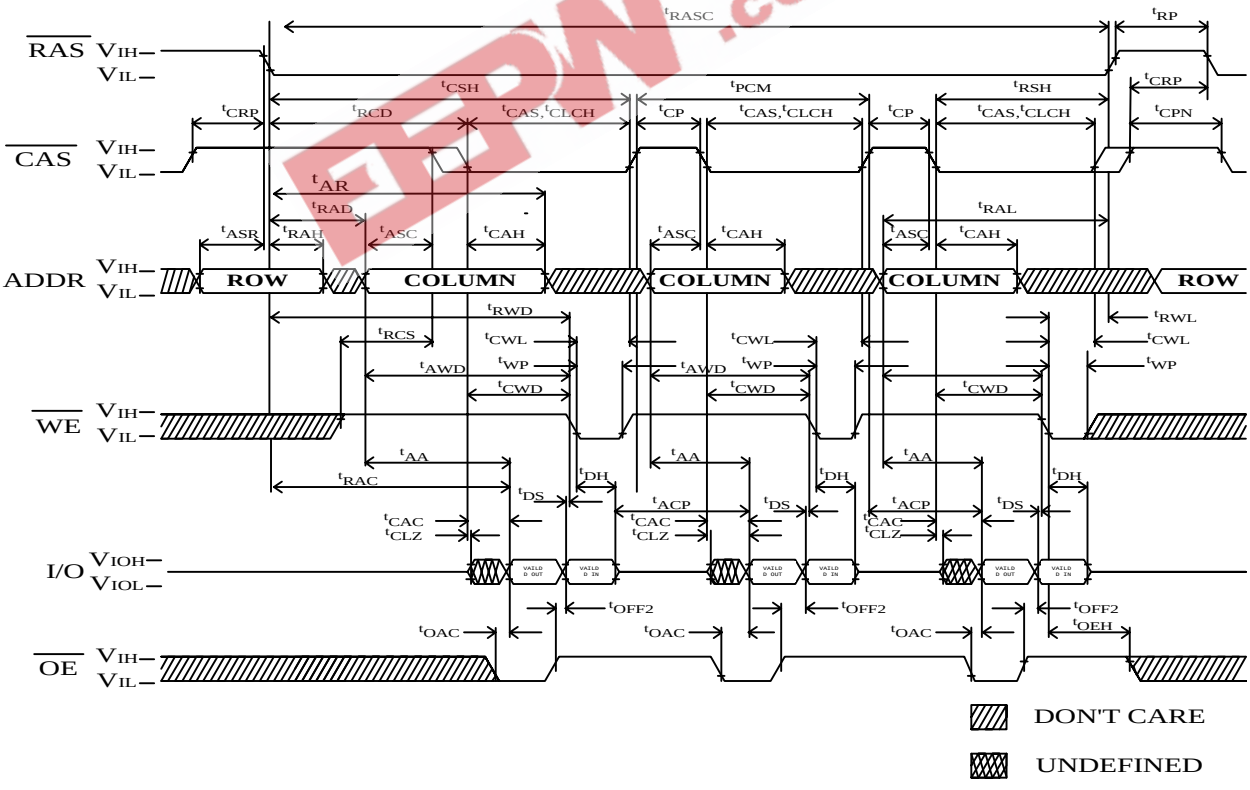
Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

2. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

FAST-PAGE-MODE EARLY-WRITE CYCLE



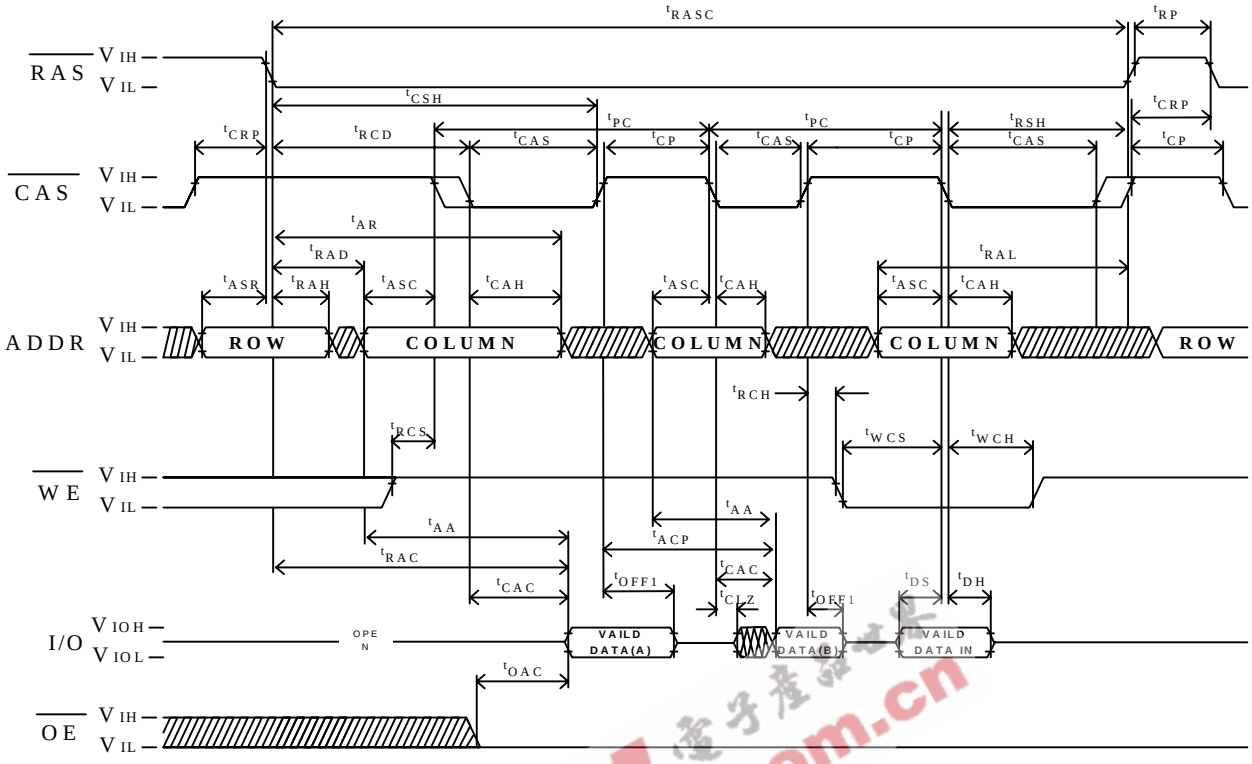
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



Note: t_{PC} can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

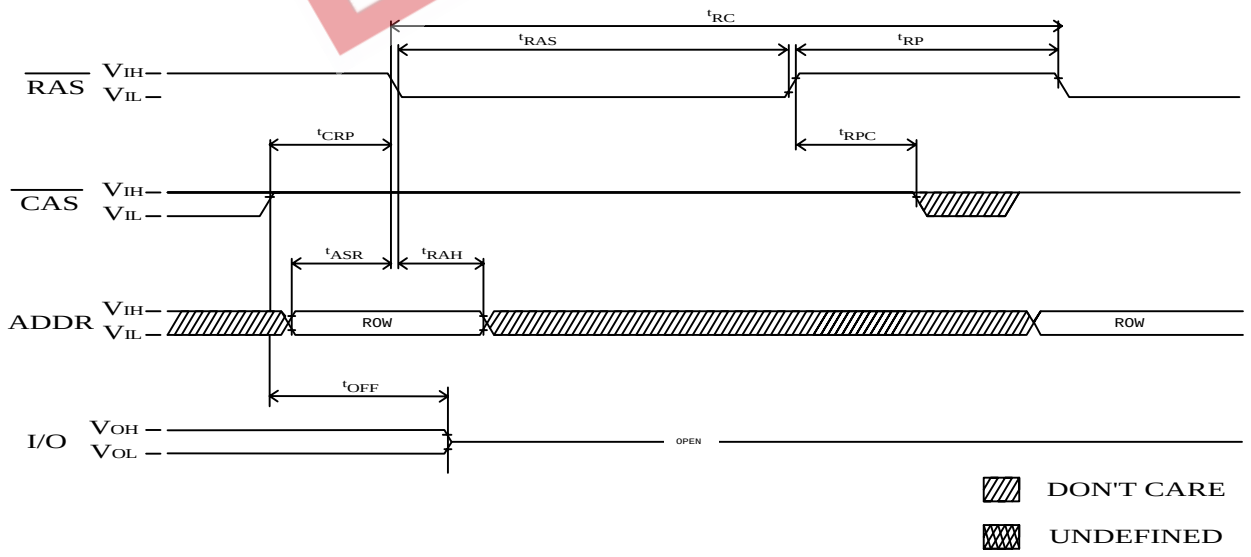
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



RAS ONLY REFRESH CYCLE

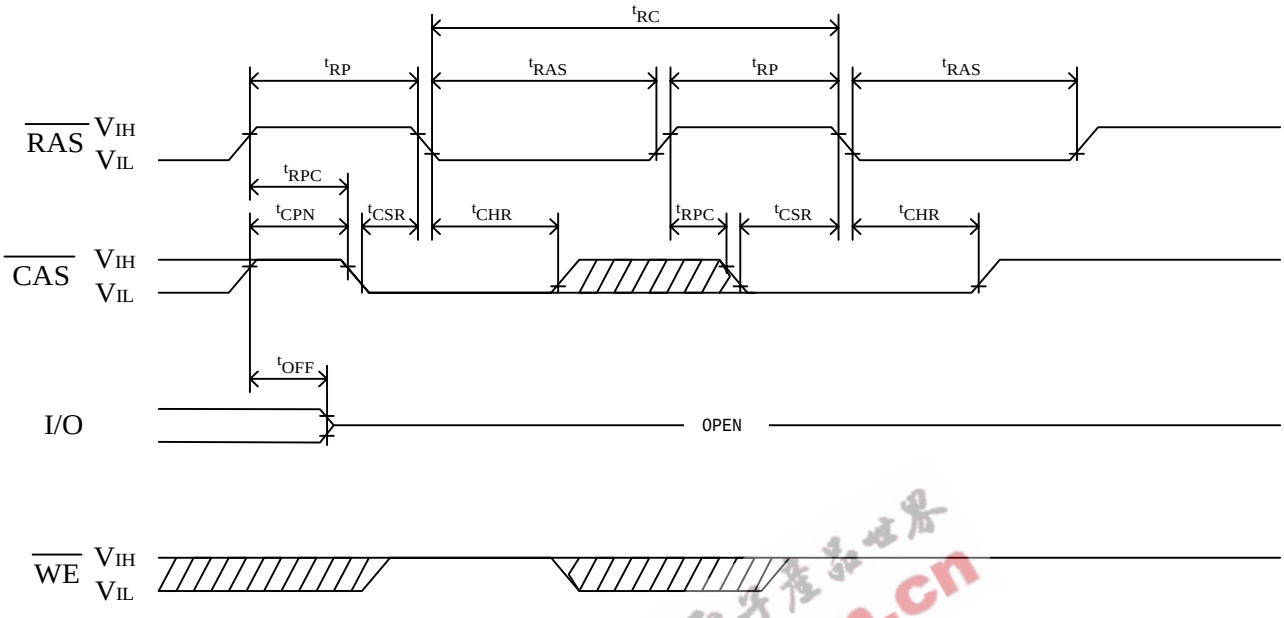
(ADDR=A0-A7 ; OE, WE =DON'T CARE)



Note1:Do not drive data prior to tristate.

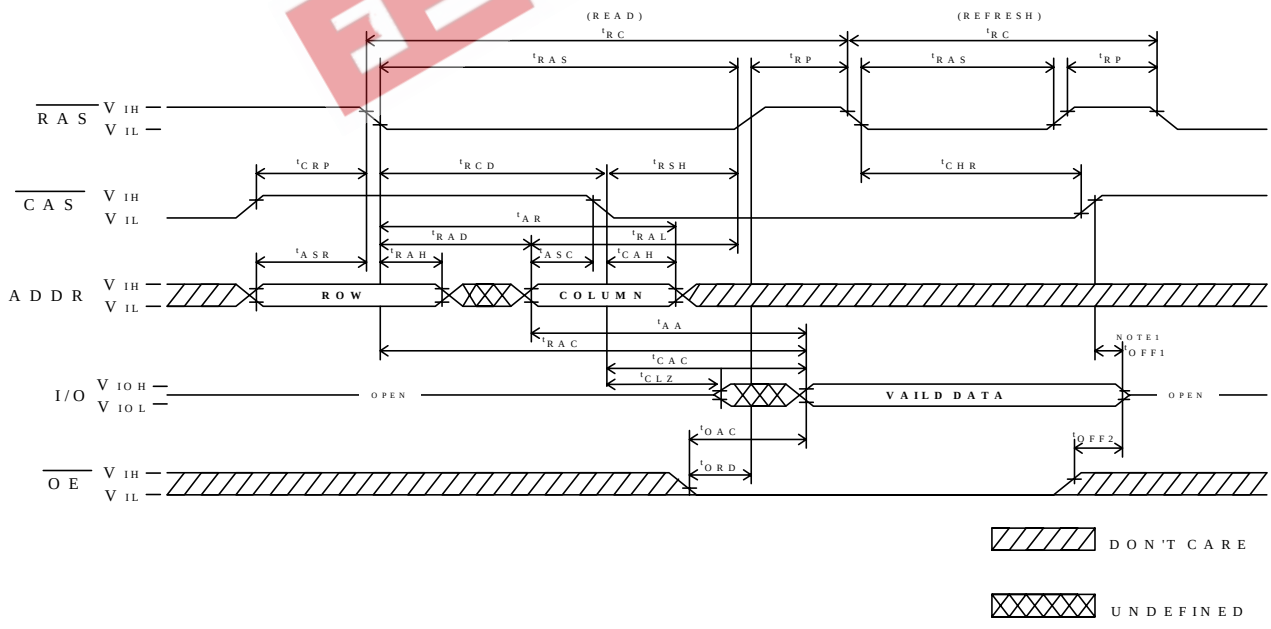
CBR REFRESH CYCLE

(A0-A7 ; $\overline{OE}$ =DON'T CARE)



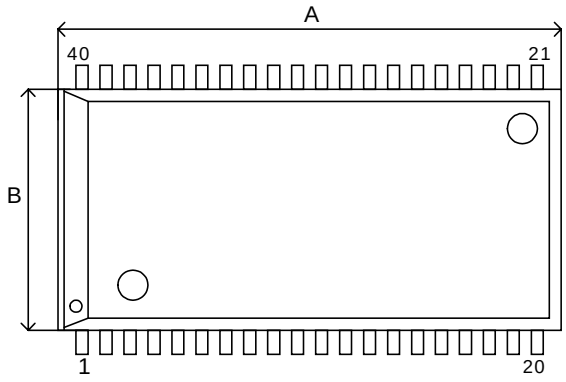
HIDDEN REFRESH CYCLE

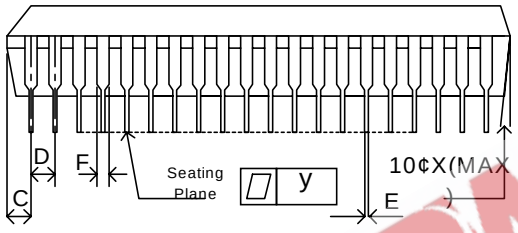
($\overline{WE}$ =HIGH ; $\overline{OE}$ =LOW)

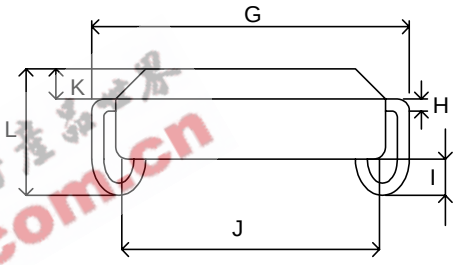


Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

PACKAGE DIMENSIONS
40-LEAD SOJ DRAM (400 mil)

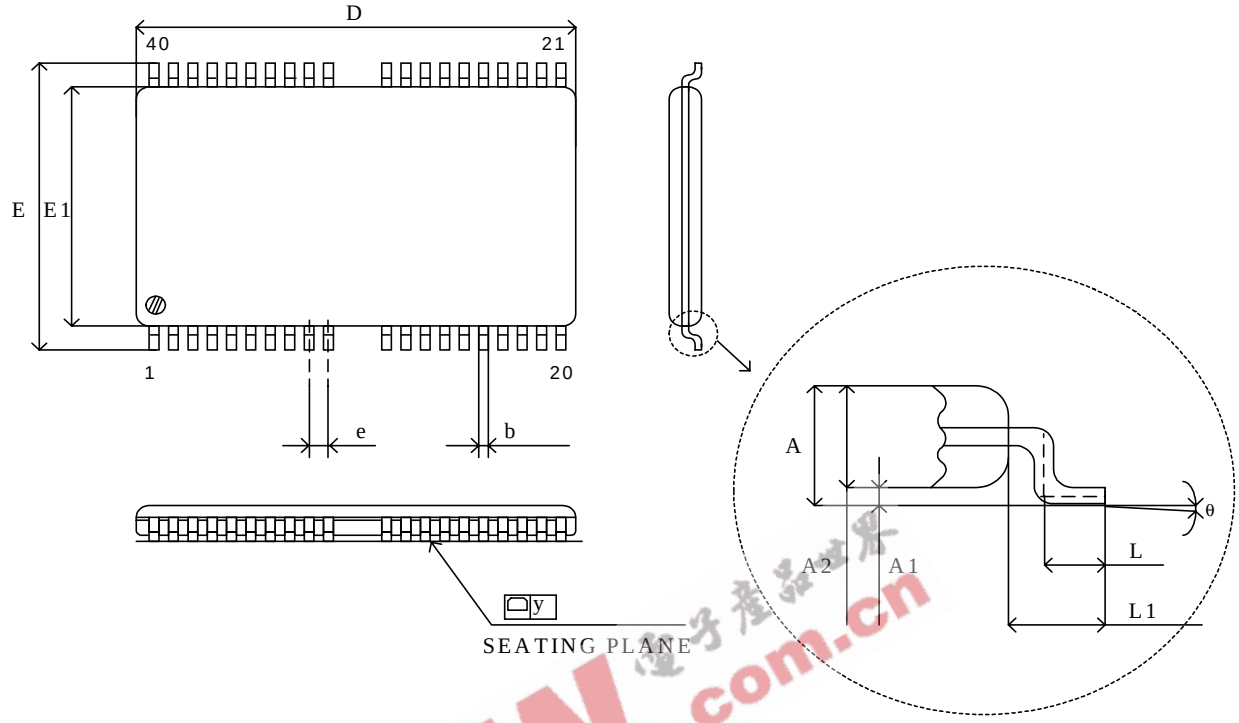






SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	1.025±0.010	26.035±0.254
B	0.400±0.005	10.160±0.127
C	0.045(MAX)	1.143(MAX)
D	0.050±0.006	1.27±0.152
E	0.019±0.003	0.483±0.08
F	0.026±0.003	0.661±0.080
G	0.440±0.010	11.176±0.254
H	0.011±0.003	0.280±0.080
I	0.025(MIN)	0.635(MIN)
J	0.364±0.020	9.246±0.508
K	0.047±0.006	1.194±0.152
L	0.150(MAX)	3.810(MAX)
y	0.004(MAX)	0.102(MAX)

PACKAGE DIMENSIONS
40-LEAD TSOP II DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max)	1.20(max)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.014(typ.)	0.35(typ.)
e	0.0315(typ.)	0.80typ.)
D	0.725±0.004	18.41±0.10
E	0.463±0.008	11.76±0.20
E1	0.400±0.004	10.16±0.10
L1	0.031	0.80
L	0.020±0.004	0.500±0.10
y	0.004(max)	0.10(max)
θ	0°~5°	0°~5°