



T4 Series

SNUBBERLESS™ & LOGIC LEVEL

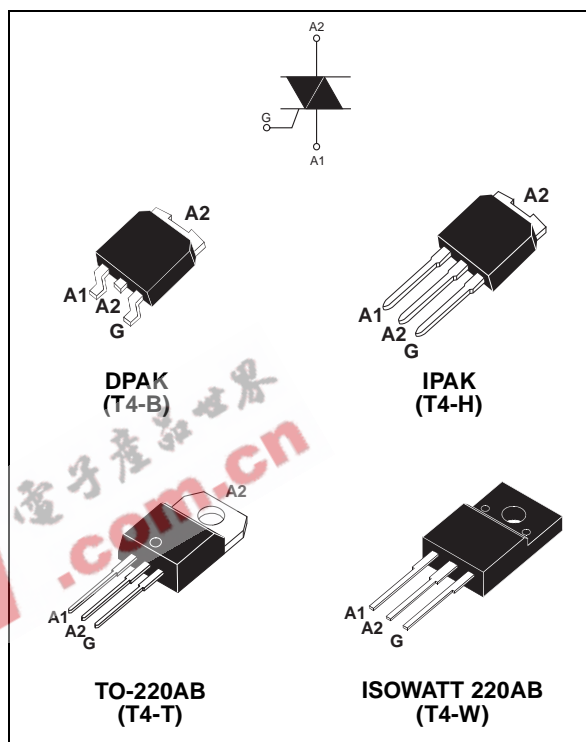
4A TRIACs

MAIN FEATURES:

| Symbol | Value | Unit |
|-------------------|------------|------|
| $I_{T(RMS)}$ | 4 | A |
| V_{DRM}/V_{RRM} | 600 to 800 | V |
| $I_{GTT} (Q_1)$ | 5 to 35 | mA |

DESCRIPTION

Based on ST's Snubberless / Logic level technology providing high commutation performances, the T4 series is suitable for use on AC inductive loads. They are recommended for applications using universal motors, electrovalves.... such as kitchen aid equipments, power tools, dishwashers,... Available in a fully insulated package, the T4...-...W version complies with UL standards (ref. E81734).



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit | |
|--------------------|--|--------------------------|---------------------------|--------------------------------|------------------------|
| $I_{T(RMS)}$ | RMS on-state current (full sine wave) | DKPAK / IPAK TO-220AB | $T_c = 110^\circ\text{C}$ | 4 | A |
| | | ISOWATT 220AB | $T_c = 105^\circ\text{C}$ | | |
| I_{TSM} | Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C) | F = 50 Hz | t = 20 ms | 30 | A |
| | | F = 60 Hz | t = 16.7 ms | 31 | |
| I^2t | I^2t Value for fusing | tp = 10 ms | | 5.1 | A^2s |
| dl/dt | Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, tr ≤ 100 ns | F = 120 Hz | $T_j = 125^\circ\text{C}$ | 50 | $\text{A}/\mu\text{s}$ |
| I_{GM} | Peak gate current | tp = 20 μs | $T_j = 125^\circ\text{C}$ | 4 | A |
| $P_{G(AV)}$ | Average gate power dissipation | | $T_j = 125^\circ\text{C}$ | 1 | W |
| T_{stg} T_j | Storage junction temperature range Operating junction temperature range | | | - 40 to + 150 - 40 to + 125 | $^\circ\text{C}$ |

T4 Series

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise specified)

| Symbol | Test Conditions | Quadrant | | T4 | | | Unit |
|--------------------------|--|--------------|------|------|------|------|------|
| | | | | T405 | T410 | T435 | |
| I _{GT} (1) | V _D = 12 V R _L = 30 Ω | I - II - III | MAX. | 5 | 10 | 35 | mA |
| V _{GT} | | I - II - III | MAX. | 1.3 | | | V |
| V _{GD} | V _D = V _{DRM} R _L = 33 kΩ T _j = 125°C | I - II - III | MIN. | 0.2 | | | V |
| I _H (2) | I _T = 100 mA | | MAX. | 10 | 15 | 35 | mA |
| I _L | I _G = 1.2 I _{GT} | I - III | MAX. | 10 | 25 | 50 | mA |
| | | II | | 15 | 30 | 60 | |
| dV/dt (2) | V _D = 67 %V _{DRM} gate open T _j = 125°C | | MIN. | 20 | 40 | 400 | V/μs |
| (di/dt) _c (2) | (dV/dt) _c = 0.1 V/μs T _j = 125°C | | MIN. | 1.8 | 2.7 | - | A/ms |
| | (dV/dt) _c = 10 V/μs T _j = 125°C | | | 0.9 | 2.0 | - | |
| | Without snubber T _j = 125°C | | | - | - | 2.5 | |

STATIC CHARACTERISTICS

| Symbol | Test Conditions | | Value | Unit | | |
|--------------------------------------|--|-----------------------|------------------------|------|-----|----|
| V _{TM} (2) | I _{TM} = 5.5 A t _p = 380 μs | T _j = 25°C | MAX. | 1.6 | V | |
| V _{to} (2) | Threshold voltage | | T _j = 125°C | MAX. | 0.9 | V |
| R _d (2) | Dynamic resistance | | T _j = 125°C | MAX. | 120 | mΩ |
| I _{DRM} I _{RDM} | V _{DRM} = V _{RDM} | | T _j = 25°C | MAX. | 5 | μA |
| | | | T _j = 125°C | | 1 | mA |

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1

THERMAL RESISTANCES

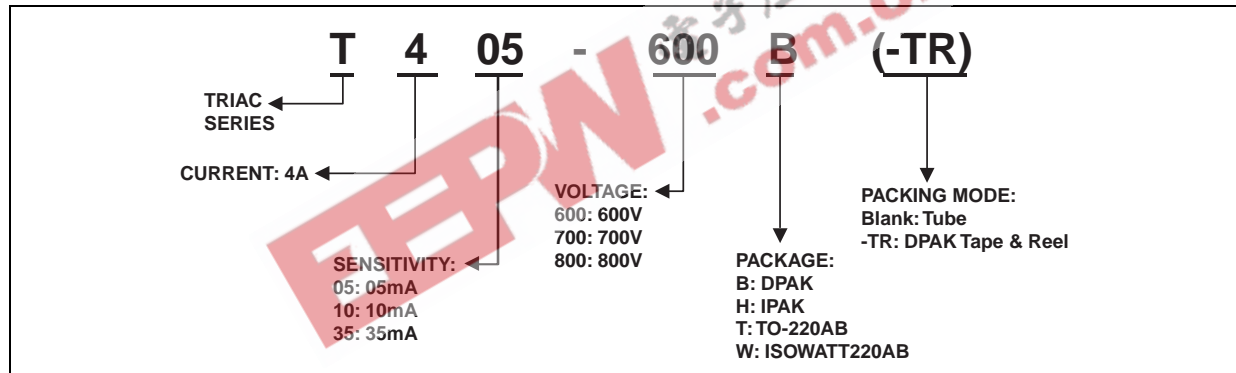
| Symbol | Parameter | | Value | Unit | | |
|----------------------|-----------------------|--|--------------------------|--------------------------|------|------|
| R _{th(j-c)} | Junction to case (AC) | | DPAK IPAK TO-220AB | 2.6 | °C/W | |
| | | | ISOWATT220AB | 4.0 | | |
| R _{th(j-a)} | Junction to ambient | | S = 0.5 cm ² | DPAK | 70 | °C/W |
| | | | | TO-220AB ISOWATT220AB | 60 | |
| | | | | IPAK | 100 | |

S = Copper surface under tab

PRODUCT SELECTOR

| Part Number | Voltage (xxx) | | | Sensitivity | Type | Package |
|-------------|---------------|-------|-------|-------------|-------------|--------------|
| | 600 V | 700 V | 800 V | | | |
| T405-xxxB | X | X | X | 5 mA | Logic level | DPAK |
| T405-xxxH | X | X | X | 5 mA | Logic level | IPAK |
| T405-xxxT | X | X | X | 5 mA | Logic level | TO-220AB |
| T405-xxxW | X | X | X | 5 mA | Logic level | ISOWATT220AB |
| T410-xxxB | X | X | X | 10 mA | Logic level | DPAK |
| T410-xxxH | X | X | X | 10 mA | Logic level | IPAK |
| T410-xxxT | X | X | X | 10 mA | Logic level | TO-220AB |
| T410-xxxW | X | X | X | 10 mA | Logic level | ISOWATT220AB |
| T435-xxxB | X | X | X | 35 mA | Snubberless | DPAK |
| T435-xxxH | X | X | X | 35 mA | Snubberless | IPAK |
| T435-xxxT | X | X | X | 35 mA | Snubberless | TO-220AB |
| T435-xxxW | X | X | X | 35 mA | Snubberless | ISOWATT220AB |

ORDERING INFORMATION



OTHER INFORMATION

| Part Number | Marking | Weight | Base quantity | Packing mode |
|--------------|----------|--------|---------------|--------------|
| T4xx-yyyB | T4xyyyyB | 0.3 g | 75 | Tube |
| T4xx-yyyB-TR | T4xyyyyB | 0.3 g | 2500 | Tape & reel |
| T4xx-yyyH | T4xyyyy | 0.4 g | 75 | Tube |
| T4xx-yyyT | T4xyyyyT | 2.3 g | 50 | Tube |
| T4xx-yyyW | T4xyyyyW | 2.1 g | 50 | Tube |

Note: xx = sensitivity, yyy = voltage

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

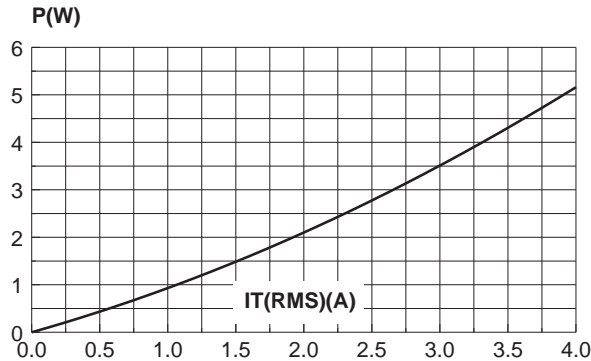


Fig. 2-1: RMS on-state current case versus temperature (full cycle).

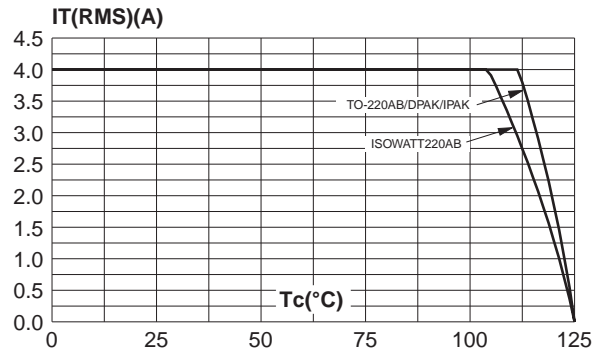


Fig. 2-2: RMS on-state current versus ambient temperature (printed circuit FR4, copper thickness: 35µm), full cycle.

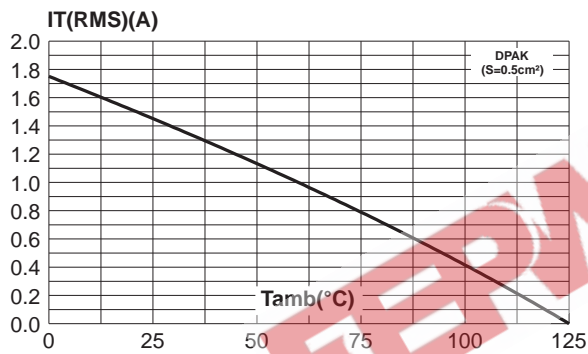


Fig. 3: Relative variation of thermal impedance versus pulse duration.

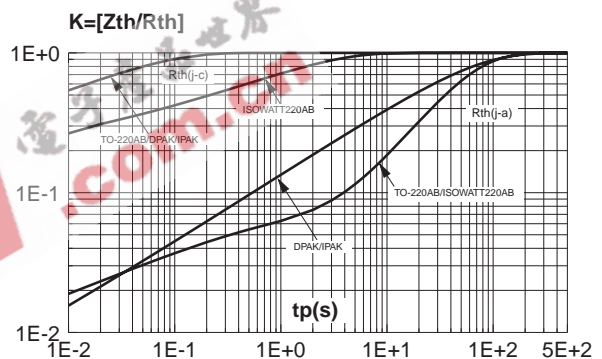


Fig. 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

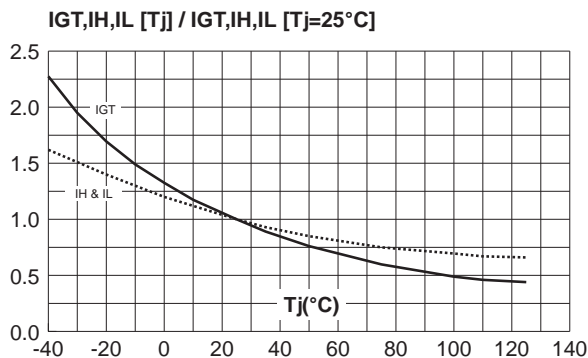


Fig. 5: Surge peak on-state current versus number of cycles.

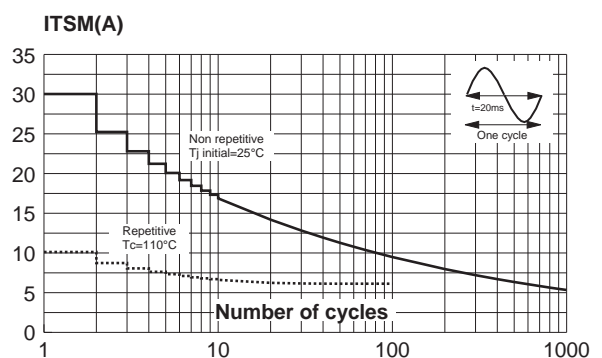


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t .

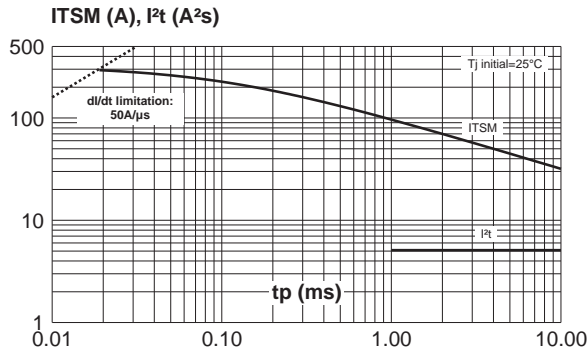


Fig. 7: On-state characteristics (maximum values).

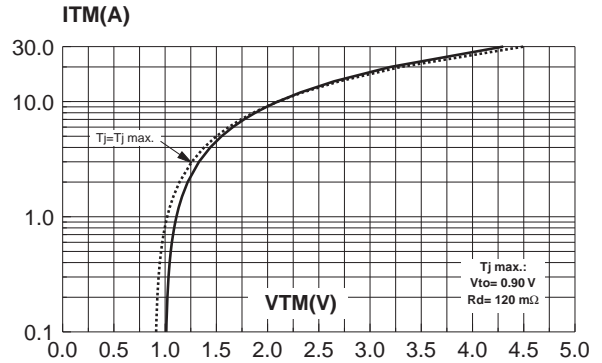


Fig. 8: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).

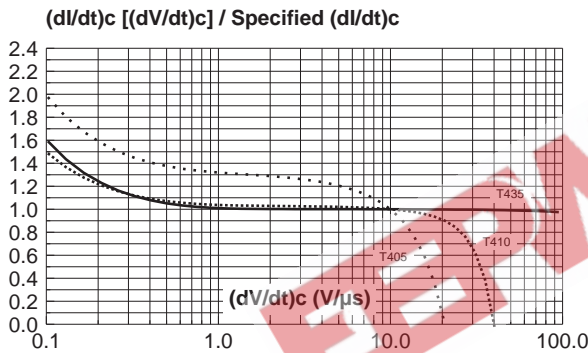


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

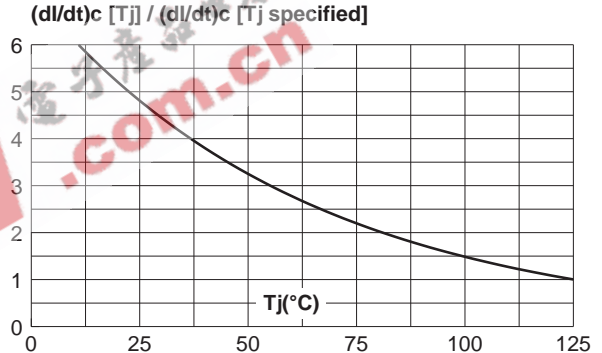
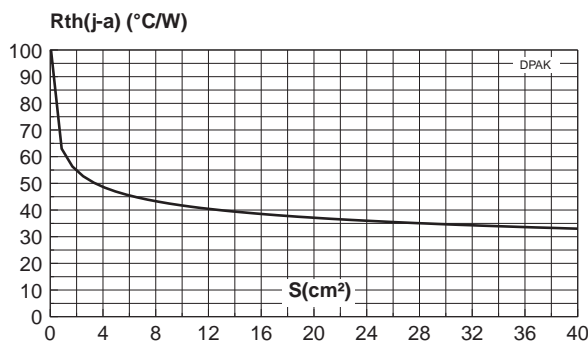


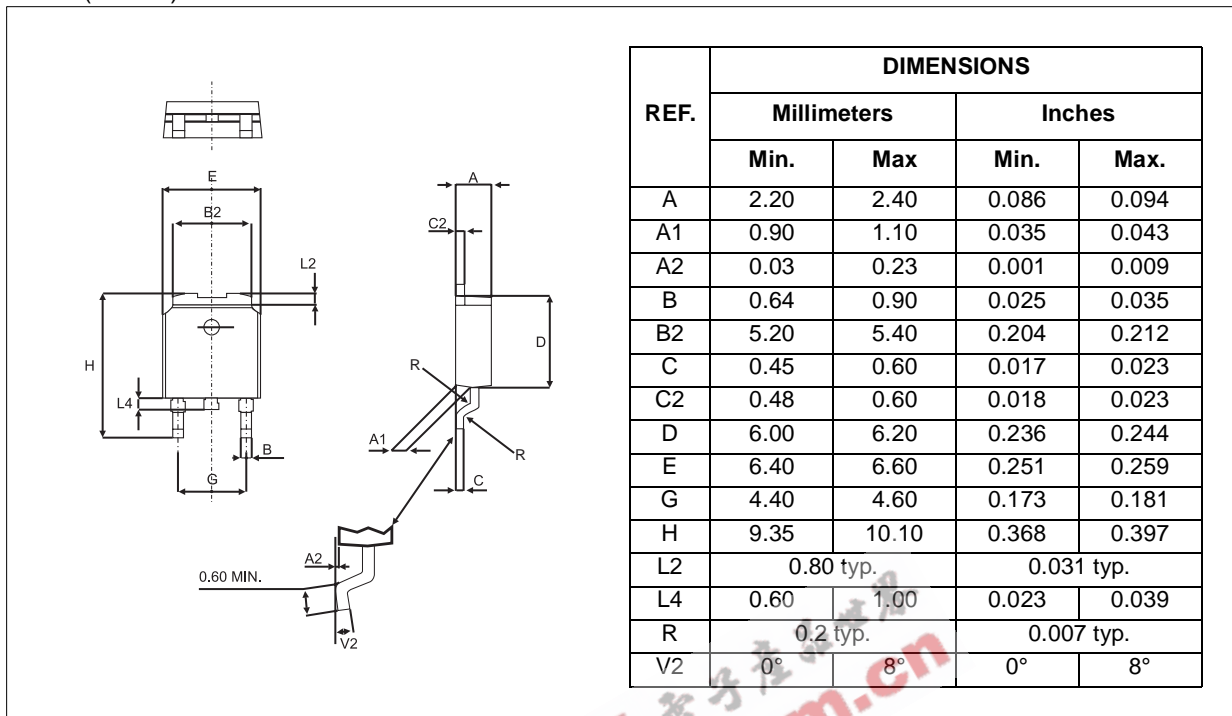
Fig. 10: DPAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: $35\mu\text{m}$).



T4 Series

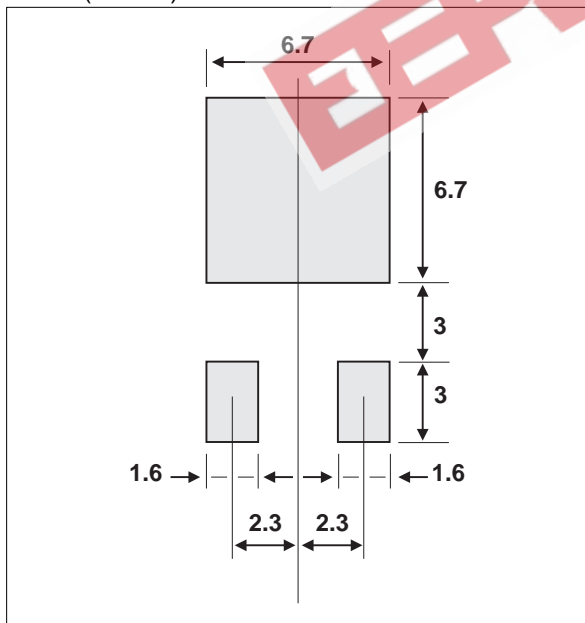
PACKAGE MECHANICAL DATA

DPAK (Plastic)



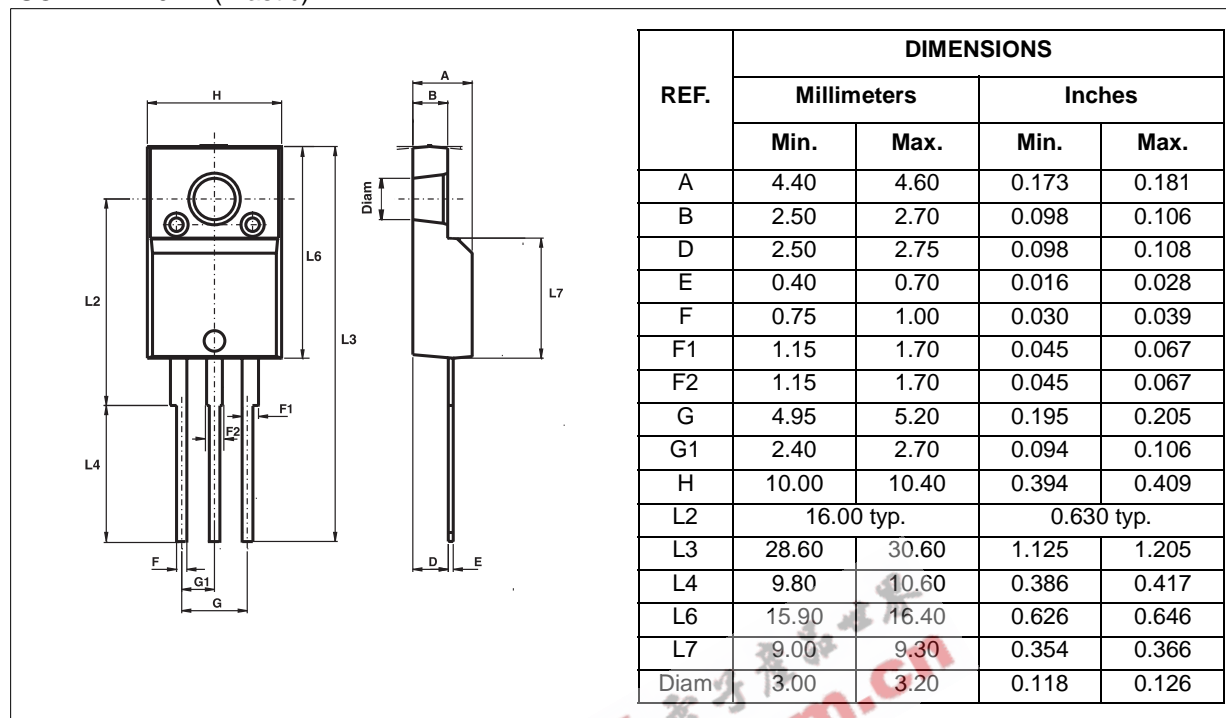
FOOTPRINT DIMENSIONS (in millimeters)

DPAK (Plastic)



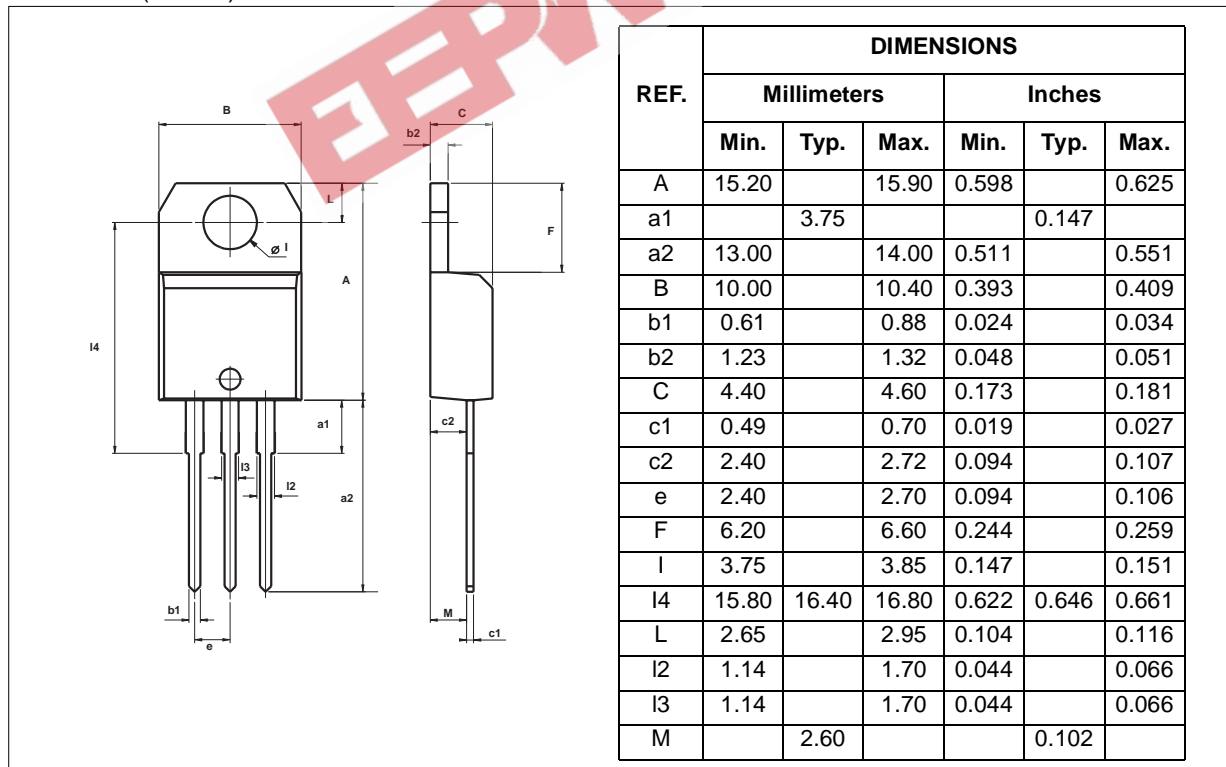
PACKAGE MECHANICAL DATA

ISOWATT220AB (Plastic)



PACKAGE MECHANICAL DATA

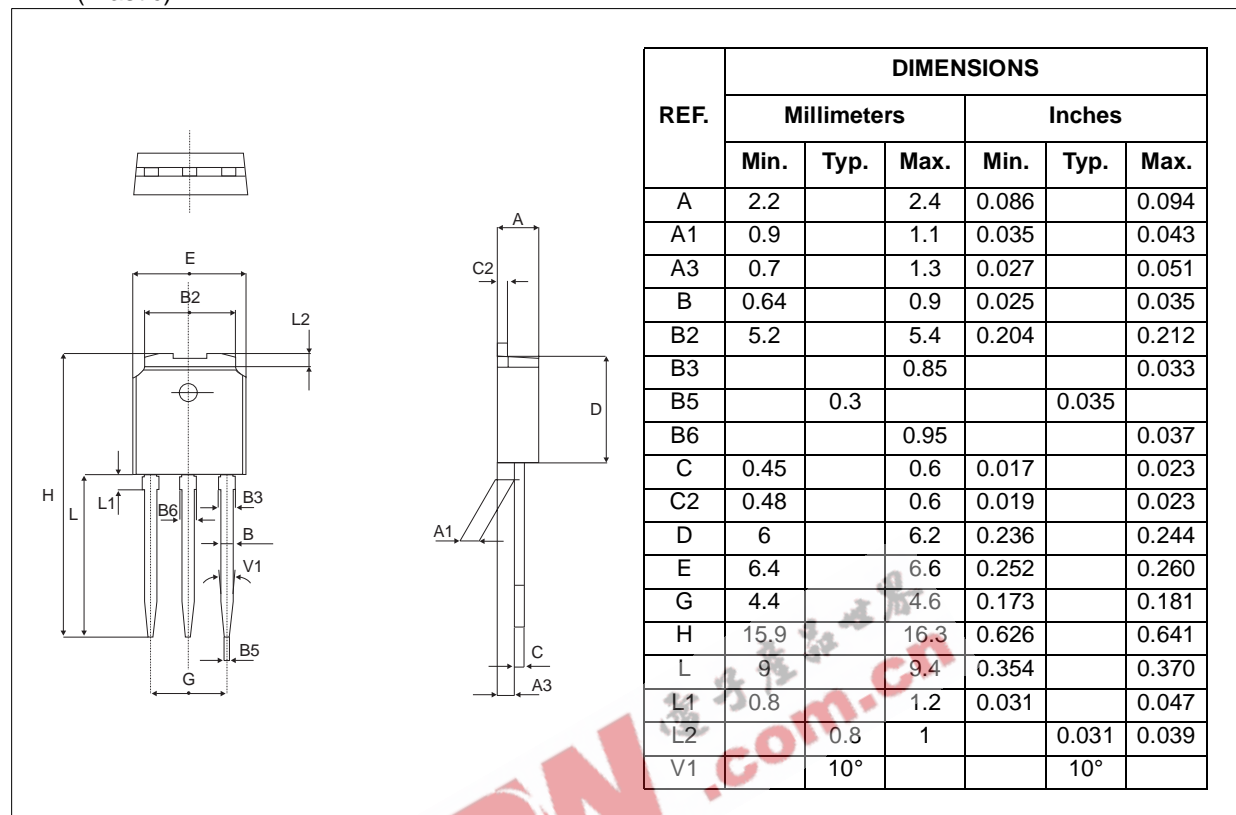
TO-220AB (Plastic)



T4 Series

PACKAGE MECHANICAL DATA

IPAK (Plastic)



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia
Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A

<http://www.st.com>