

DRAM

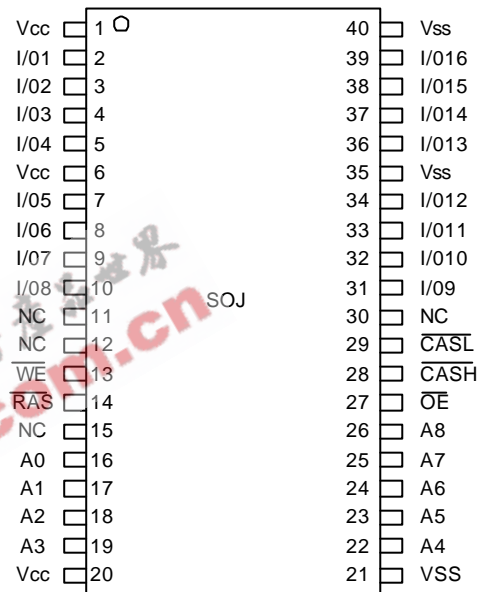
256K x 16 DYNAMIC RAM
FAST PAGE MODE

FEATURES

- Industry-standard x 16 pinouts and timing functions.
- Single 5V (±10%) power supply.
- All device pins are TTL- compatible.
- 512-cycle refresh in 8ms.
- Refresh modes: $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ (CBR) and HIDDEN.
- Conventional FAST PAGE MODE access cycle.
- BYTE WRITE and BYTE READ access cycles.

will write data into the upper byte (IO9~16).

PIN ASSIGNMENT (Top View)



OPTION

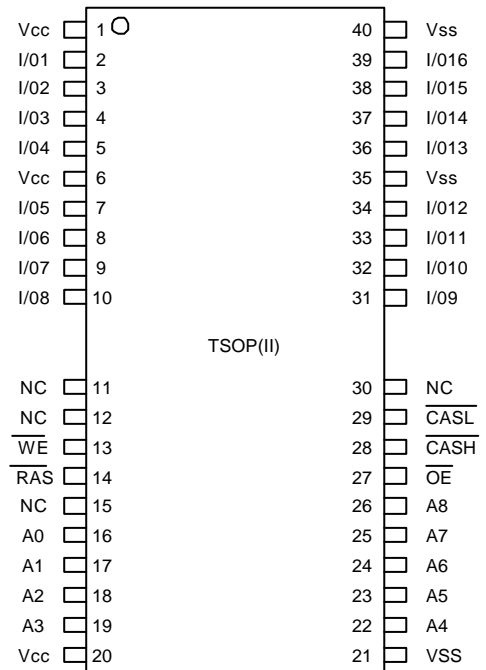
TIMING	MARKING
30ns	-30
35ns	-35
45ns	-45
60ns	-60

PACKAGE	MARKING
SOJ	J
TSOP(II)	S

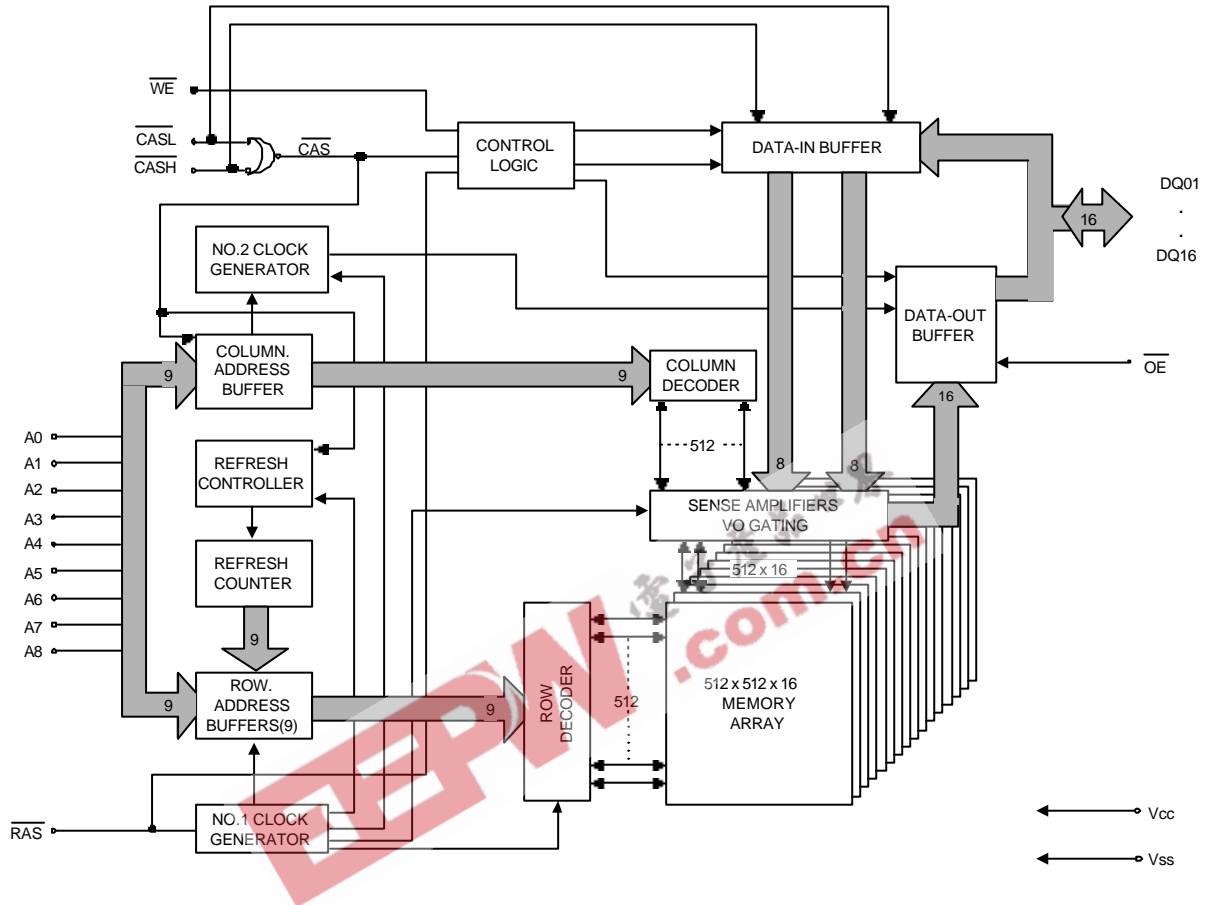
GENERAL DESCRIPTION

The T224160B is a randomly accessed solid state memory containing 4,194,304 bits organized in a x16 configuration. The T224160B has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. It offers Fast Page mode operation

The T224160B $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ to transition low and by the last to transition back high. Use only one of the two $\overline{\text{CAS}}$ and leave the other staying high during WRITE will result in a BYTE WRITE. $\overline{\text{CASL}}$ transiting low in a WRITE cycle will write data into the lower byte (IO1~IO8), and $\overline{\text{CASH}}$ transiting low



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~26	A0-A8	Input	Address Input
14	$\overline{\text{RAS}}$	Input	Row Address Strobe
28	$\overline{\text{CASH}}$	Input	Column Address Strobe /Upper Byte Control
29	$\overline{\text{CASL}}$	Input	Column Address Strobe /Lower Byte Control
13	$\overline{\text{WE}}$	Input	Write Enable
27	$\overline{\text{OE}}$	Input	Output Enable
2~5,6~10,31~34,36~39	I/O1 - I/O16	Input/ Output	Data Input/ Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any pin Relative to VSS... .. -1V to 7V
 Operating Temperature, Ta (ambient)..0°C to +70°C
 Storage Temperature (plastic)..... -55°C to +150°C
 Power Dissipation
 1.2W
 Short Circuit Output Current.....
 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ Ta ≤ 70°C; VCC = 5V ± 10 % unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM.	MIN	MAX	UNITS	NOTES
Supply Voltage		V _{CC}	4.5	5.5	V	1
Supply Voltage		V _{SS}	0	0	V	
Input High (Logic) voltage		V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic) voltage		V _{IL}	-1.0	0.8	V	1
Input Leakage Current	0V ≤ V _{IN} ≤ 7V	I _{LI}	-10	10	uA	
Output Leakage Current	0V ≤ V _{OUT} ≤ 7V Output(s) disabled	I _{LO}	-10	10	uA	
Output High Voltage	I _{OH} = -5 mA	V _{OH}	2.4	-	V	
Output Low Voltage	I _{OL} = 4.2 mA	V _{OL}	-	0.4	V	

Note: 1.All Voltages referenced to Vss

DC CHARACTERISTICS

(Ta = 0 to 70°C, Vcc = 5V ±10%, Vss = 0V)

Parameter	Symbol	-30		-35		-45		-60		Unit	Test Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating Current	Icc1	-	200	-	180	-	160	-	140	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling $t_{\text{RC}} = \text{min}$
Standby Current	Icc2	-	4	-	4	-	4	-	4	mA	TTL interface, $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{\text{IH}}$, $D_{\text{OUT}} = \text{High-Z}$
Standby Current	Icc3	-	2	-	2	-	2	-	2	mA	CMOS interface, $\overline{\text{RAS}}$, $\overline{\text{CAS}} > V_{\text{CC}} - 0.2\text{V}$
Fast Page Mode Current	Icc4	-	200	-	180	-	160	-	140	mA	$\overline{\text{RAS}} = V_{\text{IL}}$, $\overline{\text{CAS}}$ cycling, $t_{\text{PC}} = \text{min}$
$\overline{\text{RAS}}$ -only refresh Current	Icc5	-	200	-	180	-	160	-	140	mA	$\overline{\text{CAS}} = V_{\text{IH}}$, $\overline{\text{RAS}}$ cycling, $t_{\text{RC}} = \text{min}$
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current	Icc6	-	200	-	180	-	160	-	140	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{\text{RC}} = \text{min}$

Note: Icc depends on output load condition when the device is selected.

Icc max is specified at the output open condition, Icc is specified as an average current.

CAPACITANCE

(Ta = 25°C, Vcc = 5V, f = 1M HZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (address)	C _{I1}	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	-	7	pF
Output Capacitance (data-in/out)	C _{I/O}	-	10	pF

AC CHARACTERISTICS (note 1,2,3) (Ta = 0 to 70°C)

AC TEST CONDITIONS:

Vcc=5V ±10%, input pulse level = 0 to 3V

Input rise and fall times: 2ns

Output Load: 2TTL gate + CL (50pF)

AC CHARACTERISTICS PARAMETER	SYM	-30		-35		-45		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t _{RC}	55		65		85		110		ns	
Read-Modify-Write Cycle Time	t _{RWC}	85		95		115		155		ns	
Fast-Page-Mode Read or Write Cycle Time	t _{PC}	19		21		25		40		ns	
Fast-Page-Mode Read-Write Cycle Time	t _{PCM}	56		58		65		80		ns	
Access Time From $\overline{\text{RAS}}$	t _{RAC}		30		35		45		60	ns	4
Access Time From $\overline{\text{CAS}}$	t _{CAC}		8		9		11		15	ns	5
Access Time From $\overline{\text{OE}}$	t _{OAC}		8		9		11		15	ns	13
Access Time From Column Address	t _{AA}		13		15		19		30	ns	8
Access Time From $\overline{\text{CAS}}$ Precharge	t _{ACP}		15		18		22		35	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	30	10K	35	10K	45	10K	60	10K	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RASC}	30	100K	35	100K	45	100K	60	100K	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	8		9		11		15		ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	25		30		35		40		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	5	10K	6	10K	7	10K	15	10K	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	30		35		45		60		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	3		3		5		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	10	24	10	28	10	37	20	45	ns	7
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	3		3		5		5		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	5		5		5		5		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	8	17	8	20	8	26	15	30	ns	8
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	4		4		6		15		ns	
Column Address Hold Time (Reference to $\overline{\text{RAS}}$)	t _{AR}	26		30		40		50		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	13		15		19		30		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	14
Read Command Hold Time Reference to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	9,14
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	t _{CLZ}	3		3		3		3		ns	
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	t _{OFF1}	3	15	3	15	3	15	3	15	ns	10,16

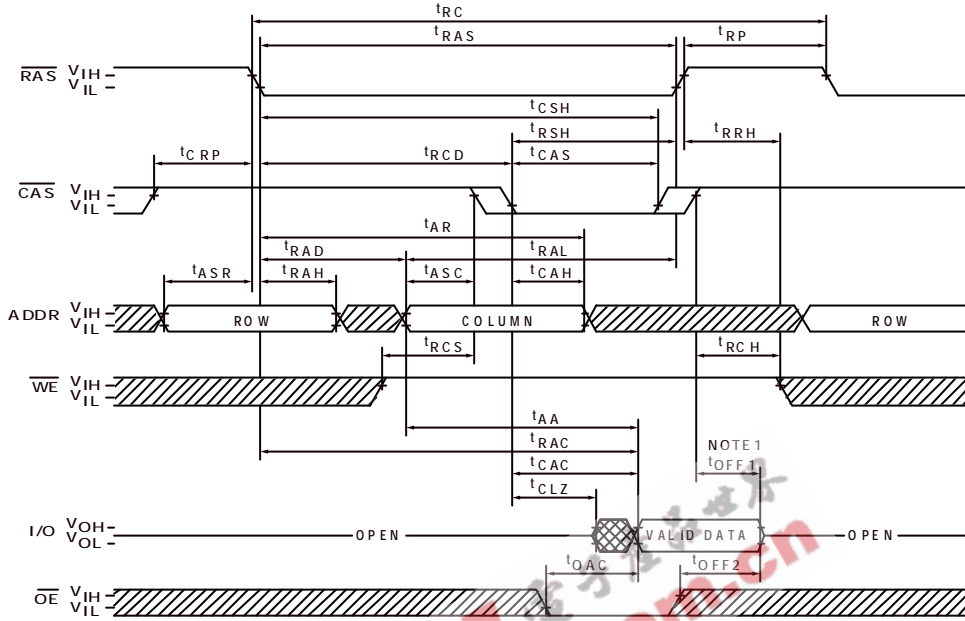
AC CHARACTERISTICS (continued)

AC CHARACTERISTICS PARAMETER	SYM	-30		-35		-45		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output Buffer Turn-off \overline{OE} to	tOFF2	-	8	-	8	-	8	-	15	ns	16
Write Command Setup Time	tWCS	0		0		0		0		ns	11,14
Write Command Hold Time	tWCH	4		4		6		10		ns	
Write Command Hold Time (Reference to \overline{RAS})	tWCR	26		30		46		50		ns	14
Write Command Pulse Width	tWP	4		4		6		10		ns	14
Write Command to \overline{RAS} Lead Time	tRWL	6		7		9		15		ns	14
Write Command to \overline{CAS} Lead Time	tCWL	6		7		9		15		ns	14
Data-in Setup Time	tDS	0		0		0		0		ns	12
Data-in Hold Time	tDH	4		4		6		15		ns	12
Data-in Hold Time (Reference to \overline{RAS})	tDHR	26		30		40		50		ns	
\overline{RAS} to \overline{WE} Delay Time	tRWD	46		51		61		85		ns	11
Column Address to \overline{WE} Delay Time	tAWD	29		31		35		55		ns	11
\overline{CAS} to \overline{WE} Delay Time	tCWD	24		25		27		40		ns	11
Transition Time (rise or fall)	tT	1.5	50	2.5	50	2.5	50	3	50	ns	2,3
Refresh Period (512 cycles)	tREF		8		8		8		8	ms	
\overline{RAS} to \overline{CAS} Precharge Time	tRPC	10		10		10		10		ns	
\overline{CAS} Setup Time (CBR REFRESH)	tCSR	10		10		10		10		ns	6
\overline{CAS} Hold Time (CBR REFRESH)	tCHR	10		10		10		10		ns	6
\overline{OE} Hold Time From \overline{WE} During Read-Modify-Write Cycle	tOEH	4		4		6		15		ns	15
\overline{OE} Setup Prior to \overline{RAS} During Hidden Refresh Cycle	tORD	0		0		0		0		ns	
Write Command Hold Time (Test Mode in)	tWTH	10		10		10		10		ns	
Write Command Setup Time (Test Mode in)	tWTS	10		10		10		10		ns	

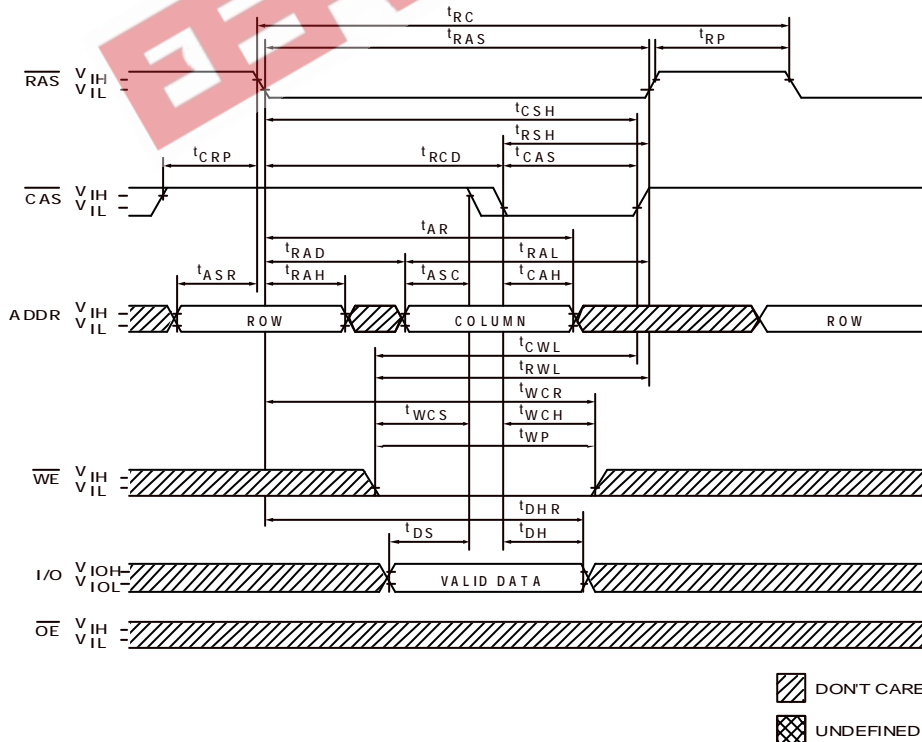
Notes:

1. An initial pause of 200us is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ only or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
2. $V_{\text{IH}}(2.4\text{V})$ and $V_{\text{IL}}(0.8\text{V})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{\text{IH}}(2.4\text{V})$ and $V_{\text{IL}}(0.8\text{V})$.
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{\text{RCD}} < t_{\text{RCD}}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. Enables on-chip refresh and address counters.
7. Operation within the $t_{\text{RCD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, access time is controlled by t_{CAC} .
8. Operation within the t_{RAD} limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, access time is controlled by t_{AA} .
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. $t_{\text{OFF1}}(\text{max})$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
11. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ or $\overline{\text{OE}}$ go back to V_{IH}) is indeterminate. $\overline{\text{OE}}$ held high and $\overline{\text{WE}}$ taken low after $\overline{\text{CAS}}$ goes low result in a LATE WRITE ($\overline{\text{OE}}$ - controlled) cycle.
12. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if $\overline{\text{OE}}$ is low then taken HIGH before $\overline{\text{CAS}}$ goes high, I/O goes open, if $\overline{\text{OE}}$ is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. WRITE command is defined as $\overline{\text{WE}}$ going low.
15. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OFF2} and t_{OEH} met ($\overline{\text{OE}}$ high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
16. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.

READ CYCLE



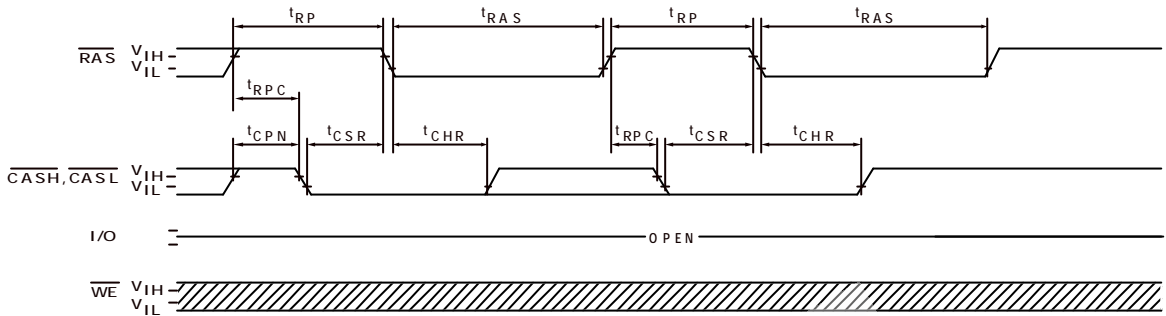
EARLY WRITE CYCLE



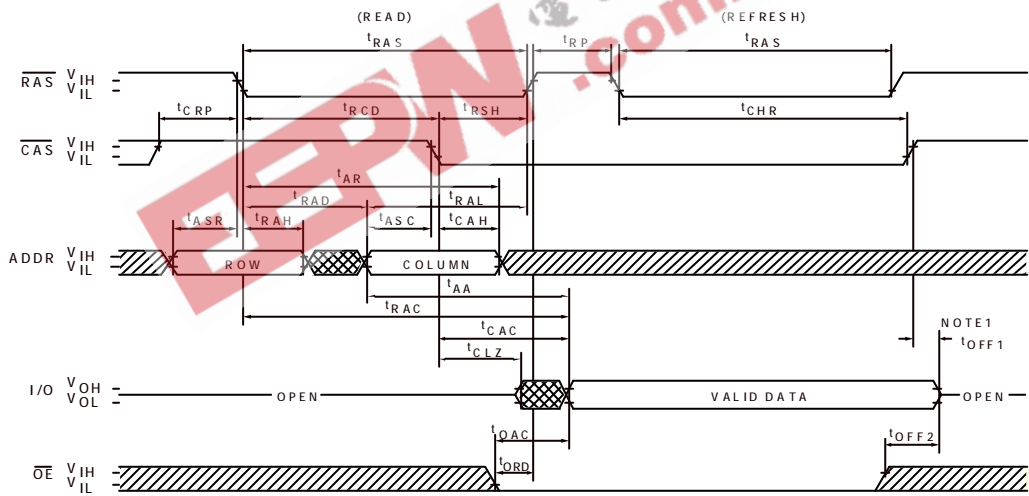
 DONT CARE
 UNDEFINED

Note: t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

CBR REFRESH CYCLE
(A0-A8 ; \overline{OE} =DON'T CARE)

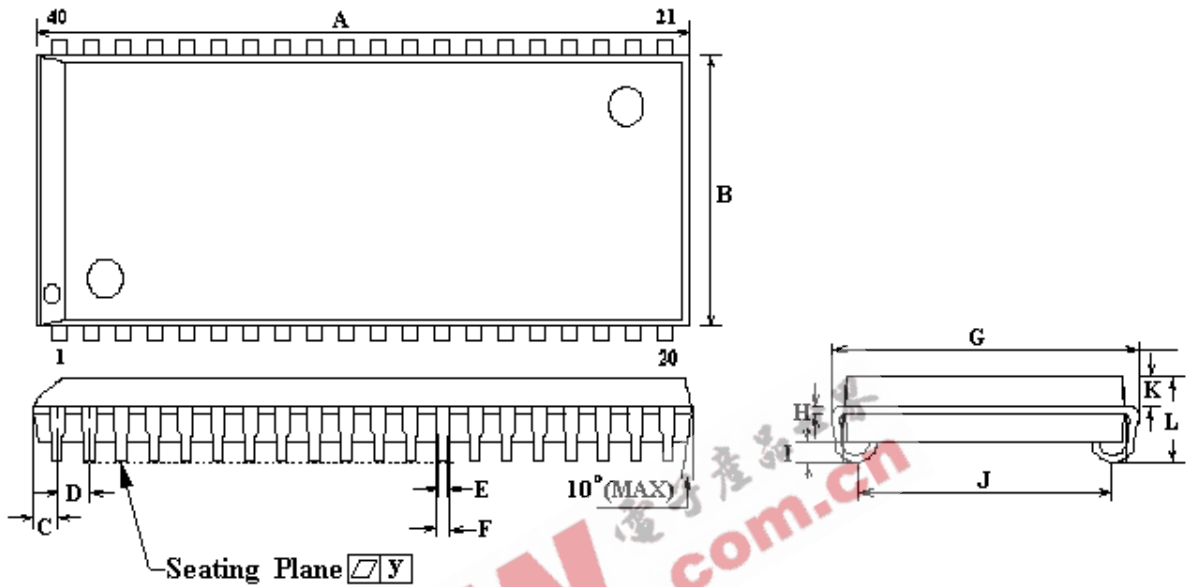


HIDDEN REFRESH CYCLE
(\overline{WE} =HIGH ; \overline{OE} =LOW)



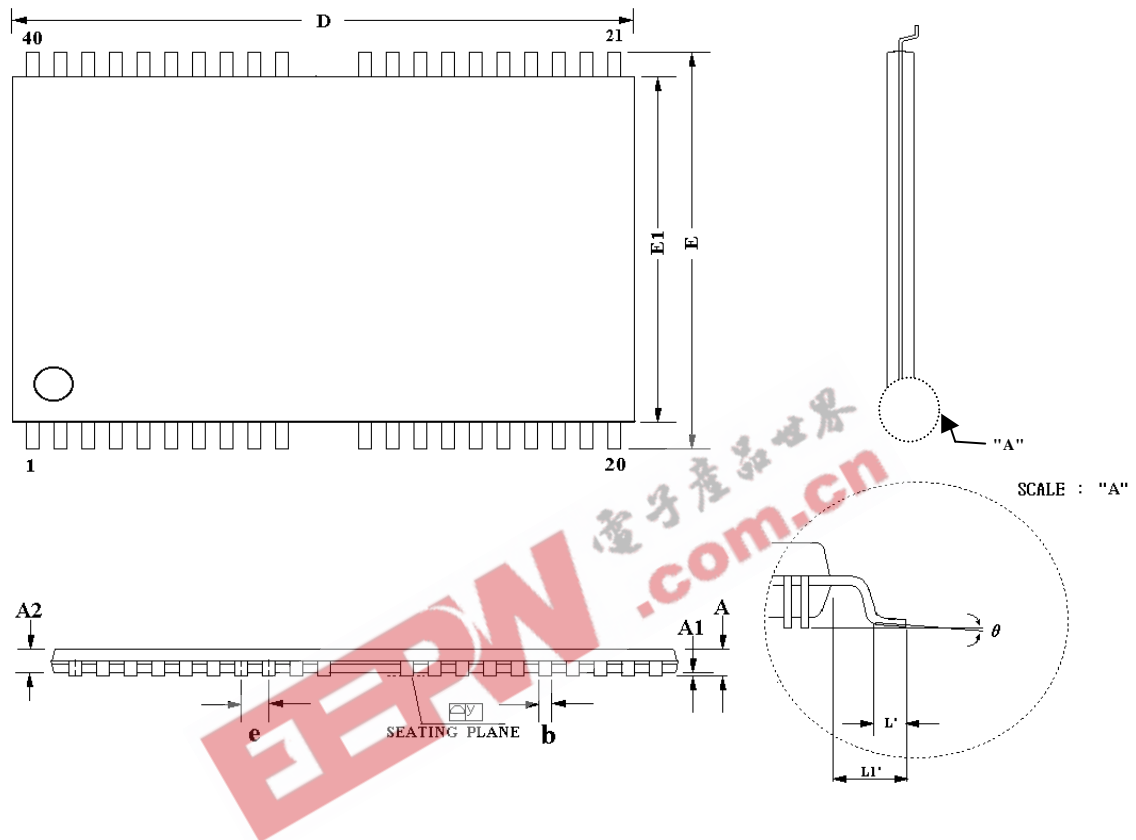
Note: 1. t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

PACKAGE DIMENSIONS
40-LEAD SOJ DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	1.025±0.010	26.035±0.254
B	0.400±0.005	10.160±0.127
C	0.045(MAX)	1.143(MAX)
D	0.050±0.006	1.27±0.152
E	0.019±0.003	0.483±0.08
F	0.026±0.003	0.661±0.080
G	0.440±0.010	11.176±0.254
H	0.011±0.003	0.280±0.080
I	0.025(MIN)	0.635(MIN)
J	0.364±0.020	9.246±0.508
K	0.047±0.006	1.194±0.152
L	0.150(MAX)	3.810(MAX)
y	0.004(MAX)	0.102(MAX)

PACKAGE DIMENSIONS
40-LEAD TSOP II DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max)	1.20(max)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.014(typ.)	0.35(typ.)
c	0.005(typ.)	0.127(typ.)
D	0.725±0.004	18.41±0.10
E	0.463±0.008	11.76±0.20
E1	0.400±0.004	10.16±0.10
L1'	0.031	0.80
L'	0.020±0.004	0.500±0.10
y	0.004(max)	0.10(max)
θ	0°~5°	0°~5°