

**SDRAM**

**4M x 16 SDRAM**  
**1M x 16bit x 4Banks Synchronous DRAM**

**FEATURES**

- 3.3V power supply
- Four banks operation
- LVTTTL compatible with multiplexed address
- All inputs are sampled at the positive going edge of system clock
- DQM for masking
- Auto refresh and self refresh
- 64ms refresh period
- 15.6 us refresh interval.
- MRS cycle with address key programs
  - CAS Latency ( 2 & 3 )
  - Burst Length ( 1 , 2 , 4 , 8 & full page)
  - Burst Type (Sequential & Interleave)
- Available package type in 54 pin TSOP(II)
- Operating temperature : 0 ~ +70 °C

**GRNERAL DESCRIPTION**

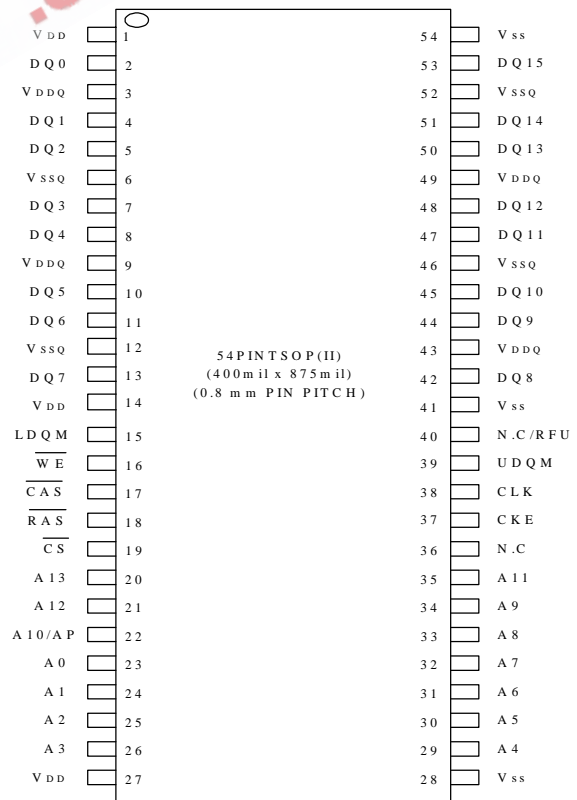
The T436416C is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits , fabricated with high performance CMOS technology .

Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

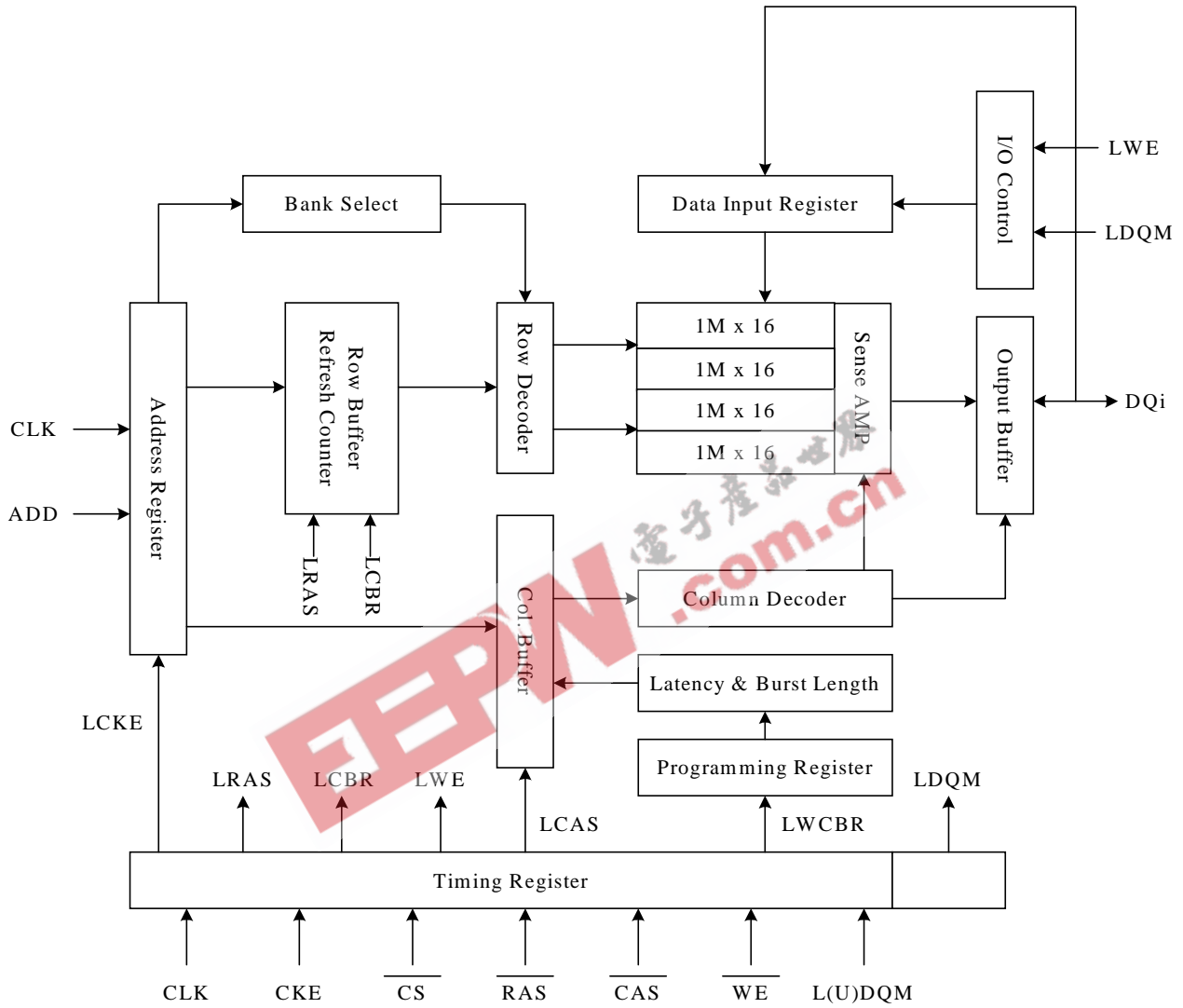
**ORDERING INFORMATION**

PART NO.	MAX FREQUENCY	PACKAGE
T436416C-6S	166 MHz	54 pin TSOP(II)
T436416C-7S	143 MHz	54 pin TSOP(II)
T436416C-6SG	166 MHz	54 pin TSOP(II) lead-free
T436416C-7SG	143 MHz	54 pin TSOP(II) lead-free

**PIN ARRANGEMENT (Top View)**



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all input.
$\overline{\text{CS}}$	Chip Select	Disables or enables device operation by masking or enabling all input except CLK,CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11,column address : CA0 ~ CA7
A12 ~ A13	Bank Select Address	Selects bank to be activated during row address latch time. Select bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access .
$\overline{\text{WE}}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.
L(U)DQM	Data Input/Output Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
V <sub>DD</sub> /V <sub>SS</sub>	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V <sub>DDQ</sub> /V <sub>SSQ</sub>	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/Reserved for Future Use	This pin is recommended to be left No Connection on the device.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative To Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-1.0 to 4.6	V
Supply Voltage Relative To Vss	V <sub>DD</sub> ,V <sub>DDQ</sub>	-1.0 to 4.6	V
Short circuit Output Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>D</sub>	1	W
Operating Temperature	T <sub>OPR</sub>	0 to +70	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(T<sub>A</sub> = 0 to +70°C, Voltage referenced to Vss=0V)

Parameter	Symbol	Min.	Typ	Max.	Unit	Notes
Supply Voltage	V <sub>DD</sub> ,V <sub>DDQ</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DD</sub> +0.3V	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output logic high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> =-2mA
Output logic low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> =2mA
Input leakage current	I <sub>IL</sub>	-5	-	5	uA	3
Output leakage current	I <sub>OL</sub>	-5	-	5	uA	4

**Note :** 1. V<sub>IH</sub> (max) = 4.6V AC for pulse width ≤ 10ns acceptable.  
 2. V<sub>IL</sub> (min) = -1.5V AC for pulse width ≤ 10ns acceptable.  
 3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DD</sub>+ 0.3V , all other pin are not under test = 0V.  
 4. Dout = disable, 0V ≤ V<sub>OUT</sub> ≤ V<sub>DD</sub> .

**CAPACITANCE**

(T<sub>A</sub> =25°C,V<sub>DD</sub>=3.3V, f = 1MHz)

Pin	Symbol	Min	Max	Unit
CLOCK	C <sub>CLK</sub>	2.0	4.0	pF
ADDRESS	C <sub>ADD</sub>	2.0	4.0	pF
DQ0 ~ DQ15	C <sub>OUT</sub>	2.0	4.0	pF
RAS,CAS,WE,CS,CKE,LDQM, UDQM	C <sub>IN</sub>	2.0	5.0	pF

**DC CHARACTERISTICS**
 $T_A = 0 \text{ to } 70^\circ\text{C}$  ,  $V_{IH}(\text{min})/V_{IL}(\text{max})=2.0\text{V}/0.8\text{V}$ 

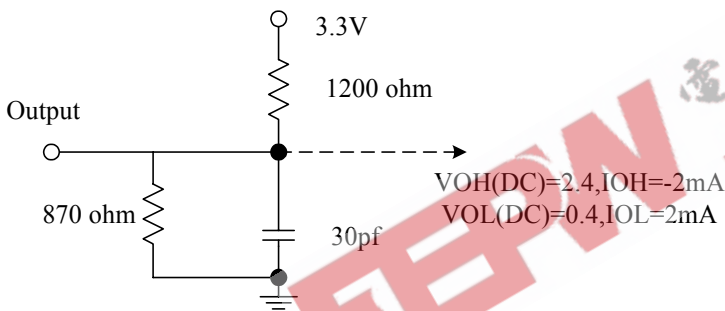
Parameter	Symbol	Speed version		Unit	Test Condition	Note
		-6	-7			
Operating Current ( One Bank Active)	I <sub>CC1</sub>	110	100	mA	Burst Length = 1 $t_{RC} \geq t_{RC}(\text{min})$ , $t_{CC} \geq t_{CC}(\text{min})$ , IOL= 0 mA	1,2
Precharge Standby Current in power- down mode	I <sub>CC2P</sub>	2		mA	$\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = t_{CC}(\text{min})$	2
	I <sub>CC2PS</sub>	1			$\text{CKE} \leq V_{IL}(\text{max})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$	
Precharge Standby Current in non power-down mode	I <sub>CC2N</sub>	20		mA	$\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = t_{CC}(\text{min})$ Input signals are changed one time during 2CLK	2
	I <sub>CC2NS</sub>	15			$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{min})$ , $t_{CC} = \infty$ Input signals are stable	
Active Standby Current in power- down mode	I <sub>CC3P</sub>	10		mA	$\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = t_{CC}(\text{min})$	2
	I <sub>CC3PS</sub>	10			$\text{CKE} \leq V_{IL}(\text{max})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$	
Active Standby Current in non power-down mode (One Bank Active)	I <sub>CC3N</sub>	30		mA	$\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = t_{CC}(\text{min})$ Input signals are changed one time during 2CLK	2
	I <sub>CC3NS</sub>	25			$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{min})$ , $t_{CC} = \infty$ Input signals are stable	
Operating Current (Burst Mode)	I <sub>CC4</sub>	150	140	mA	CAS Latency 3      IOL=0 mA, Page Burst	1,2
		150	140		CAS Latency 2      All Band Activated $t_{CCD} = t_{CCD}(\text{min})$	
Refresh Current	I <sub>CC5</sub>	180	180	mA	$t_{RC} \geq t_{RC}(\text{min})$	2
Self refresh Current	I <sub>CC6</sub>	1		mA	$\text{CKE} \leq 0.2\text{V}$	

- Note: 1. Measured with output open. Addresses are changed one time during 2CLKS .  
 2.  $t_{CC}$  : Clock cycle time.  
 $t_{RC}$  : Row cycle time.  
 $t_{CCD}$  : Column address to column address delay time.

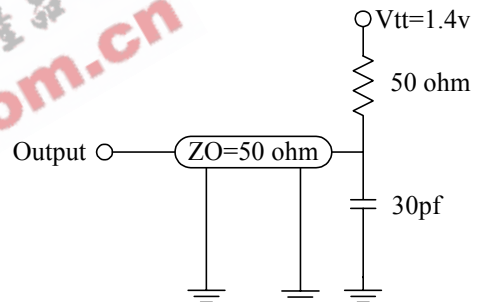
**AC OPERATING CONDITIONS**

( $V_{DD}=3.3V \pm 0.3V$ ,  $T_A=0$  to  $70^{\circ}C$ )

Parameter	Value	Unit
Input levels ( $V_{IH}/V_{IL}$ )	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r / t_f = 1 / 1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig.1) DC Output Load Circuit



(Fig.2) AC Output Load Circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Speed Version		Unit	Note
		-6	-7		
Row active to row active delay	tRRD(min)	12	14	ns	1
RAS to CAS delay	tRCD(min)	18	20	ns	1
Row precharge time	tRP(min)	18	20	ns	1
Row active time	tRAS(min)	40	42	ns	1
	tRAS(max)	100K		ns	
Row cycle time (operating)	tRC(min)	58	63	ns	1
Row cycle time (auto refresh)	tRFC(min)	60	70	ns	1,5
Last data in to new col. Address delay	tCDL(min)	1		CLK	2
Last data in to row precharge	tRDL(min)	2		CLK	2
Last data in to burst stop	tBDL(min)	1		CLK	2
Col. Address to col. Address delay	tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4
	CAS latency=2	1			

- Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

**AC CHARACTERISTICS**

(AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-7		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS Latency = 3	t <sub>CC</sub>	6	1K	7	1K	ns	1
	CAS Latency = 2		8		10			
CLK to valid Output delay	CAS Latency = 3	t <sub>SAC</sub>	-	5.5	-	6	ns	1
	CAS Latency = 2		-	6	-	6	ns	
Output data hold time		t <sub>OH</sub>	2.5		2.5		ns	2
CLK high pulse width		t <sub>CH</sub>	2.5		2.5		ns	3
CLK low pulse width		t <sub>CL</sub>	2.5		2.5		ns	3
Input setup time		t <sub>SS</sub>	1.5		1.5		ns	3
Input hold time		t <sub>SH</sub>	1		1		ns	3
CLK to output in Low-Z		t <sub>SLZ</sub>	0		0		ns	2
CLK to output in Hi-Z	CAS Latency = 3	t <sub>SHZ</sub>	-	5.5	-	6	ns	
	CAS Latency = 2		-	6	-	6	ns	

Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr &amp; tf)=1ns.

If tr &amp; tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr+tf)/2-1]ns should be added to the parameter.



**FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE**

T436416C-6S

(Unit : number of clock)

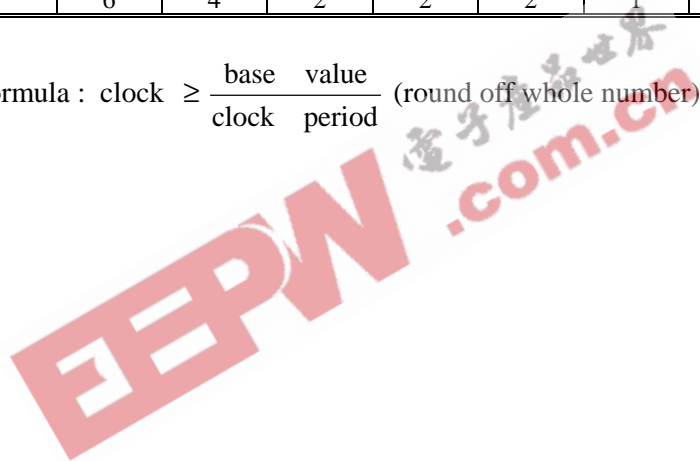
Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		58ns	40ns	18ns	12ns	18ns	6ns	6ns	12ns
166MHz(6.0ns)	3	10	7	3	2	3	1	1	2
143MHz(7.0ns)	3	9	6	3	2	3	1	1	2
133MHz(7.5ns)	3	8	6	3	2	3	1	1	2
125MHz(8.0ns)	2	8	5	3	2	3	1	1	2
100MHz(10.0ns)	2	6	4	2	2	2	1	1	2

T436416C-7S

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		63ns	42ns	20ns	14ns	20ns	7ns	7ns	14ns
143MHz(7.0ns)	3	9	6	3	2	3	1	1	2
133MHz(7.5ns)	3	9	6	3	2	3	1	1	2
125MHz(8.0ns)	3	8	6	3	2	3	1	1	2
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2
83MHz(12.0ns)	2	6	4	2	2	2	1	1	2

Note : 1. Clock count formula :  $\text{clock} \geq \frac{\text{base value}}{\text{clock period}}$  (round off whole number).



**MODE REGISTER**

Register Programmed with MRS

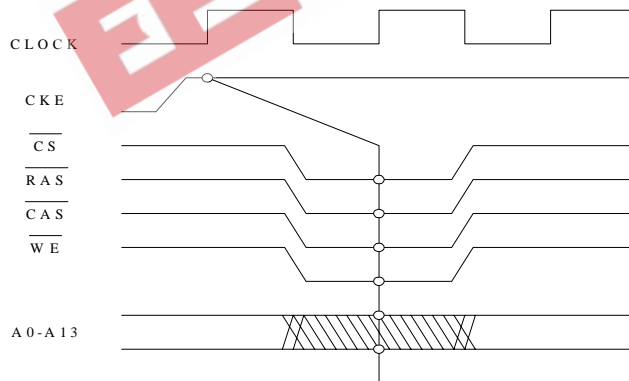
Address	A13~A12	A11~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	RFU	TM	CAS Latency			BT	Burst Length			

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : 256

- Note : 1. RFU (reserved for future use) should stay “0” during MRS cycle.  
 2. Test mode use A7~A8, vendor specific options use A9, A10~A11 and A12~A13.  
 A7~A8, A10 /AP~A11 and A12~A13 must be set to low for normal SDRAM operation.  
 Refer to the table for specific codes for various burst length, burst type and CAS latencies.

**Mode Register Write Timing**



**Burst Length and Sequence**

(Burst of Two)

Starting Address (column address A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

Starting Address (column address A1-A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256 for 4Mx16 device.

**POWER UP SEQUENCE**

1. Apply power and start clock, attempt to maintain CKE = ‘H’ , L(U)DQM = ‘H’ and the other pin are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initialize the mode register.  
Cf.) Sequence of 4 & 5 is regardless of the order.  
The device is now ready for normal operation.

**SIMPLIFIED TRUTH TABLE**

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A13, A12	A10/AP	A9~A0, A11	Note
Register	Mode Register Set	H	X	L	L	L	L	X	X			1,2
Refresh	Auto Refresh	H	H	L	L	L	H	X	X		3	
	Self Refresh		Entry						L			
		Exit	L	H	L	H	H	X	X		3	
Bank Active & Row Address		H	X	L	L	H	H	X	V	Row Address		
Read Column Address	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4,5
	Auto Precharge Enable									H		
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4,5
	Auto Precharge Enable									H		
Burst Stop		H	X	L	H	H	L	X	X		6	
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L		4
	All Banks								X	H		
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X			
	Exit			L	H	X	X		X	X		
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H		H			
	Exit	L	H	L	H	X	X	X	X			
DQM		H		X				V	X		7	
No Operation Command		H	X	H	X	X	X	X	X			
		H		L	H	H	H					

(V=Valid , X=Don't Care , H=Logic High , L=logic Low)

Notes :

- OP Code : Operation Code. A0~A11 , A13~A12 : Program keys.(@MRS)
- MRS can be issued only at both banks precharge state. A new command can be issued after 2 clock cycle of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM. The automatical precharge without row precharge command is meant by 'Auto'. Auto / self refresh can be issued only at both banks precharge state.
- A13~A12 : Bank select address.  
 If both A13 and A12 are 'Low' : at read , write , row active and precharge , bank A is selected.  
 If both A13 is 'Low' and A12 is 'High' : at read , write , row active and precharge , bank B is selected.  
 If both A13 is 'High' and A12 is 'Low' : at read , write , row active and precharge , bank C is selected.  
 If both A13 and A12 are 'High' : at read , write , row active and precharge , bank D is selected  
 If A10/AP is 'High' : at row precharge , A13 and A12 ignored and all banks are selected.
- During burst read or write with auto precharge , new read/write command cannot be issued.  
 Another bank read/write command can be issued after the end of burst.  
 New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)



\*note : 1. All input expect CKE & DQM can be don't care when  $\overline{CS}$  is high at the CLK high going edge.

2. Bank active & read/write are controlled by A13 – A12.

A13	A12	Active & Read/Write
0	0	Bank A
1	0	Bank B
0	1	Bank C
1	1	Bank D

3. Enable and disable auto precharge function are controlled by A10/AP in read/wirte command.

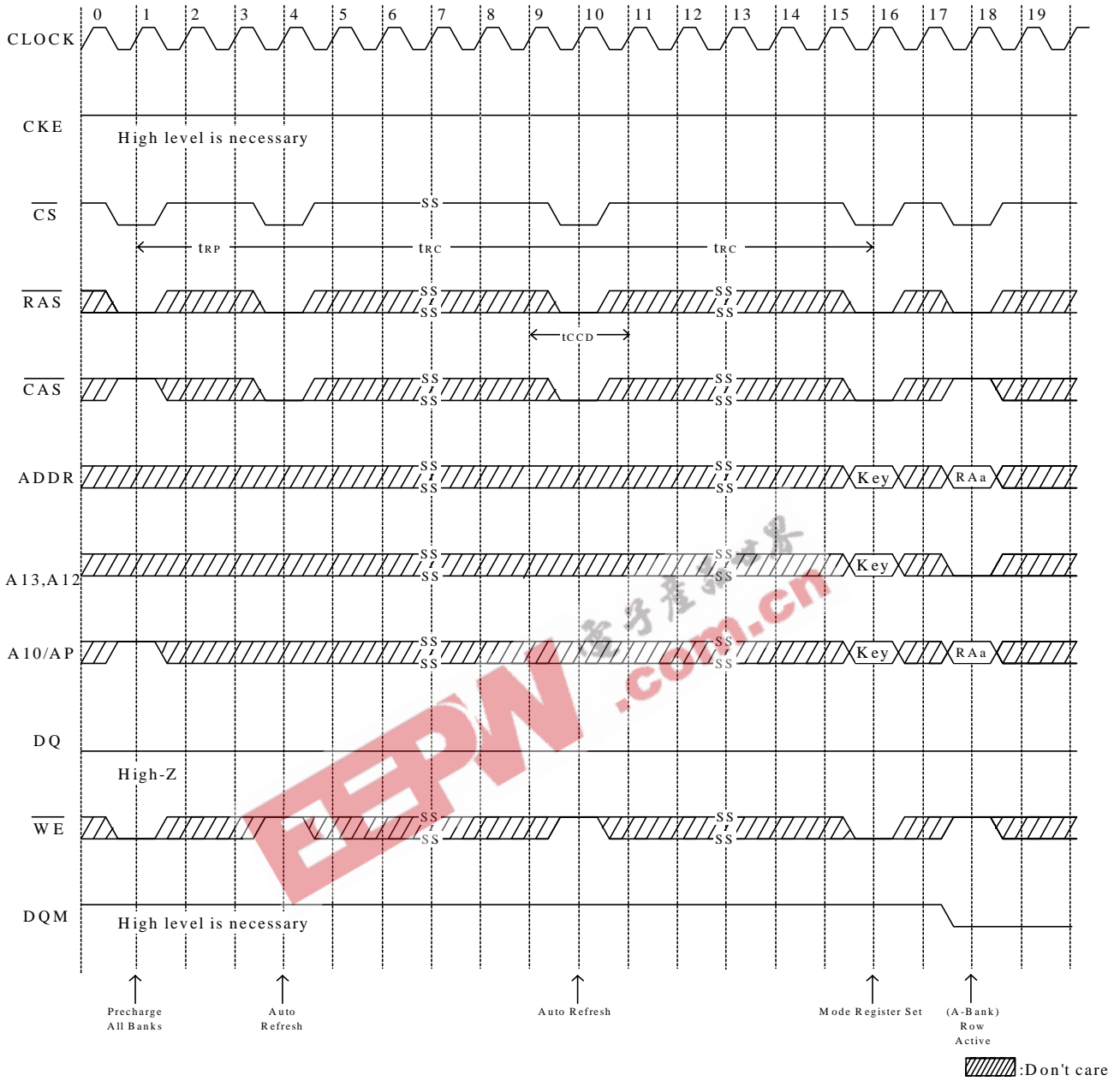
A10	Auto-Precharge
0	Disable (End of burst)
1	Enable (End of burst)

A13	A12	Operation
0	0	Enable read/write command for bank A .
1	0	Enable read/write command for bank B .
0	1	Enable read/write command for bank C .
1	1	Enable read/write command for bank D .

4. A10/AP and A13~A12 control bank precharge when precharge command is asserted.

A10/AP	A13	A12	precharge
0	0	0	Bank A
0	1	0	Bank B
0	0	1	Bank C
0	1	1	Bank D
1	X	X	All Banks

Power Up Sequence



Read & Write Cycle at Same Bank @Burst Length = 4

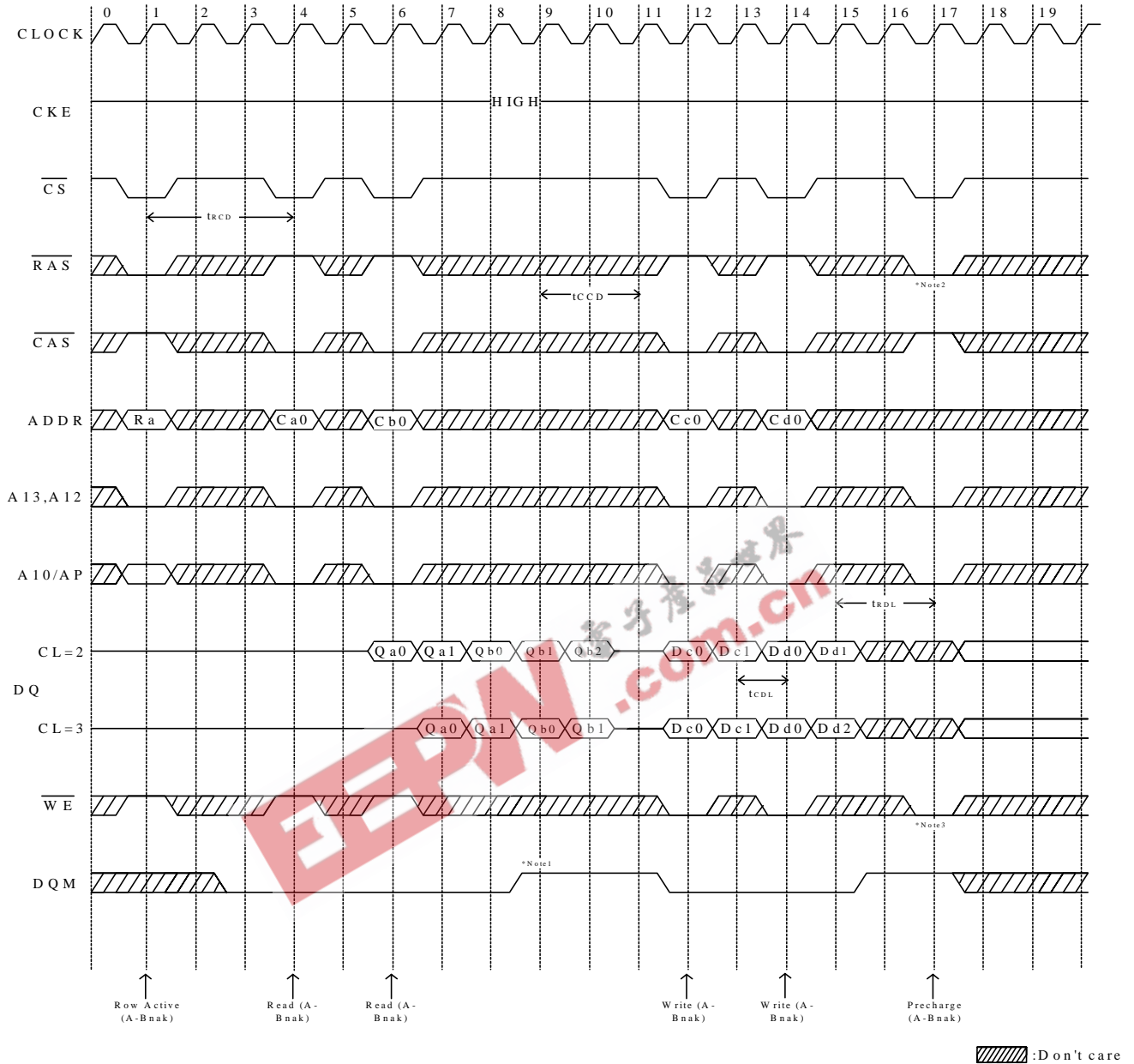


- \*Note : 1. Minimum row cycle times is required to complete internal DRAM operation.
- 2. Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clock.
- 3. Access time from Row active command.  $t_{CC} * (t_{RCD} + \text{CAS latency} - 1) + t_{SAC}$
- 4. Output will be Hi-Z after the end of burst.(1,2,4,8 bit burst)

Burst can't end in Full Page Mode.

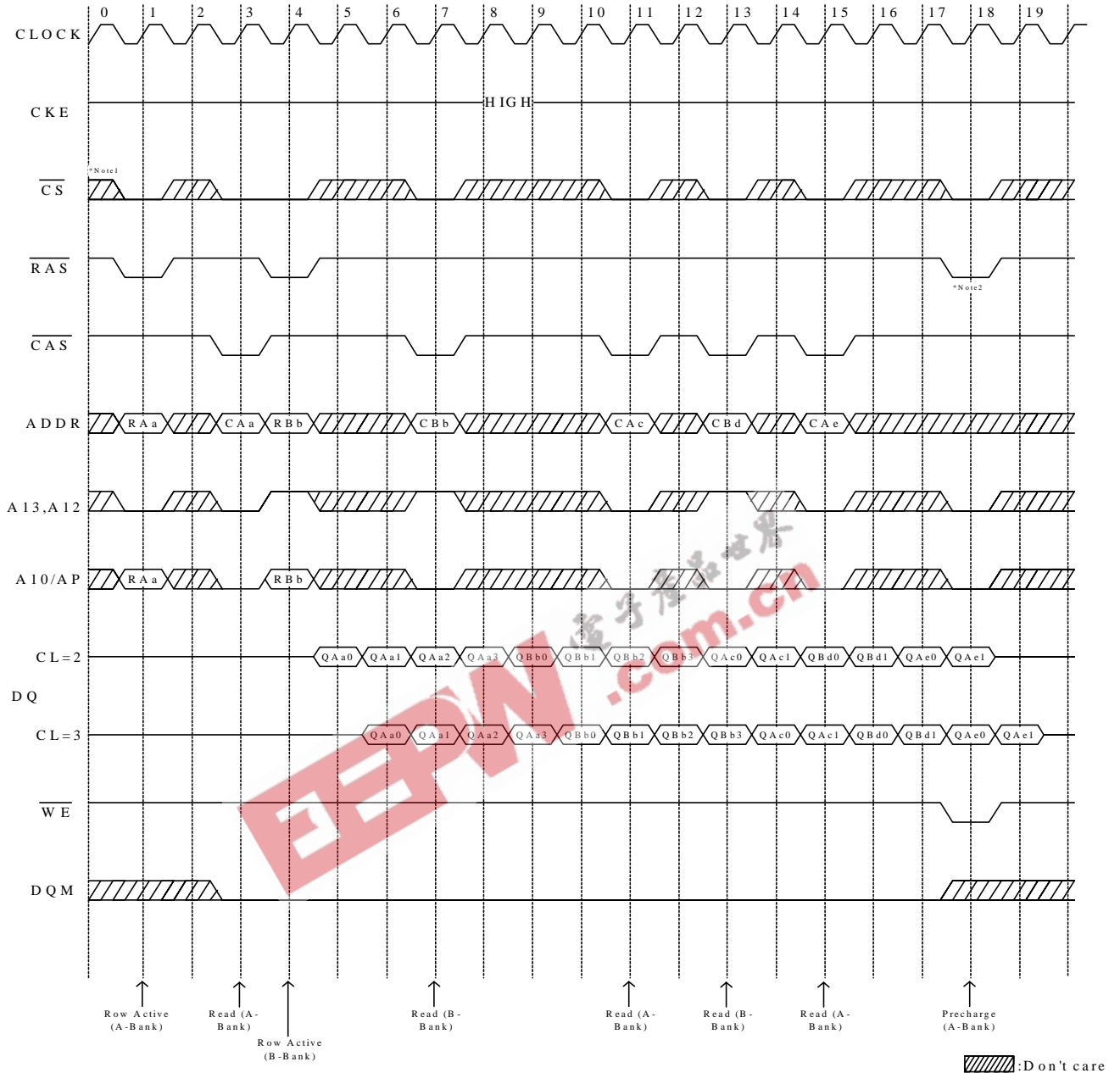


Page Read & Write Cycle at Same Bank @ Burst Length = 4



- \*Note : 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, trDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

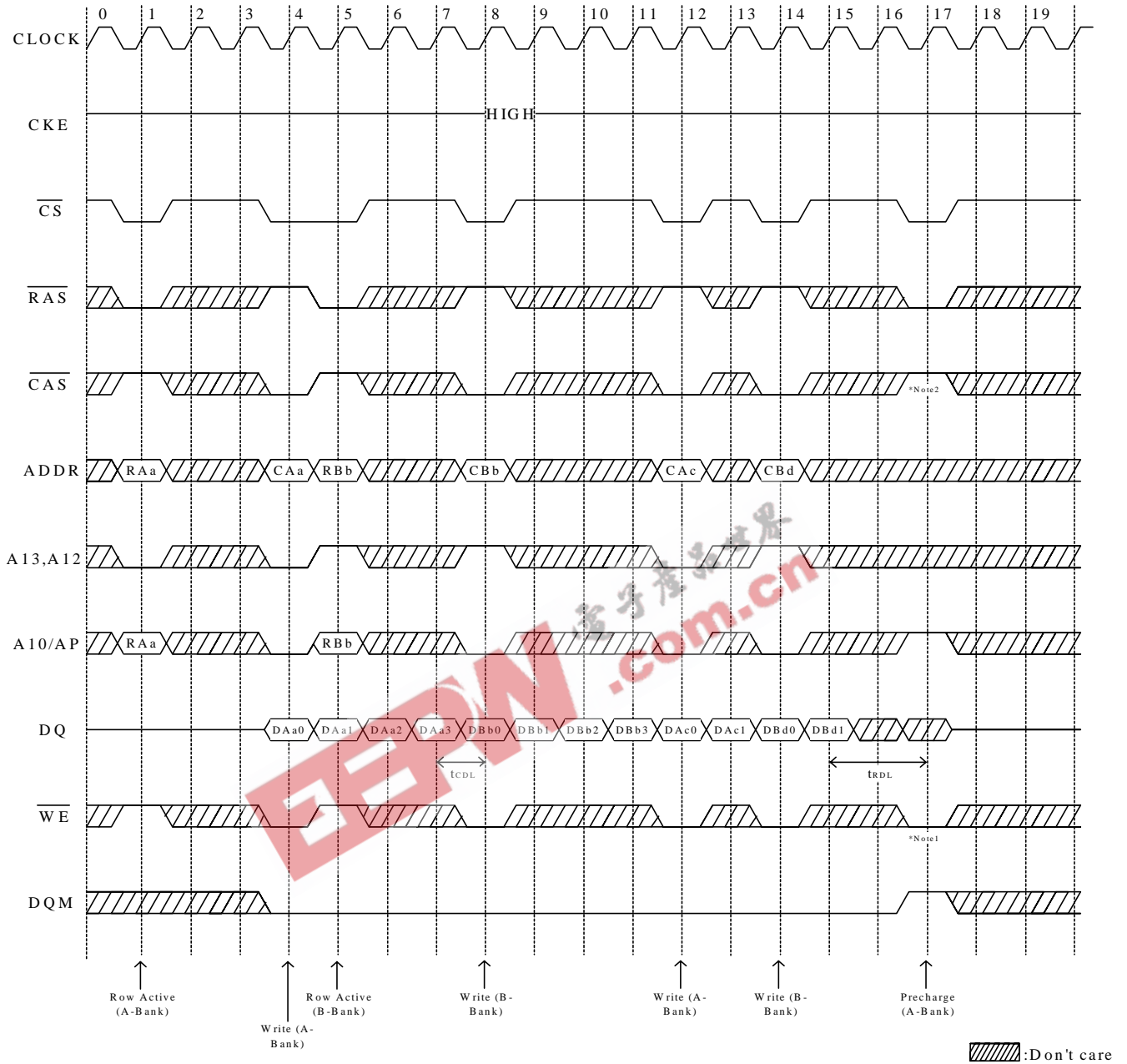
Page Read Cycle at Different Bank @ Burst Length = 4



\*Note : 1.  $\overline{CS}$  can be don't cared when  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  are high at the clock high going edge.

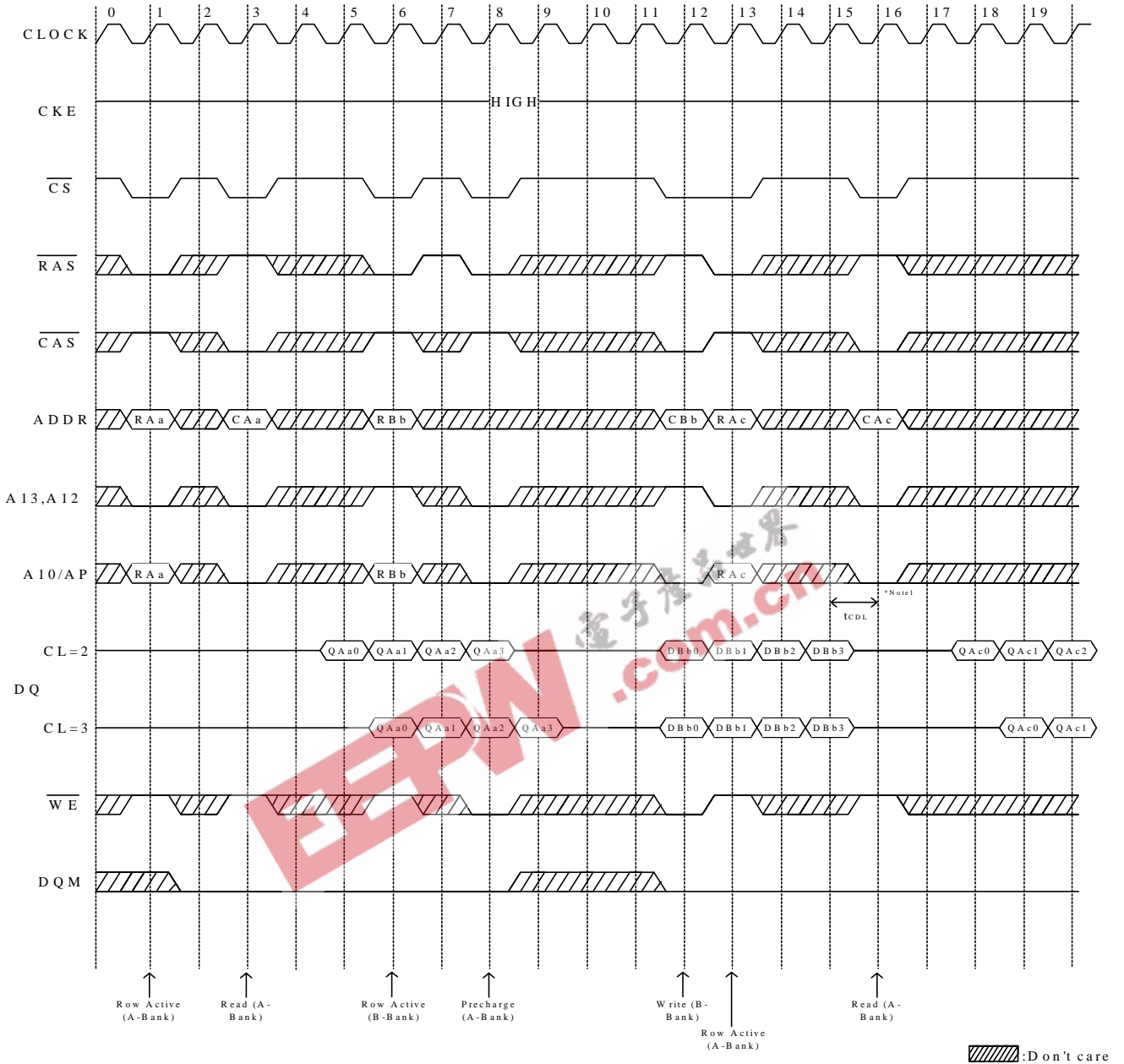
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write cycle at Different Bank @ Burst Length = 4



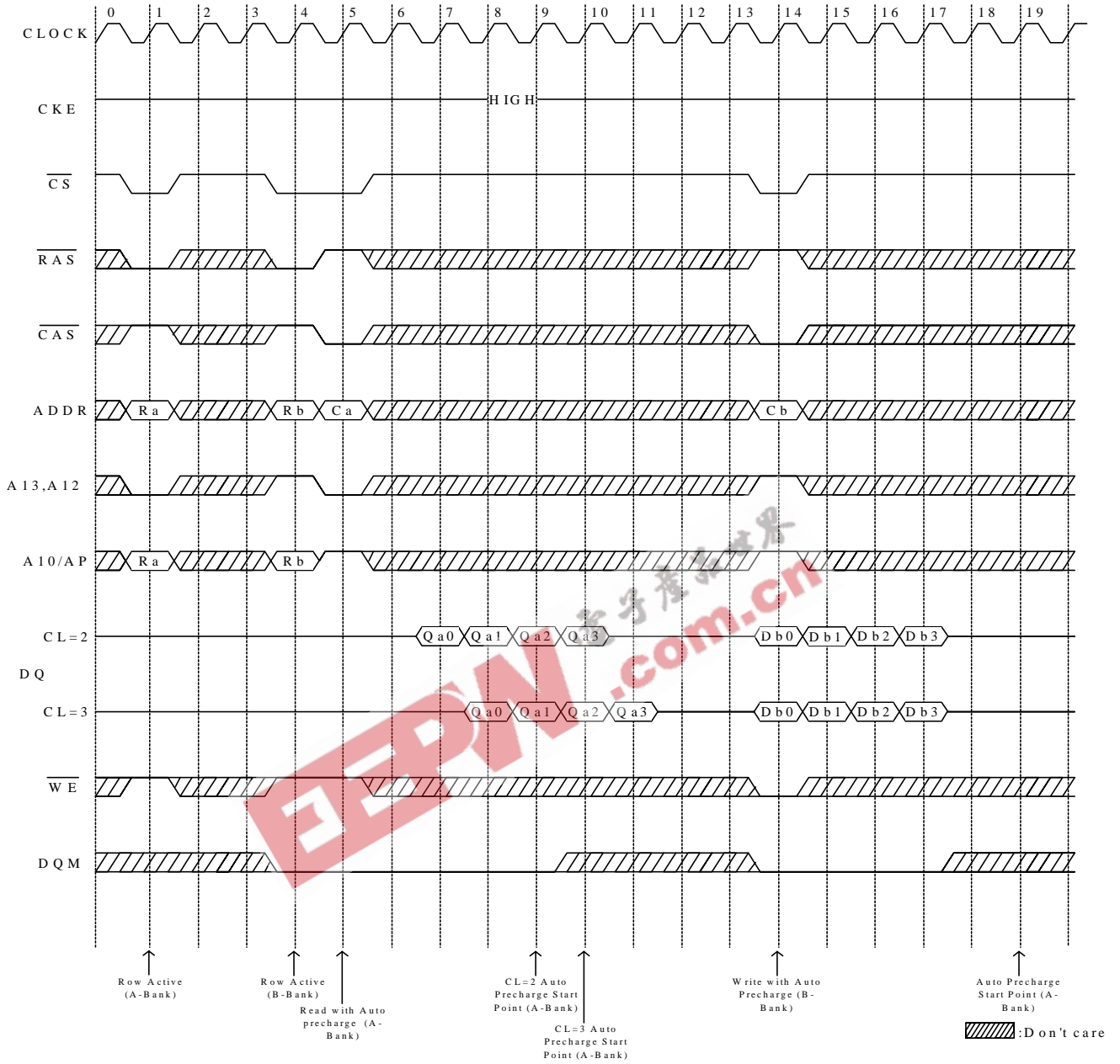
- \*Note : 1. To interrupt burst write by row precharge, DQM should be asserted to mask invalid input data.  
 2. To interrupt burst write by row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



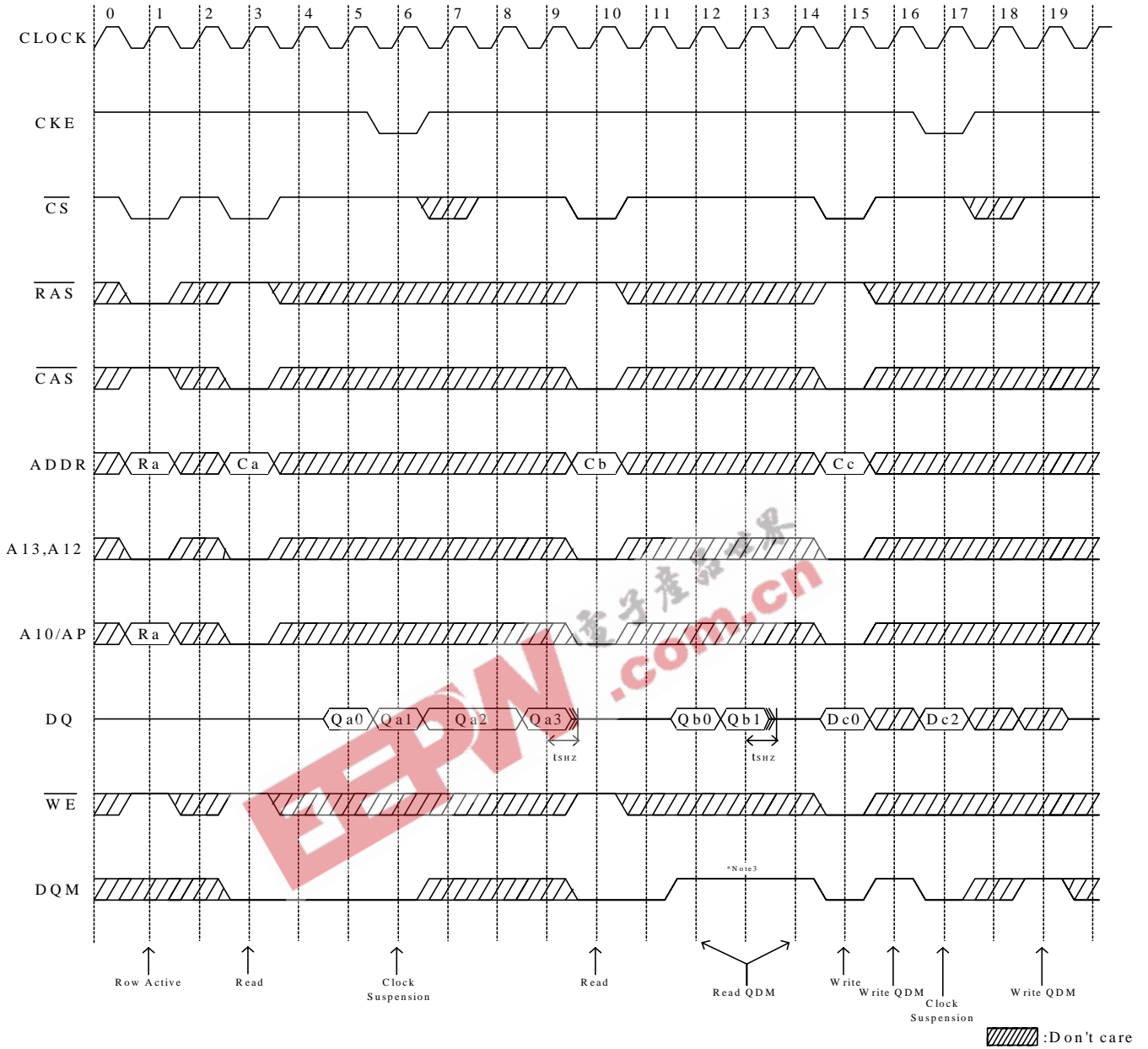
\*Note : 1.  $t_{CDL}$  should be met to complete write.

**Read & Write Cycle with Auto Precharge @ Burst Length = 4**



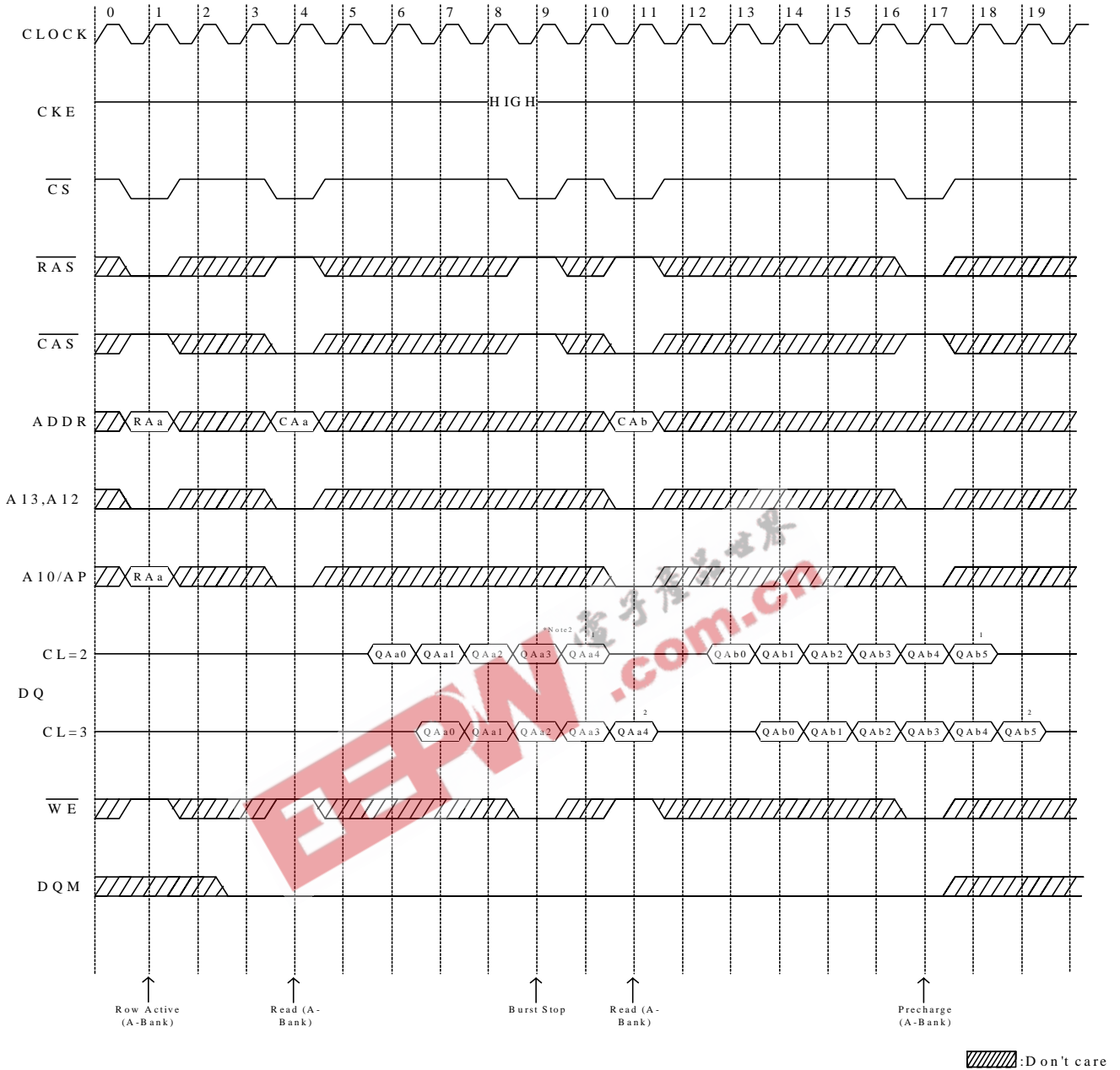
\*Note : 1. tCDL should be controlled to meet minimum tRAS before internal precharge start.  
(In the case of Burst Length = 1 & 2)

Clock suspension & DQM Operation Cycle @ CAS Latency = 2 ,Burst Length = 4



\*Note 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Burst Length=Full Page



\*Note : 1. Burst can't end in full page mode, so auto precharge can't issue.

2. About the valid DQs after burst stop, it is same as the case of  $\overline{\text{RAS}}$  interrupt.

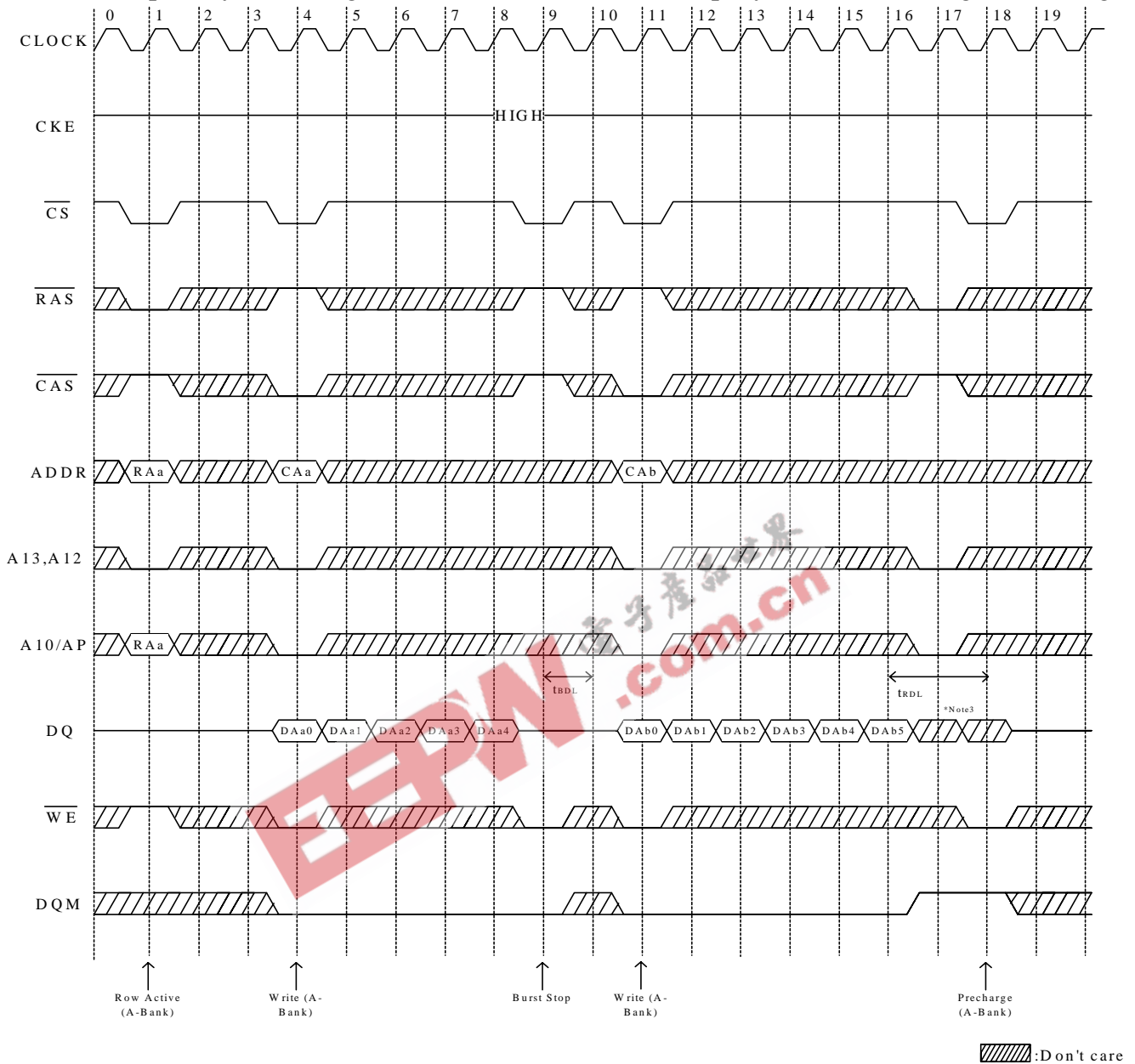
Both cases are illustrated above timing diagram. See the table 1,2 on them.

But at burst write, burst stop and  $\overline{\text{RAS}}$  interrupt should be compared carefully.

Refer the timing diagram of 'Full Page write burst stop cycle'.

3. Burst stop is valid at every burst length.

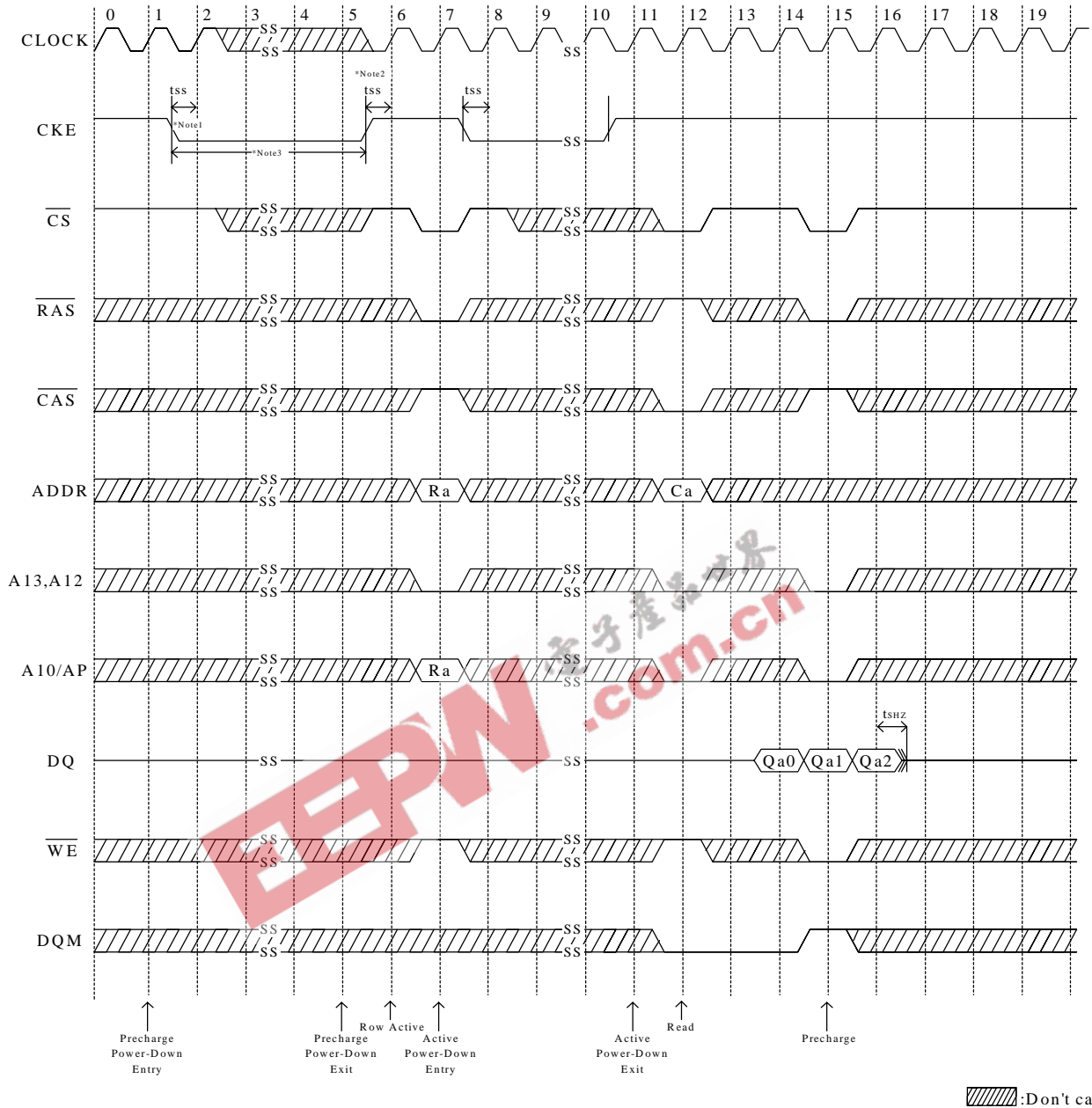
Write Interrupted by Prechareg Command & Write Burst Stop Cycle @ Burst Length=Full Page



- \*Note : 1. Burst can't end in full page mode, so auto precharge can't issue.
- 2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL. DQM at write interrupted by precharge command is needed to prevent invalid write. Input data after Row precharge cycle will be masked internally.
- 3. Burst stop is valid at every burst length.

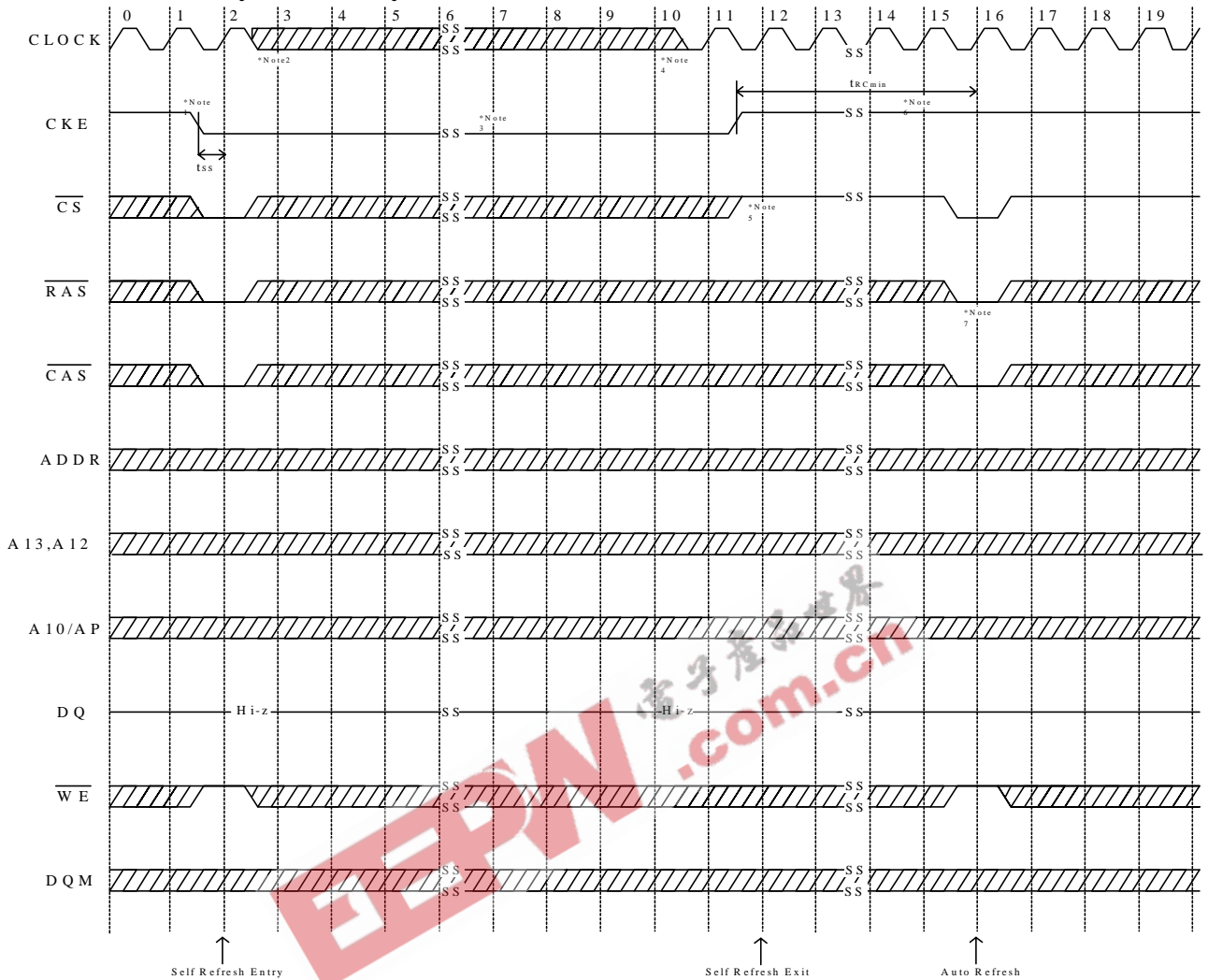


Active/ Precharge Power Down Mode @ CAS latency = 2, Butsr length = 4



- \*Note : 1. Both banks should be in idle state prior to entering precharge power down mode.
- 2. CKE should be set high at least 1CLK+tSS prior to Row active command.
- 3. Can not violate minimum refresh specification.(64ms)

Self Refresh Entry & Exit Cycle



: Don't care

\*Note : TO ENTER SELF REFRESH MODE

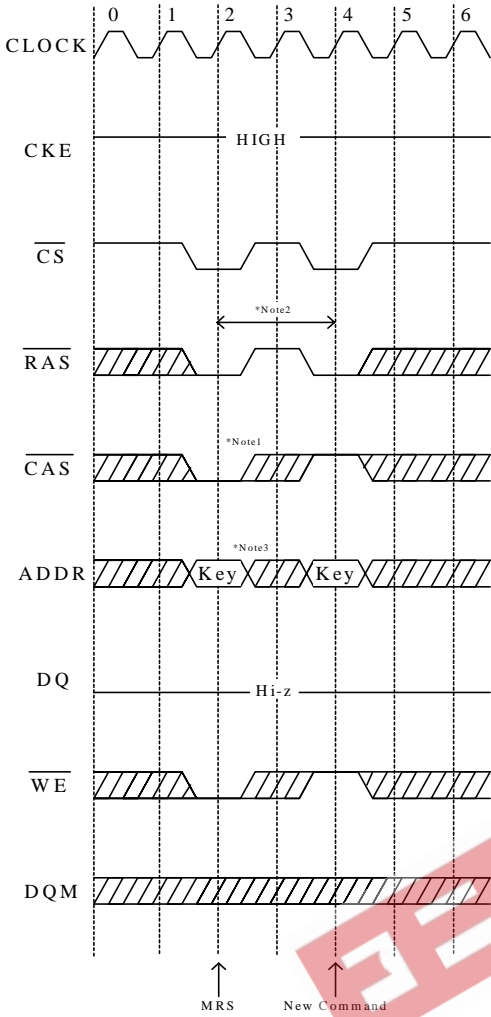
1.  $\overline{CS}$ ,  $\overline{RAS}$  &  $\overline{CAS}$  with  $\overline{CKE}$  should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for  $\overline{CKE}$ .
3. The device remains in self refresh mode as long as  $\overline{CKE}$  stays 'Low'.

Cf.) Once the device enters self refresh mode, minimum  $t_{RAS}$  is required before exit from self refresh.

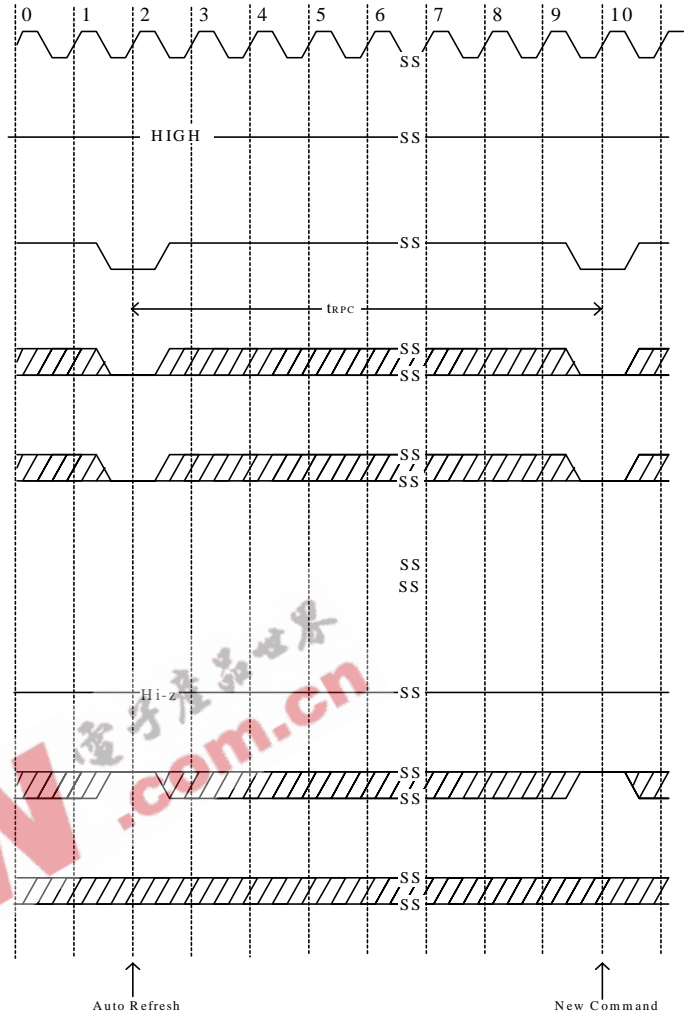
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning  $\overline{CKE}$  high.
5.  $\overline{CS}$  starts from high.
6. Minimum  $t_{RC}$  is required after  $\overline{CKE}$  going high to complete self refresh exit.
7. Burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



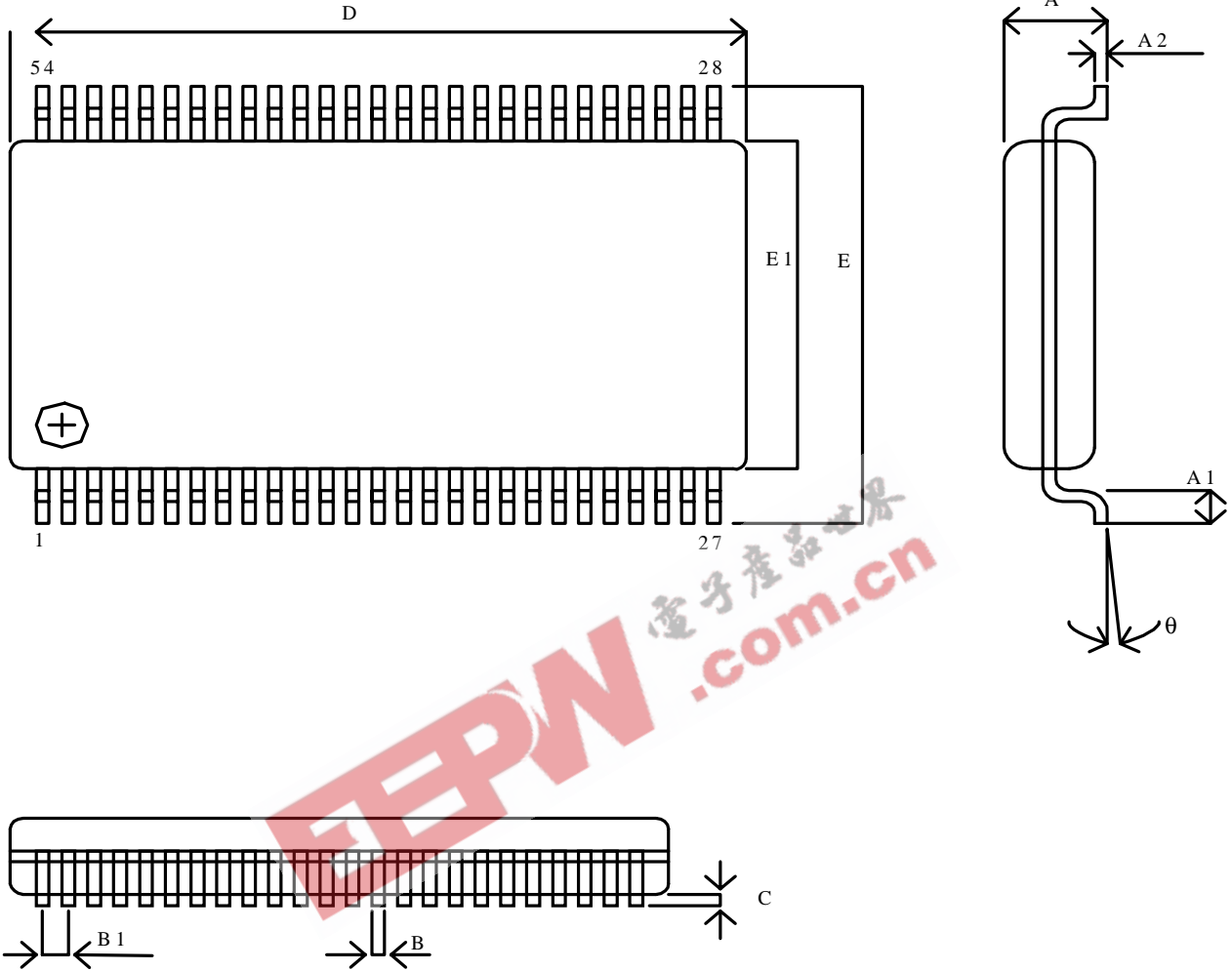
▨: Don't care

\*Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

- \*Note :
1. CS, RAS, CAS & WE activation at the same clock cycle with address key will set internal mode register.
  2. Minimum 2 clock cycles should be met before new RAS activation.
  3. Please refer to Mode Register Set table.

**PACKAGE DIMENSIONS**  
**54 LEAD TSOP-II (400 mil)**



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.2	-	-	0.047
A1	0.4	0.5	0.6	0.016	0.020	0.024
A2	-	0.15	-	-	0.006	-
B	0.24	0.32	0.40	0.009	0.012	0.016
B1	-	0.8	-	-	0.0315	-
C	0.05	0.10	0.15	0.002	0.004	0.006
D	22.12	22.22	22.62	0.871	0.875	0.905
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.06	10.16	10.26	0.396	0.400	0.404
θ	0	-	8	0	-	8