VOLTAGE DETECTOR

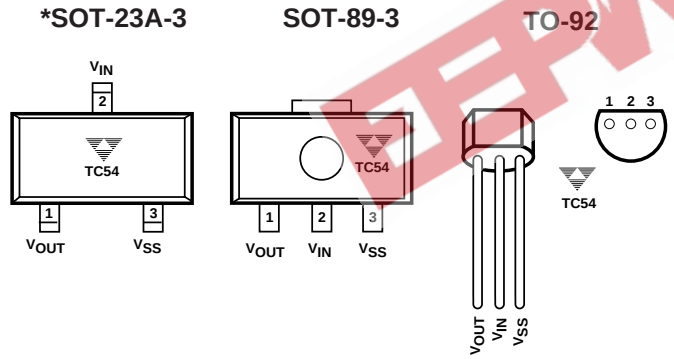
FEATURES

- **Precise Detection Thresholds .... Standard ± 2.0%**
  Custom ± 1.0%
- **Small Packages SOT-23A-3, SOT-89, TO-92**
- **Low Current Drain ..... Typ. 1µA**
- **Wide Detection Range ..... 2.1V to 6.0V**
- **Wide Operating Voltage Range ..... 1.5V to 10V**

APPLICATIONS

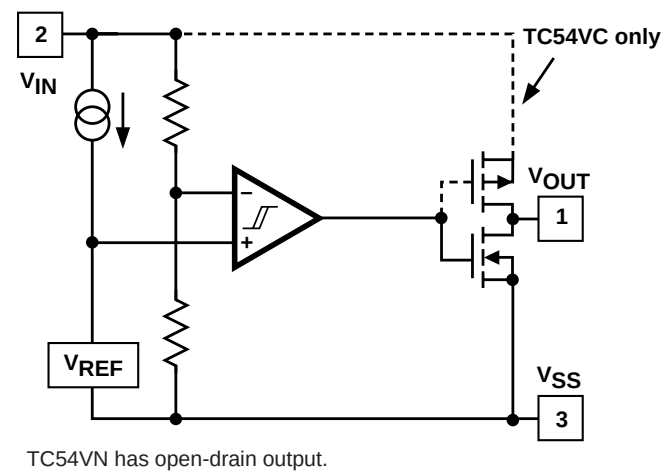
- **Battery Voltage Monitoring**
- **Microprocessor Reset**
- **System Brownout Protection**
- **Switching Circuit in Battery Backup**
- **Level Discriminator**

PIN CONFIGURATIONS



*SOT-23A-3 is equivalent to EIAJ (SC-59)

FUNCTIONAL BLOCK DIAGRAM



TC54VN has open-drain output.
TC54VC has complementary output.

GENERAL DESCRIPTION

The TC54 Series are CMOS voltage detectors, suited especially for battery-powered applications because of their extremely low 1µA operating current and small surface-mount packaging. Each part is laser trimmed to the desired threshold voltage which can be specified from 2.1V to 6.0V, in 0.1V steps.

The device includes a comparator, low-current high-precision reference, laser-trimmed divider, hysteresis circuit and output driver. The TC54 is available with either an open-drain or complementary output stage.

In operation, the TC54's output (V_{OUT}) remains in the logic HIGH state as long as V_{IN} is greater than the specified threshold voltage ($V_{\overline{DET}}$). When V_{IN} falls below $V_{\overline{DET}}$, the output is driven to a logic LOW. V_{OUT} remains LOW until V_{IN} rises above $V_{\overline{DET}}$ by an amount V_{HYST}, whereupon it resets to a logic HIGH.

ORDERING INFORMATION

PART CODE TC54 V X XX X X X XX XXX

Output form:
N = Nch Open Drain
C = CMOS Output

Detected Voltage:
Ex: 21 = 2.1V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
1 = ± 1.0% (custom)
2 = ± 2.0% (standard)

Temperature: E: – 40°C to + 85°C

Package Type and Pin Count:
CB: SOT-23A-3*, MB: SOT-89-3, ZB: TO-92-3

Taping Direction:
Standard Taping
Reverse Taping
No suffix: TO-92 Bulk

*SOT-23A-3 is equivalent to EIAJ (SC-59).

TC54

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{IN}) 12V
Output Voltage: CMOS ..... (V_{SS} – 0.3) to (V_{IN} + 0.3)
Open Drain ..... (V_{SS} – 0.3) to 12V
Output Current 50mA
Power Dissipation: ($T_A \leq 70°C$)
SOT-23A-3 ..... 240mW
SOT-89-3 ..... 400mW
TO-92 ..... 440mW
Operating Temperature ..... – 40°C to + 85°C
Storage Temperature ..... – 65°C to + 150°C
Soldering Temperature ..... 300°C, 10 seconds

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

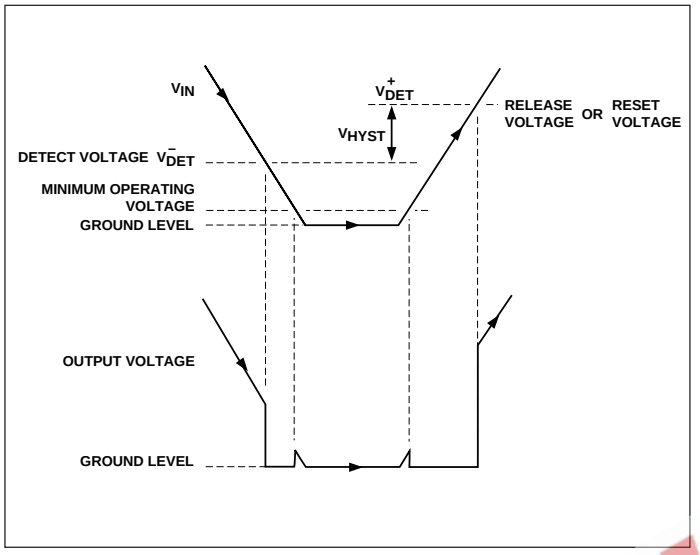
ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IN}	Operating Voltage	$V_{\overline{DET}}$ = 2.1 to 6.0V		1.5		10.0	V
I_{SS}	Quiescent Current	V_{IN} = 2.1V			1.0	3.0	µA
		3.0V			1.3	3.4	
		4.0V			1.6	3.8	
		5.0V			2.0	4.2	
$V_{\overline{DET}}$	Threshold Voltage			($V_{\overline{DET}}$) x 0.98		($V_{\overline{DET}}$) x 1.02	V
V_{HYST}	Hysteresis Range			($V_{\overline{DET}}$) x 0.02	($V_{\overline{DET}}$) x 0.05	($V_{\overline{DET}}$) x 0.08	V
I_{OUT}	Output Current	Nch V_{DS} = 0.5	V_{IN} = 2.1V		7.7		mA
			3.0V		10.1		
			4.0V		11.5		
			5.0V		13.0		
		Pch V_{DS} = 2.1V	V_{IN} = 8.0V		– 10.0		
T_C ($V_{\overline{DET}}$)	Tempco of ($V_{\overline{DET}}$)	– 40°C ≤ T_A ≤ 85°C			± 100		ppm/°C

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{IN}	Analog input. This pin is both the power supply input and the voltage to be monitored.
2	V_{OUT}	Digital output. This output goes low when V_{IN} drops below $V_{\overline{DET}}$ and returns high when V_{IN} rises above $V_{\overline{DET}}$ + V_{HYST}. (See timing chart).
3	V_{SS}	Ground terminal.

TIMING CHART



DESCRIPTION OF OPERATION

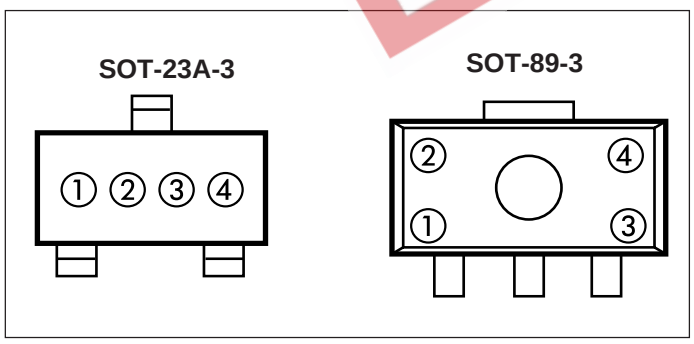
Refer to the Timing Chart below. In normal steady-state operation, when $V_{IN} > V^-_{DET}$, the output will be at a logic high. In the case of the TC54V, this is an open-drain condition. If and when the input falls below V^-_{DET}, the output will pull down (Logic 0) to V_{SS}. Generally, V_{OUT} can pull down to within 0.5V of V_{SS} at rated output current and input voltage. (See the Electrical Characteristics section).

The output, V_{OUT}, will stay valid until the input voltage falls below the Minimum Operating Voltage, V_{IN}(MIN), of 1.5V. Below this minimum operating voltage, the output is undefined. During power-up or anytime V_{IN} has fallen below V_{IN} (MIN), V_{OUT} will remain undefined until V_{IN} rises above V_{IN}(MIN), at which time the output will become valid. V_{OUT} will be in its active low state while V_{IN}(MIN) < V_{IN} < V^+_{DET}. ($V^+_{DET} = V^-_{DET} + V_{HYST}$). If and when the input rises above V^+_{DET}, the output will assume its inactive state. (High for TC54VC, open-drain for TC54VN).

APPLICATIONS

Refer to TelCom Semiconductor Application Note #2, *Using the TC54 Voltage Detector.*

MARKING



① = output (Nch or CMOS) plus first voltage digit

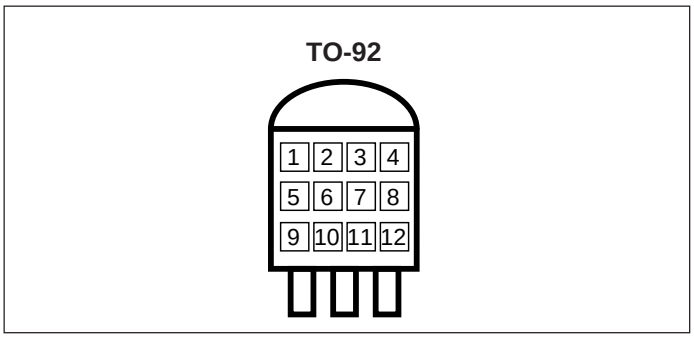
	2	3	4	5	6
Nch	M	N	P	R	S
CMOS	C	D	E	F	H

ex: CMOS 3.x = ⓓ◯◯◯

② = first voltage decimal (0-9)

ex: CMOS 3.4 = ⓓ④◯◯

③ & ④ = assembly lot number



①, ② & ③ = 54_ (fixed)

④ = output (C = CMOS, N = Nch)

⑤ = first voltage digit (2-6)

⑥ = first voltage decimal (0-9)

⑦ = extra feature code : fixed : 0

⑧ = detecting accuracy
1 = ± 1.0% (custom), 2 = ± 2.0% (standard)

⑨, ⑩, ⑪ & ⑫ = assembly lot number