

TC40H375 4-BIT BISTABLE LATCH

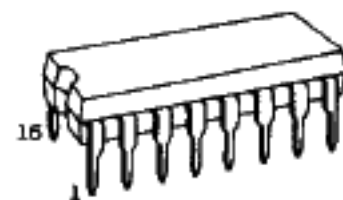
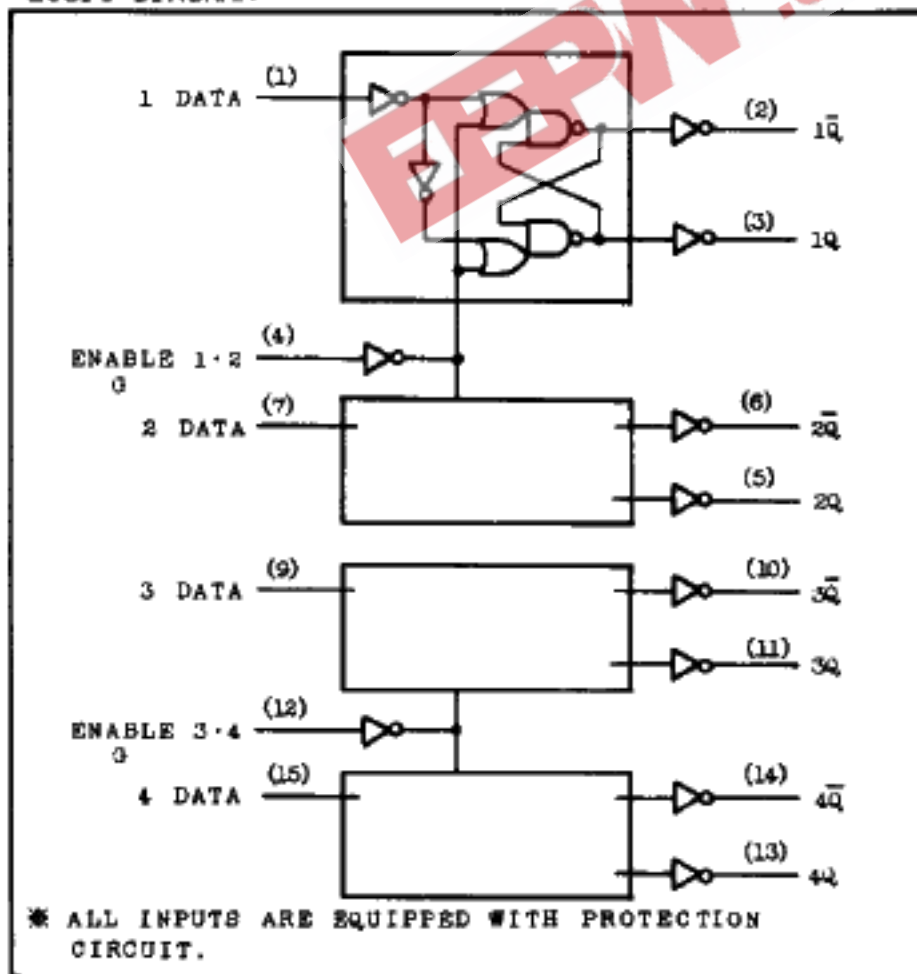
The TC40H375 is a 4-bit latch having ENABLE input terminal common in two circuits.

When ENABLE input is at "H" level, DATA input is transmitted to output as it is. If ENABLE input is transferred from "H" level to "L" level, latch holds input DATA immediately before falling. When ENABLE input is at "L" level, output does not change even if input DATA changes.

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP)/180 (MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$
Lead Temp./Time	T_{sol}	$260^{\circ}C \cdot 10 \text{ sec}$	

LOGIC DIAGRAM

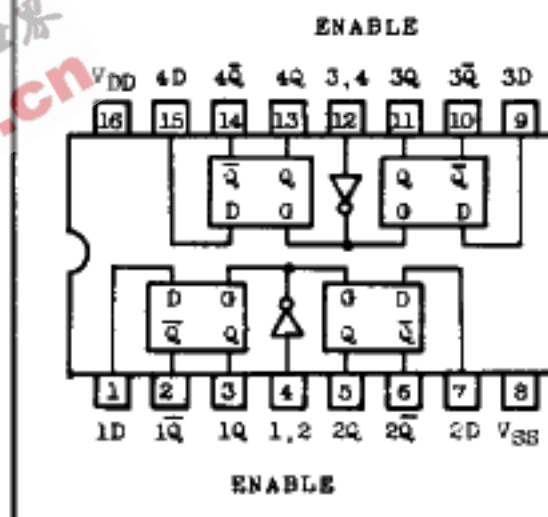


DIP16 (3D16A-P)



MFP16 (P160C-P)

PIN CONNECTION



TRUTH TABLE

INPUT		OUTPUT	
DATA	ENABLE	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	No Change	

X=Don't Care

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RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UN
Supply Voltage	V _{DD}	-	2.0	-	8.0	
Input Voltage	V _{IN}	-	0	-	V _{DD}	
Operating Temperature	T _{opr}	-	-40	-	85	

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

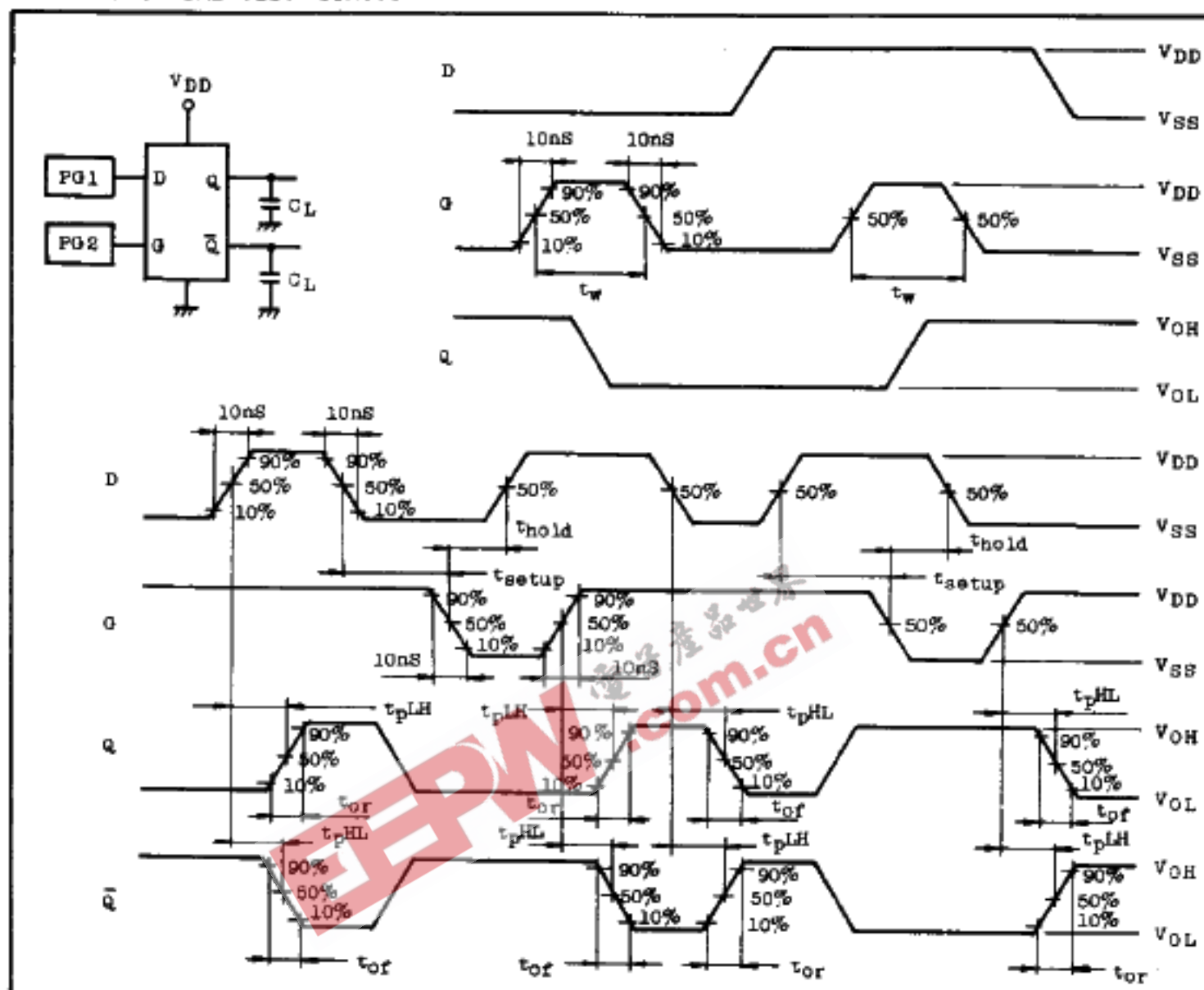
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{SS} , V _{DD}	5	-1.4	-	-1.1	-	-	-0.8	-
Input Voltage	High Level	V _{IH}	5	4.0	-	4.0	-	-	4.0	-
	Low Level	V _{IL}								
Input Current	"H" Level	I _{IH}	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0
	"L" Level	I _{IL}	8	-	-0.3	-	10 ⁻⁵	-0.3	-	-1.0
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	12.5	-	10 ⁻³	12.5	-	75

* All valid input combinations.

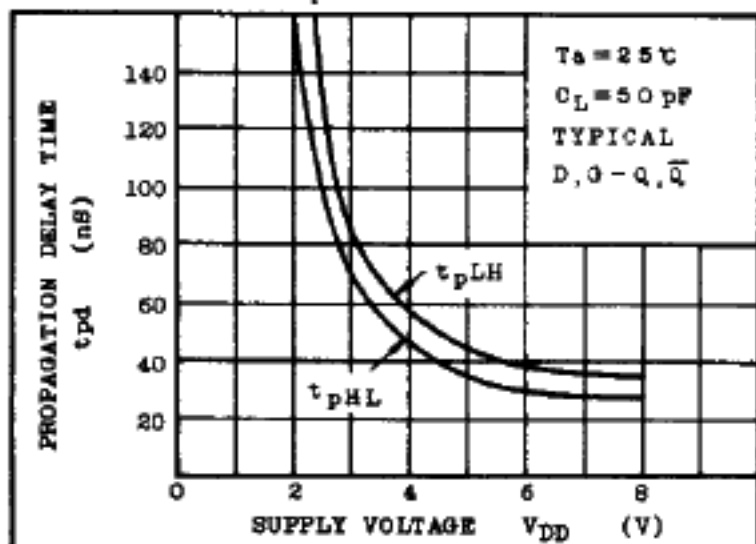
SWITCHING CHARACTERISTICS (T_a=25°C, V_{DD}=5V, C_L=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.
Output Rise Time	t _{or}		-	18	35
Output Fall Time	t _{of}		-	15	30
Propagation Delay Time	Low-High Level	t _{pLH}	-	43	65
	High-Low Level	t _{pHL}			
Propagation Delay Time	Low-High Level	t _{pLH}	-	43	65
	High-Low Level	t _{pHL}			
Minimum Enable Pulse Width	t _w		-	40	60
Minimum Hold Time	t _{hold}		-	-	6
Minimum Set-up Time	t _{set-up}		-	25	44
Input Capacitance	C _{IN}		-	5	

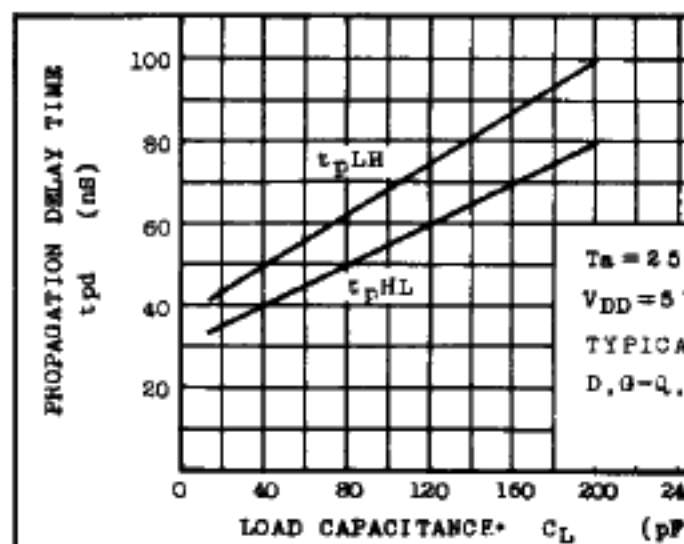
SWITCHING TIME TEST CIRCUIT AND WAVEFORM



$t_{pd} - V_{DD}$



$t_{pd} - C_L$



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