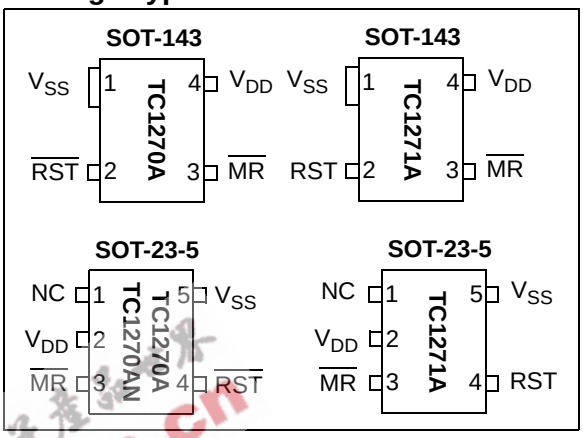
TC1270A/70AN/71A

Voltage Supervisor with Manual Reset Input

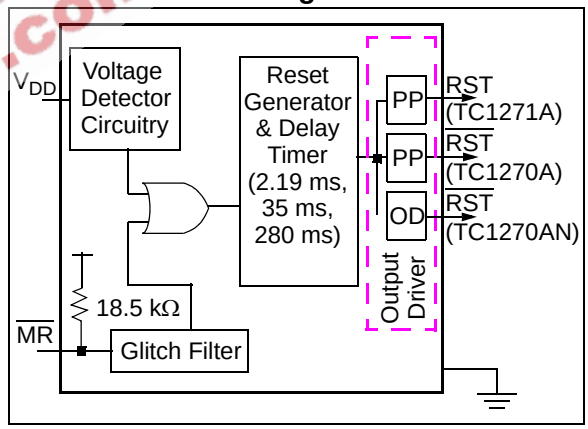
Features:

- Precision voltage monitor
  - 2.63V, 2.93V, 3.08V, 4.38V and 4.63V trip points (Typical)
- Manual Reset input
- Reset Time-out Delay:
  - Standard: 280 ms (Typical)
  - Optional: 2.19 ms, and 35 ms (Typical)
- Power Consumption ≤ 15 µA max
- No glitches on outputs during power-up
- Active Low Output Options:
  - Push-Pull Output and Open-Drain Output
- Active High Output Option:
  - Push-Pull Output
- Replacement for (Specification compatible with):
  - TC1270, TC1271
  - TCM811, TCM812
- Fully static design
- Low voltage operation (1.0V)
- ESD protection:
  - ≥ 4 kV Human Body Model (HBM)
  - ≥ 400V Machine Model (MM)
- Extended (E) Temperature range:
  -40°C to +125°C
- Package Options:
  - 4-lead SOT-143
  - 5-lead SOT-23
  - Pb-free Device

Package Types



Functional Block Diagram



Device Features

Device	Output		Reset Delay (ms) (Typ)(3)	Reset Trip Point (V) (3)	Voltage Range (V)	Temperature Range	Packages	Comment
	Type	Active Level						
TC1270A	Push-Pull	Low	2.19, 35, 280 (1)	4.63, 4.38, 3.08, 2.93, 2.63 (4)	1.0V to 5.5V	-40°C to +125°C	SOT-143 (2), SOT-23-5	Replaces TC1270 and TCM811
TC1270AN	Open-Drain	Low					SOT-23-5	New Option
TC1271A	Push-Pull	High					SOT-143 (2), SOT-23-5	Replaces TC1271 and TCM812

Note 1: The 280 ms Reset Delay time-out is compatible with the TC1270, TC1271, TCM811, and TCM812 devices.

2: The SOT-143 package is compatible with the TC1270, TC1271, TCM811, and TCM812 devices.

3: Custom Reset Trip Points and Reset Delays available, contact factory.

4: The TC1270/1 and TCM811/12 1.75V Trip Point Option is not supported.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD} to V_{SS}) .....+7.0V
Input Current, V_{DD}.....10 mA
Output Current, $\overline{RESET}$, RESET .....10 mA
Voltage on all inputs and outputs
w.r.t. V_{SS} ..... -0.6V to (V_{DD} + 1.0V)
Storage Temperature Range .....-65°C to +150°C
Operating Temperature Range.....-40°C to +125°C
Maximum Junction Temperature, T_S..... 150°C
ESD protection on all pins
Human Body Model ..... ≥ 4 kV
Machine Model .....≥ 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at those or any other conditions above those indicated in the operational listing of this specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.

Parameter	Sym	Min	Typ(1)	Max	Units	Test Conditions
Operating Voltage Range	V_{DD}	1.0	—	5.5	V	
Supply Current	I_{DD}	—	7	15	µA	$V_{DD} > V_{TRIP}$, for L/M/R/S/T, V_{DD} = 5.5V
		—	4.75	10	µA	$V_{DD} > V_{TRIP}$, for R/S/T, V_{DD} = 3.6V
		—	10	15	µA	$V_{DD} < V_{TRIP}$, for L/M/R/S/T
Reset Trip Point Threshold (3)	V_{TRIP}	4.54	4.63	4.72	V	TC127xAL: T_A = +25°C
		4.50	—	4.75	V	T_A = –40°C to +125°C
		4.30	4.38	4.46	V	TC127xAM: T_A = +25°C
		4.25	—	4.50	V	T_A = –40°C to +125°C
		3.03	3.08	3.14	V	TC127xAT: T_A = +25°C
		3.00	—	3.15	V	T_A = –40°C to +125°C
		2.88	2.93	2.98	V	TC127xAS: T_A = +25°C
		2.85	—	3.00	V	T_A = –40°C to +125°C
		2.72	2.77	2.82	V	TC127xA:(5) T_A = +25°C
		2.70	—	2.85	V	T_A = –40°C to +125°C
		2.58	2.63	2.68	V	TC127xAR: T_A = +25°C
		2.55	—	2.70	V	T_A = –40°C to +125°C

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.

2: $\overline{RST}$ output for TC1270A, and TC1270AN, RST output for TC1271A.

3: TC127XA refers to either the TC1270A, TC1270AN or TC1271A device.

4: Hysteresis is within the $V_{TRIP(MIN)}$ to $V_{TRIP(MAX)}$ window.

5: Custom ordered Voltage Trip Point. Minimum order volume requirement.

6: This specification allows this device to be used in PIC® microcontroller applications that require the In-Circuit Serial Programming™ (ICSP™) feature (see device-specific programming specifications for voltage requirements). The total time that the RST pin can be above the maximum device operational voltage (5.5V) is 100s. Current into the RST pin should be limited to 2 mA. It is recommended that the device operational temperature be maintained between 0°C to +70°C (+25°C preferred). For additional information, refer to Figure 2-41.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.

Parameter		Sym	Min	Typ(1)	Max	Units	Test Conditions
Reset Threshold Tempco			—	±30	—	ppm/°C	
Reset Trip Point Hysteresis (4)		V_{HYS}	—	0.3	—	%	Percentage of V_{TRIP} Voltage
$\overline{MR}$ Input High Threshold		V_{IH}	2.3	—	—	V	$V_{DD} > V_{TRIP(MAX)}$, L/M only
			0.7 V_{DD}	—	—	V	$V_{DD} > V_{TRIP(MAX)}$, R/S/T only
$\overline{MR}$ Input Low Threshold		V_{IL}	—	—	0.8	V	$V_{DD} > V_{TRIP(MAX)}$, L/M only
			—	—	0.25 V_{DD}	V	$V_{DD} > V_{TRIP(MAX)}$, R/S/T only
$\overline{MR}$ Pull-up Resistance			10	18.5	40	kΩ	
Open-Drain High Voltage on Output		V_{ODH}	—	—	13.5	V	Open-Drain Output pin only. V_{DD} = 3.0V, Time voltage > 5.5 applied ≤ 100s. Current into pin limited to 2 mA +25°C operation recommended **(Note 6)**
Reset Output Voltage Low (2)	TC1270A/ TC1270AN	V_{OL}	—	—	0.3	V	R/S/T only, I_{SINK} = 1.2 mA, V_{DD} = $V_{TRIP(MIN)}$
	TC1271A		—	—	0.3	V	R/S/T only, I_{SINK} = 1.2 mA, V_{DD} = $V_{TRIP(MAX)}$
	TC1270A/ TC1270AN		—	—	0.4	V	L/M only, I_{SINK} = 3.2 mA, V_{DD} = $V_{TRIP(MIN)}$
	TC1271A		—	—	0.3	V	L/M only, I_{SINK} = 3.2 mA, V_{DD} = $V_{TRIP(MAX)}$
	TC1270A/ TC1270AN		—	—	0.3	V	L/M only, I_{SINK} = 50 µA, V_{DD} > 1.0V
Reset Output Voltage High (2)	TC1270A	V_{OH}	0.8 V_{DD}	—	—	V	R/S/T only, I_{SOURCE} = 500 µA, V_{DD} = $V_{TRIP(MAX)}$
	TC1270A		V_{DD} - 1.5	—	—	V	L/M only, I_{SOURCE} = 800 µA, V_{DD} = $V_{TRIP(MAX)}$
	TC1271A		0.8 V_{DD}	—	—	V	I_{SOURCE} = 500 µA, $V_{DD} \leq V_{TRIP(MIN)}$
Input Leakage Current		I_{IL}	—	—	±1	µA	V_{PIN} = V_{DD}
Open-Drain $\overline{RST}$ Output Leakage		I_{OLOD}	—	—	1	µA	Open-Drain configuration only.
Capacitive Loading Specification on Output Pins		C_{IO}	—	—	50	pF	

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.

2: $\overline{RST}$ output for TC1270A, and TC1270AN, RST output for TC1271A.

3: TC127XA refers to either the TC1270A, TC1270AN or TC1271A device.

4: Hysteresis is within the $V_{TRIP(MIN)}$ to $V_{TRIP(MAX)}$ window.

5: Custom ordered Voltage Trip Point. Minimum order volume requirement.

6: This specification allows this device to be used in PIC® microcontroller applications that require the In-Circuit Serial Programming™ (ICSP™) feature (see device-specific programming specifications for voltage requirements). The total time that the RST pin can be above the maximum device operational voltage (5.5V) is 100s. Current into the RST pin should be limited to 2 mA. It is recommended that the device operational temperature be maintained between 0°C to +70°C (+25°C preferred). For additional information, refer to Figure 2-41.

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1.1 AC CHARACTERISTICS

1.1.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS

T			
F	Frequency	T	Time
E	Error		

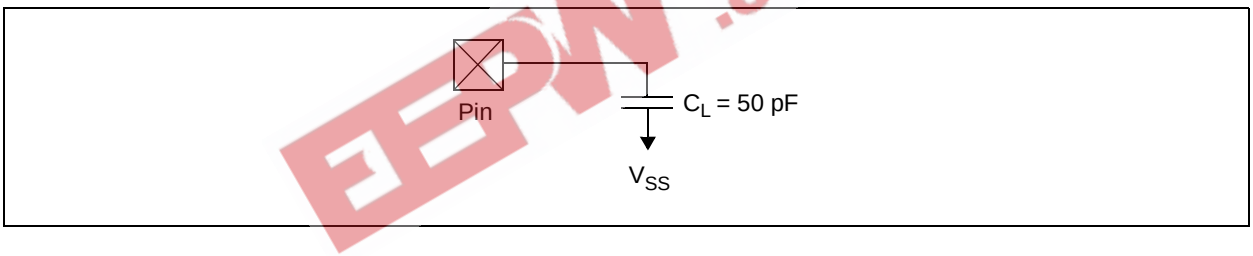
Lowercase letters (pp) and their meanings:

pp			
io	Input or Output pin	osc	Oscillator
rx	Receive	tx	Transmit
bitclk	RX/TX BITCLK	RST	Reset
drt	Device Reset Timer		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 1-1: TEST LOAD CONDITIONS



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1.1.2 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 1-2: $\overline{MR}$ PIN AND RESET PIN WAVEFORM

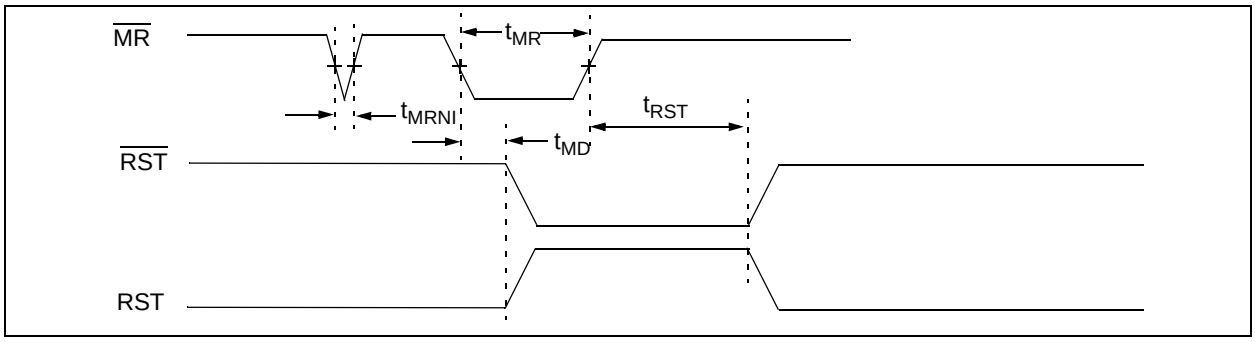
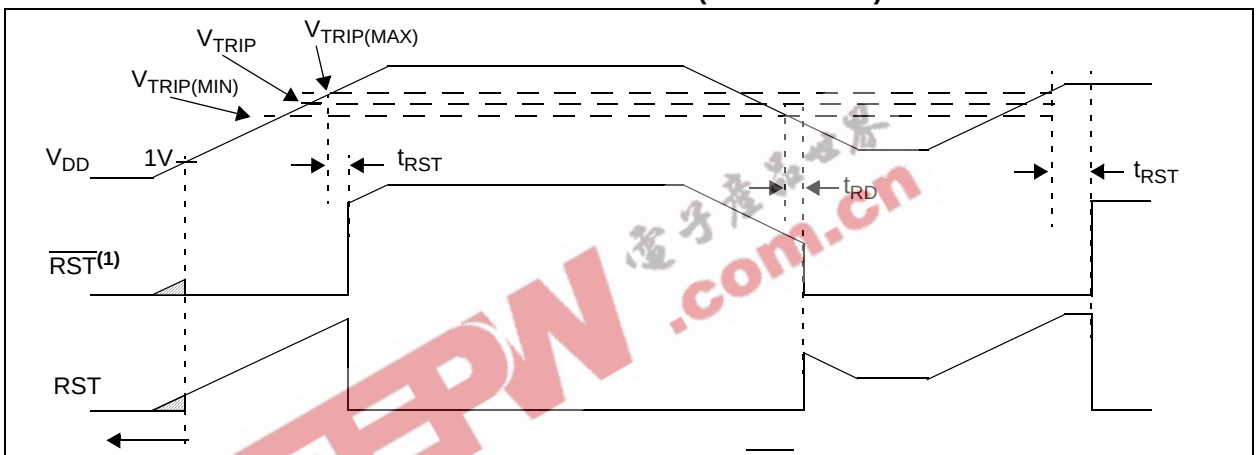


FIGURE 1-3: DEVICE VOLTAGE AND RESET PIN (ACTIVE LOW) WAVEFORM



V_{DD} < 1V is outside the device operating specification. The RST (or $\overline{RST}$) output state is unknown while V_{DD} < 1V.

Note 1: The TC1270AN requires an external pull-up resistor.

TABLE 1-1: $\overline{RESET}$ AND DEVICE RESET TIMER REQUIREMENTS

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.							
Parameter		**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Test Conditions**
V_{DD} to Reset Delay		t_{RD}	—	50	—	µs	$V_{DD} = V_{TRIP(MAX)}$ to $V_{TRIP(MIN)}$ –125 mV
Reset Active Timeout Period	TC127XAx**B**Vyy (3)	t_{RST}	1.09	2.19	4.38	ms	$V_{DD} = V_{TRIP(MAX)}$
	TC127XAx**C**Vyy (3)		17.5	35	70	ms	$V_{DD} = V_{TRIP(MAX)}$
	TC127XAxVyy (3)		140	280	560	ms	$V_{DD} = V_{TRIP(MAX)}$
$\overline{MR}$ Minimum Pulse Width		t_{MR}	10	—	—	µs	
$\overline{MR}$ Noise Immunity		t_{MRNI}	—	0.1	—	µs	
$\overline{MR}$ to Reset Propagation Delay		t_{MD}	—	0.2	—	µs	

Note 1: Unless otherwise stated, data in the Typical ("Typ") column is at 5V, +25°C.

2: $\overline{RST}$ output for TC1270A, RST output for TC1271A.

3: TC127XA refers to either the TC1270A, TC1270AN or TC1271A device. "x" indicated the selected Voltage Trip Point, while "yy" indicates the package code.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.0V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 4L-SOT-143	θ_{JA}	—	426	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

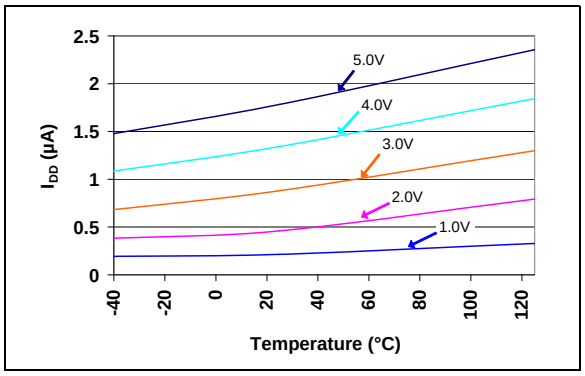

FIGURE 2-1: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

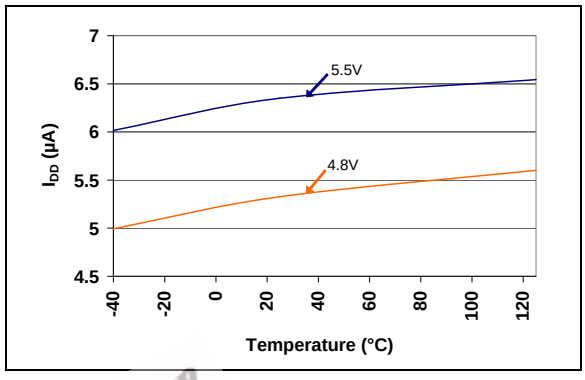

FIGURE 2-4: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

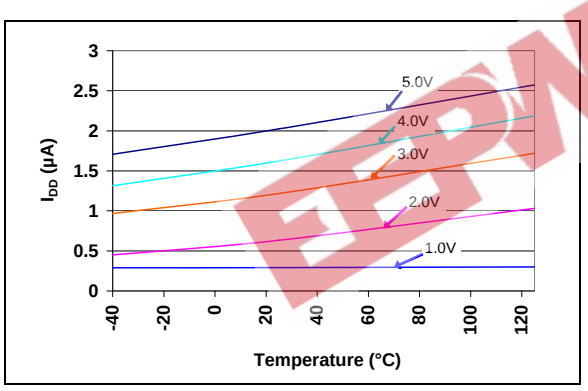

FIGURE 2-2: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

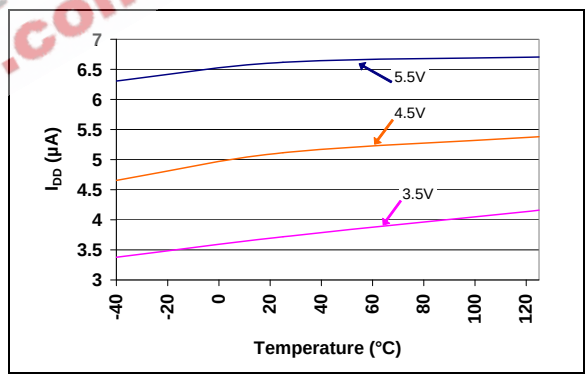

FIGURE 2-5: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

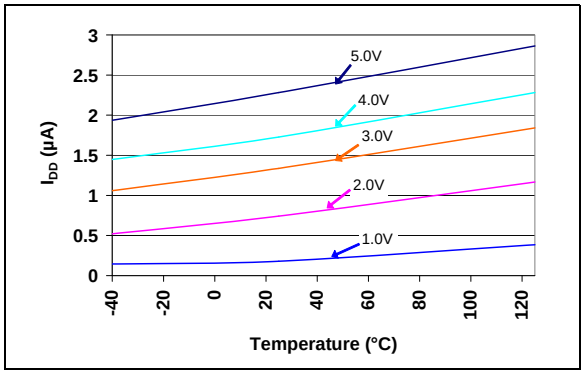

FIGURE 2-3: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

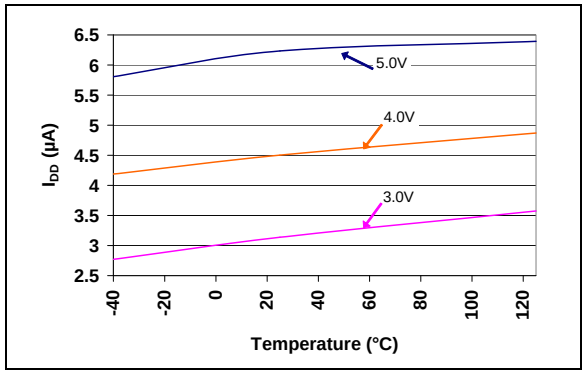

FIGURE 2-6: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

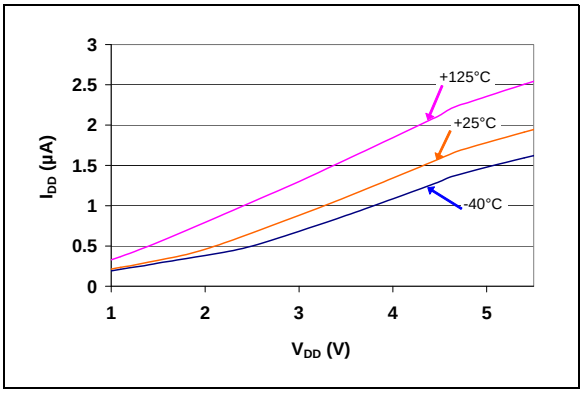

FIGURE 2-7: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

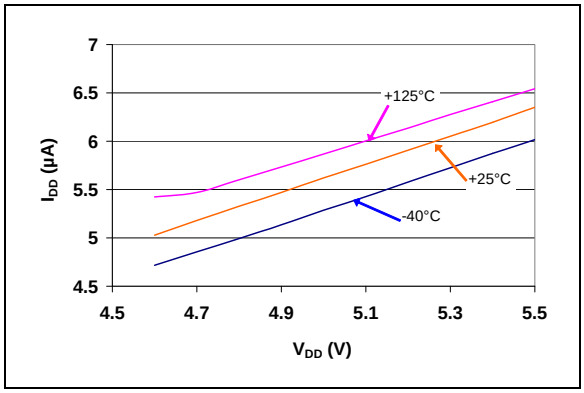

FIGURE 2-10: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

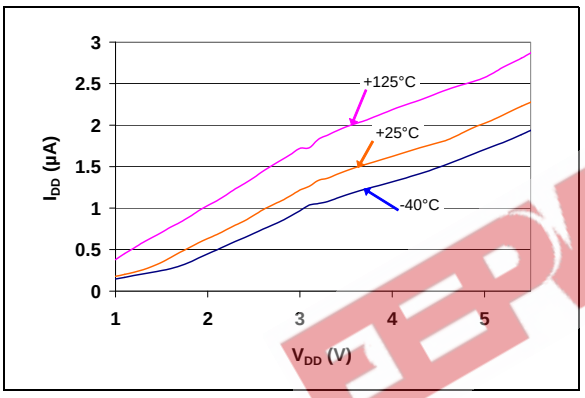

FIGURE 2-8: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

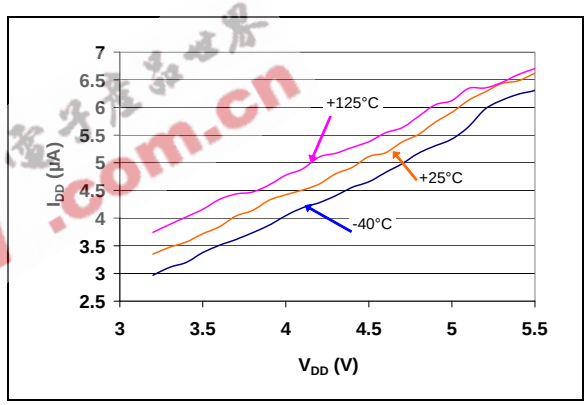

FIGURE 2-11: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

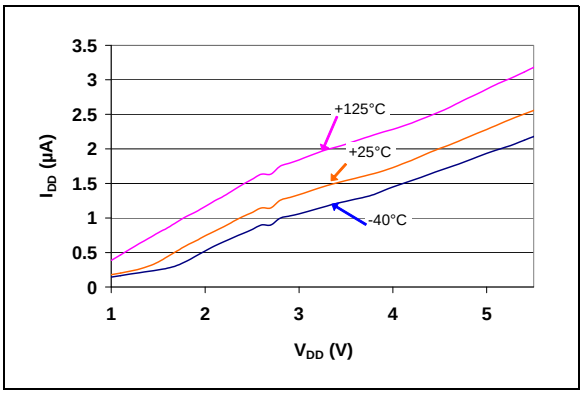

FIGURE 2-9: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

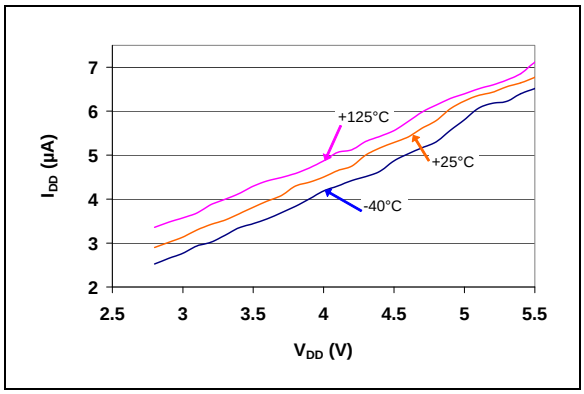

FIGURE 2-12: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

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Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

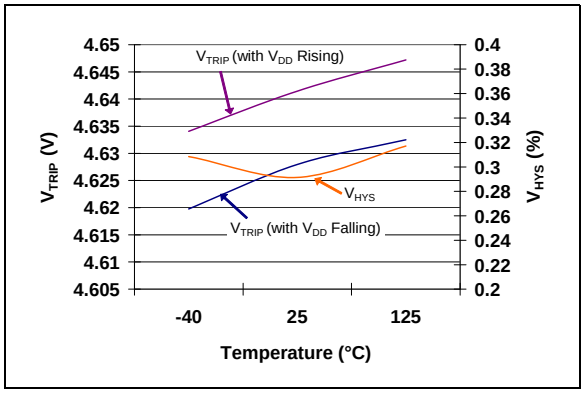

FIGURE 2-13: *V_{TRIP} and V_{HYS} vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

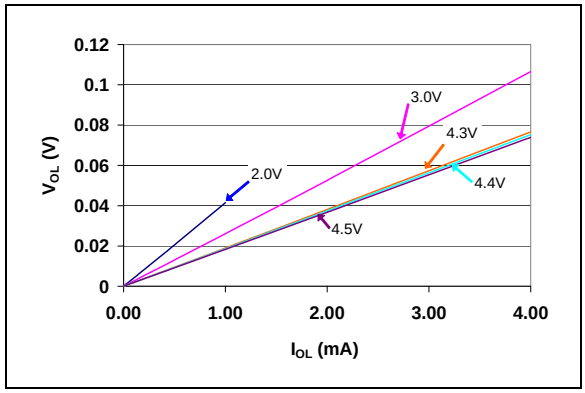

FIGURE 2-16: *V_{OL} vs. I_{OL} (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

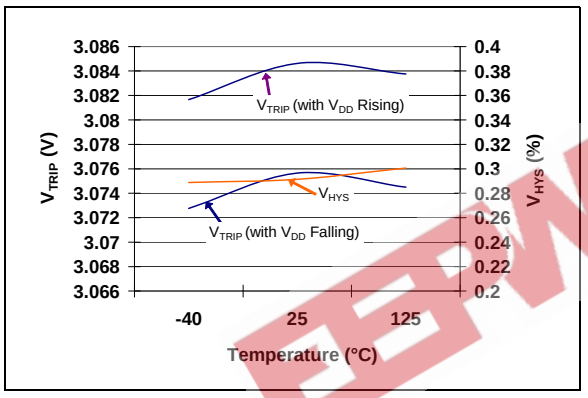

FIGURE 2-14: *V_{TRIP} and V_{HYS} vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

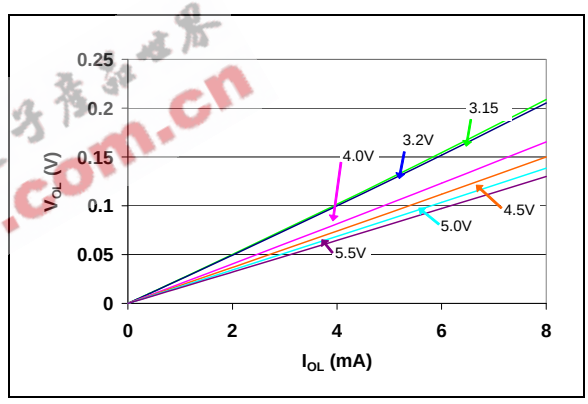

FIGURE 2-17: *V_{OL} vs. I_{OL} (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

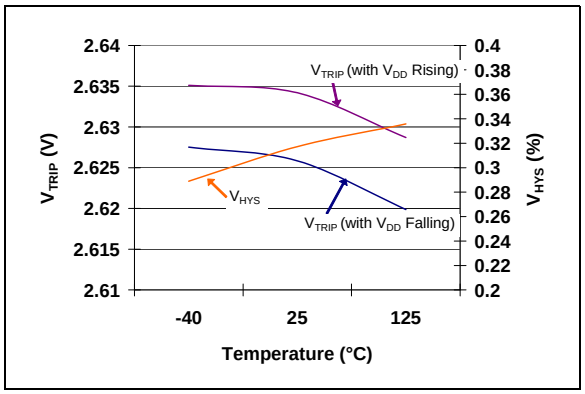

FIGURE 2-15: *V_{TRIP} and V_{HYST} vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

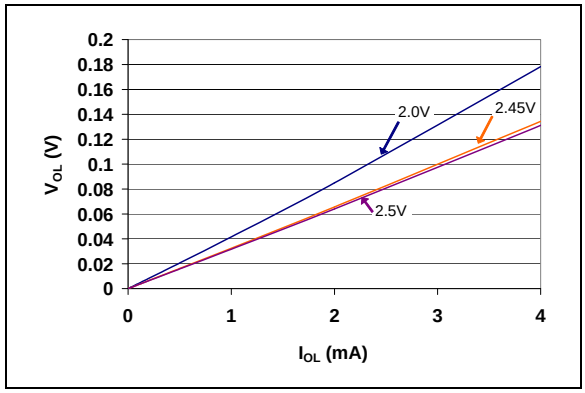

FIGURE 2-18: *V_{OL} vs. I_{OL} (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

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Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

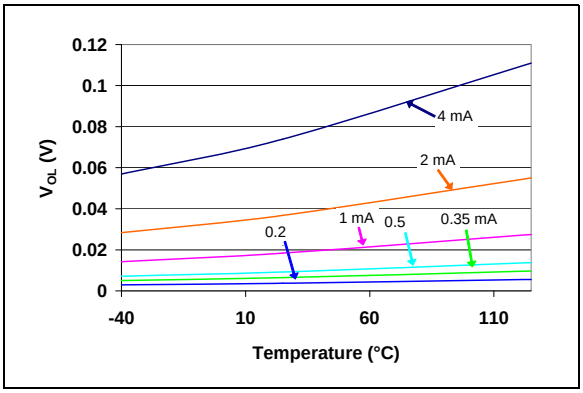

FIGURE 2-19: *V_{OL} vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.). @ V_{DD} = 4.5V).*

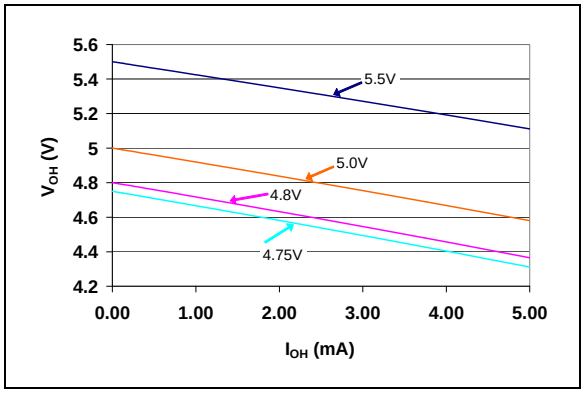

FIGURE 2-22: *V_{OH} vs. I_{OL} (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.) @ +25°C).*

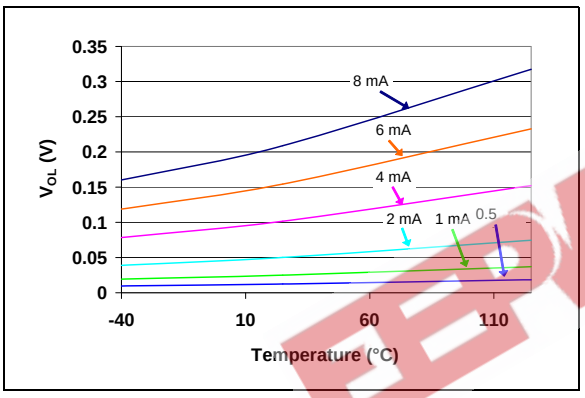

FIGURE 2-20: *V_{OL} vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.). @ V_{DD} = 2.7V).*

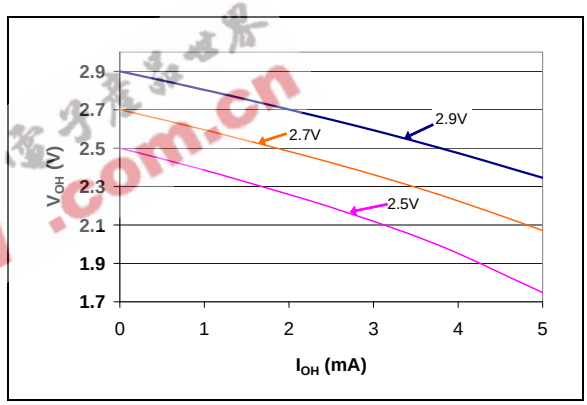

FIGURE 2-23: *V_{OH} vs. I_{OH} (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.) @ +25°C).*

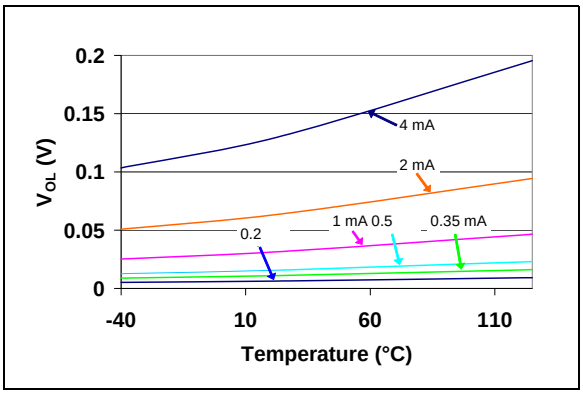

FIGURE 2-21: *V_{OL} vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.). @ V_{DD} = 1.8V).*

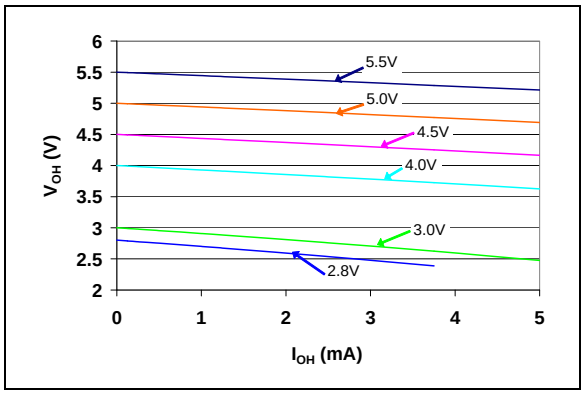

FIGURE 2-24: *V_{OH} vs. I_{OH} (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.) @ +25°C).*

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Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

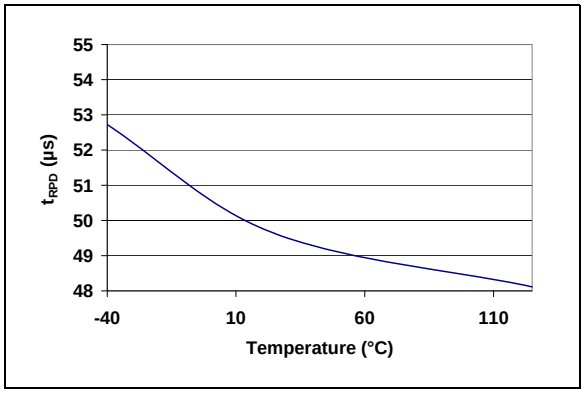

FIGURE 2-25: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

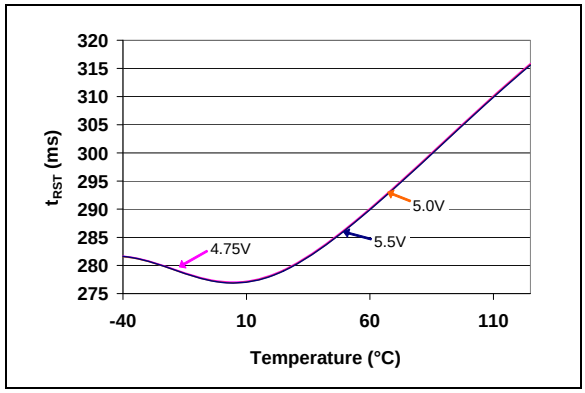

FIGURE 2-28: *Reset Timeout Period (t_{RST}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

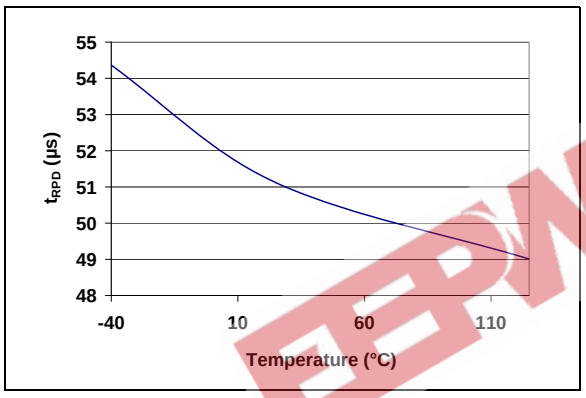

FIGURE 2-26: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

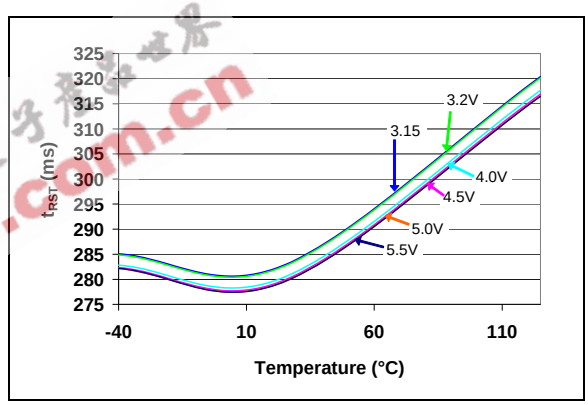

FIGURE 2-29: *Reset Timeout Period (t_{RST}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

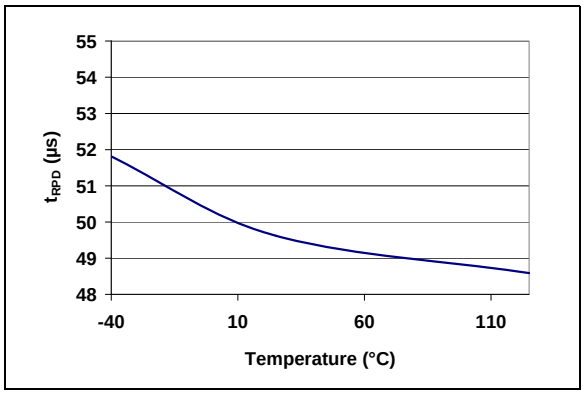

FIGURE 2-27: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

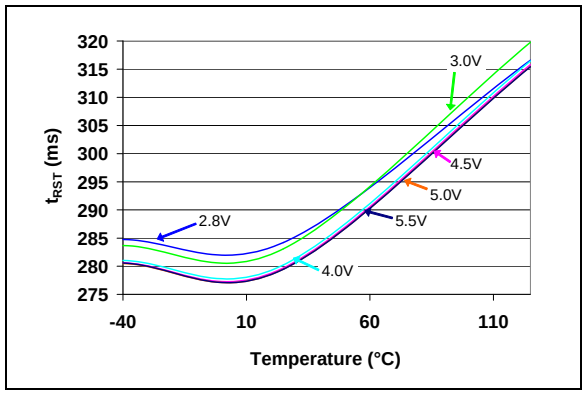

FIGURE 2-30: *Reset Timeout Period (t_{RST}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

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Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

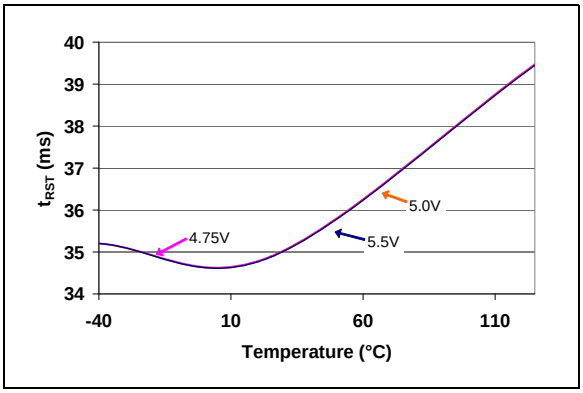

FIGURE 2-31: *Reset Timeout Period (t_{RST}) (C timeout option) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

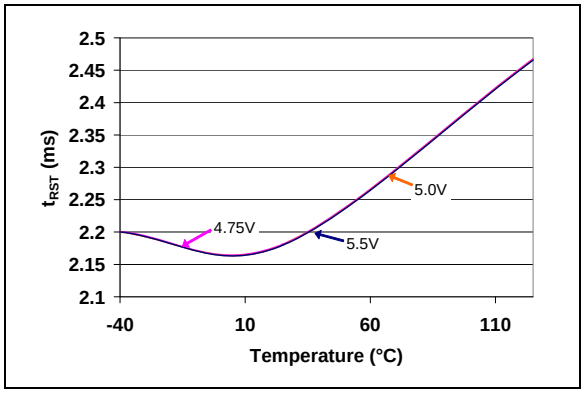

FIGURE 2-34: *Reset Timeout Period (t_{RST}) (B timeout option) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

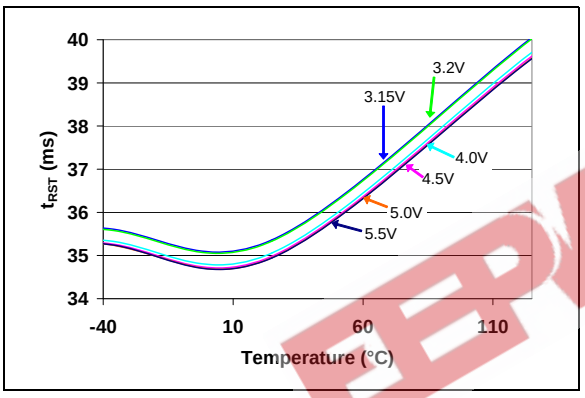

FIGURE 2-32: *Reset Timeout Period (t_{RST}) (C timeout option) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

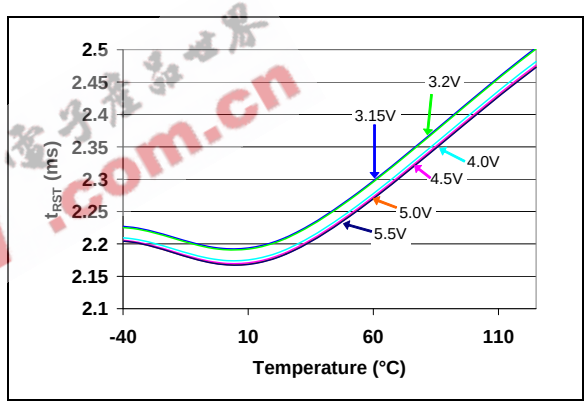

FIGURE 2-35: *Reset Timeout Period (t_{RST}) (B timeout option) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

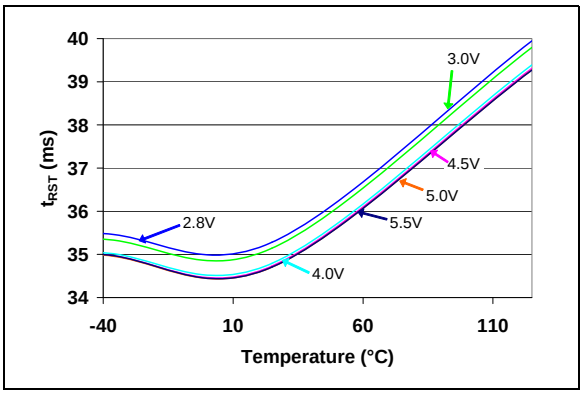

FIGURE 2-33: *Reset Timeout Period (t_{RST}) (C timeout option) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

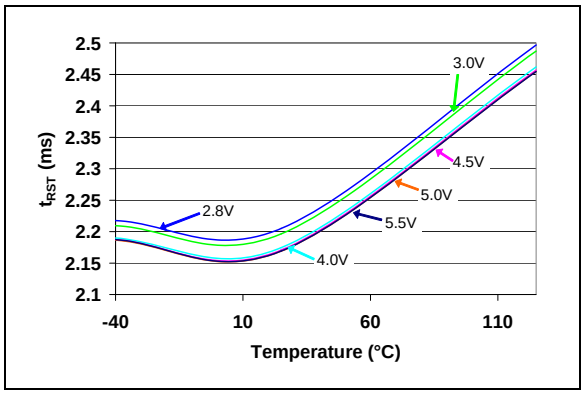

FIGURE 2-36: *Reset Timeout Period (t_{RST}) (B timeout option) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

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Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

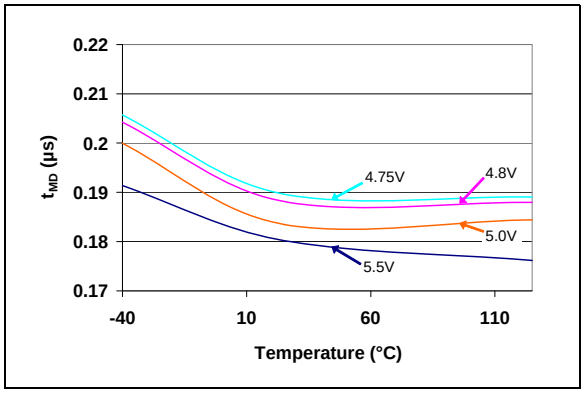

FIGURE 2-37: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min. / 4.63V typ. / 4.75V max.).*

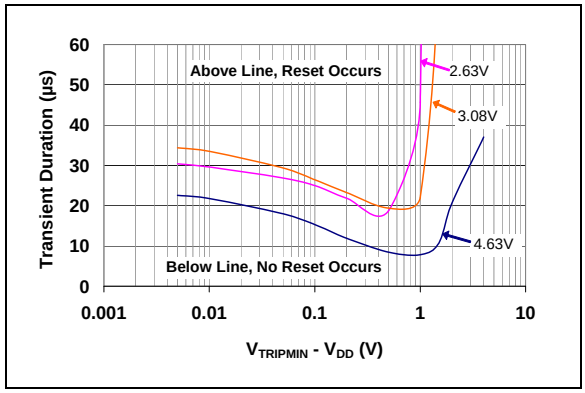

FIGURE 2-40: *V_{DD} Transient Duration vs. Reset Threshold Overdrive (V_{TRIP} (minimum) - V_{DD}).*

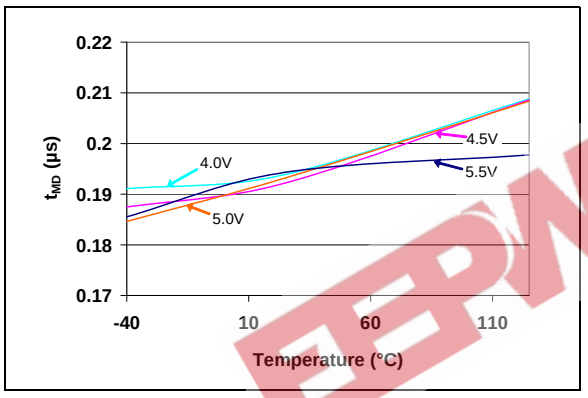

FIGURE 2-38: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min. / 3.08V typ. / 3.15V max.).*

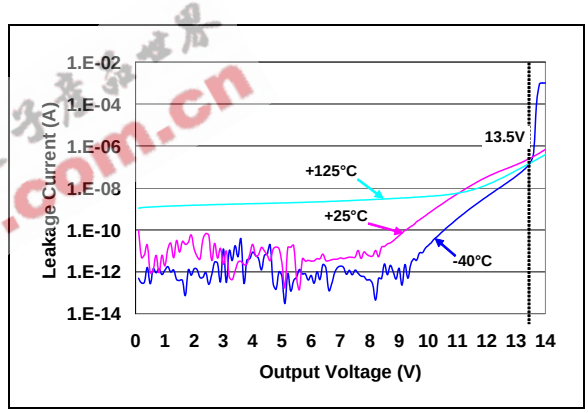

FIGURE 2-41: *Open-Drain Leakage Current vs. Voltage Applied to $\overline{RST}$ Pin (TC1270AR, TC1270ANR, TC1271AR - 2.55V minimum).*

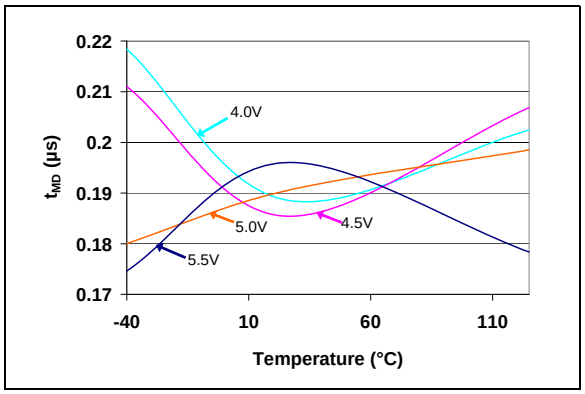

FIGURE 2-39: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min. / 2.63V typ. / 2.70V max.).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PINOUT DESCRIPTION

Pin Number					Sym	Pin		Standard Function
TC1270A (Push-Pull, active low)		TC1270AN (Open-Drain, active low)	TC1271A (Push-Pull, active high)					
SOT-23-5	SOT-143-4	SOT-23-5	SOT-23-5	SOT-143-4		Type	Buffer / Driver	
5	1		5	1	V_{SS}	—	Power	Ground
4	2	—	—	—	$\overline{RST}$	O	Push-Pull	Reset output (Push Pull), active low H = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Timer Delay completes) L = V_{DD} < V_{TRIP}, Reset pin is active Goes active (Low) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.
—	—	4	—	—	$\overline{RST}$	O	Open-Drain	Reset output (Open-Drain), active low Float = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Timer Delay completes) L = V_{DD} < V_{TRIP}, Reset pin is active Goes active (Low) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.
—	—	—	4	2	RST	O	Push-Pull	Reset output (Push Pull), active high H = V_{DD} < V_{TRIP}, Reset pin is active L = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Timer Delay completes) Goes active (High) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.

Note 1: The $\overline{MR}$ pin has an internal weak pull-up (18.5 kΩ typical).

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TABLE 3-1: PINOUT DESCRIPTION (CONTINUED)

Pin Number					Sym	Pin		Standard Function
TC1270A (Push-Pull, active low)		TC1270AN (Open-Drain, active low)	TC1271A (Push-Pull, active high)					
SOT-23-5	SOT-143-4	SOT-23-5	SOT-23-5	SOT-143-4		Type	Buffer / Driver	
3	3	—	3	3	$\overline{MR}$	I	ST (1)	Manual Reset input pin This input allows a push button switch to be directly connected to the TC1270A/70AN/71A's $\overline{MR}$ pin, which can then be used to force a system Reset. The input filter (ignores) noise pulses that occur on the $\overline{MR}$ pin. H = Switch is open (internal pull-up resistor pulls signal high). State of the RST/$\overline{RST}$ pin determined by other system conditions. L = Switch is depressed (shorted to ground). This forces the RST/$\overline{RST}$ pin Active.
2	4	—	2	4	V_{DD}	—	Power	Supply Voltage
1	—	—	1	—	NC	—		No Connection

Note 1: The $\overline{MR}$ pin has an internal weak pull-up (18.5 kΩ typical).

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3.1 Ground Terminal (V_{SS})

V_{SS} provides the negative reference for the analog input voltage. Typically, the circuit ground is used.

3.2 Supply Voltage (V_{DD})

V_{DD} can be used for power supply monitoring or a voltage level that requires monitoring.

3.3 Reset Output (RST and $\overline{RST}$)

There are three types of Reset output pins. These are:

1. Push-Pull active-low Reset
2. Push-Pull active-high Reset
3. Open-Drain active-low Reset, External pull-up resistor required.

3.3.1 ACTIVE-LOW ($\overline{RST}$) - PUSH-PULL

The $\overline{RST}$ push-pull output remains low while V_{DD} is below the reset voltage threshold (V_{TRIP}). The time that the $\overline{RST}$ pin is held low after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) is typically 280 ms. After the Reset delay timer expires, the $\overline{RST}$ pin will be driven to the high state.

3.3.2 ACTIVE-HIGH (RST) - PUSH-PULL

The RST push-pull output remains high while V_{DD} is below the reset voltage threshold (V_{TRIP}). The time that the RST pin is held high after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) is typically 280 ms. After the Reset delay timer expires, the RST pin will be driven to the low state.

3.3.3 ACTIVE-LOW ($\overline{RST}$) - OPEN-DRAIN

The $\overline{RST}$ open-drain output remains low while V_{DD} is below the reset voltage threshold (V_{TRIP}). The time that the $\overline{RST}$ pin is held low after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) depends on the Reset Timeout selected. After the Reset Delay Timer expires, the $\overline{RST}$ pin will float.

3.4 Manual Reset Input ($\overline{MR}$)

The Manual Reset ($\overline{MR}$) input pin allows a push button switch to easily be connected to the system. When the push button is depressed, it forces a system Reset. This pin has circuitry that filters noise that may be present on the $\overline{MR}$ signal.

The $\overline{MR}$ pin is active-low and has an internal pull-up resistor.

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4.0 DEVICE OPERATION

4.1 General Description

For many of today's microcontroller applications, care must be taken to prevent low-power conditions that can cause many different system problems. The most common causes are brown-out conditions, where the system supply drops below the operating level momentarily. The second most common cause is when a slowly decaying power supply causes the microcontroller to begin executing instructions without sufficient voltage to sustain volatile memory (RAM), thus producing indeterminate results.

The TC127XA family (TC1270A, TC1270AN, and TC1271A) are cost-effective voltage supervisor devices designed to keep a microcontroller in Reset until the system voltage has reached and stabilized at the proper level for reliable system operation. These devices also operate as protection from brown-out conditions when the system supply voltage drops below a safe operating level.

A Manual Reset input ($\overline{MR}$ pin) is provided. This allows a push button switch to be directly connected to the TC127XA device, and is suitable for use as a push button Reset. This allows the system to easily be reset from the external control of the push button switch. No external components are required.

The Reset pin (RST or $\overline{RST}$) will be forced active, if any of the following occur:

- During device power up
- V_{DD} goes below the device threshold voltage
- The Manual Reset input ($\overline{MR}$) goes low

Figure 4-1 shows a high level block diagram of the devices. The device can be described with three functional blocks. These are:

- Voltage Detect circuit
- Manual Reset with Glitch Filter circuit
- Reset Generator circuit

The Reset Generator circuit controls the reset delay time of the reset output signal.

There are three Reset Delay time options. Depending on the option, the reset signal ($\overline{RST}$/RST pin) will be held active for a minimum of 1.09 ms, 17.5 ms, or 140 ms.

The TC1271A has an active-high RST output while the TC1270A and TC1270AN have an active-low $\overline{RST}$ output.

The TC1270A and TC1271A have a push-pull output driver, while the TC1270AN has an open-drain output.

Figure 4-2 shows a typical circuit for a push-pull device and Figure 4-3 shows a typical circuit for an open-drain device.

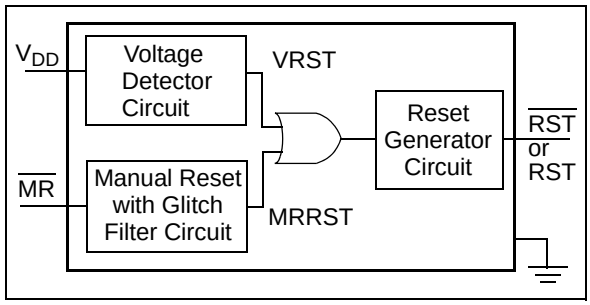

FIGURE 4-1: *TC127XA High Level Block Diagram.*

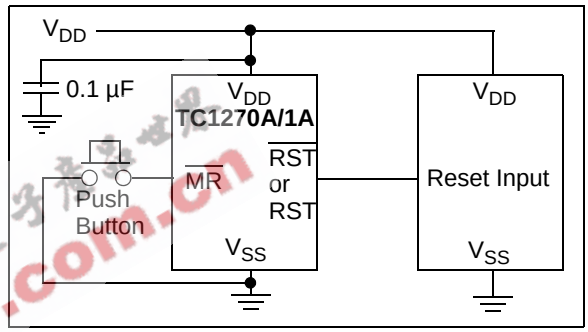

FIGURE 4-2: *Typical Push-Pull Application Circuit.*

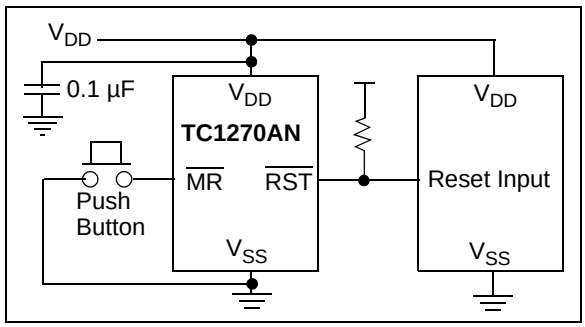

FIGURE 4-3: *Typical Open-Drain Application Circuit.*

The TC1270A and TC1271A devices are available in a 4-Pin SOT-143 package to maintain footprint compatibility with the TC1270, TC1271, TCM811, and TCM812 devices, and the SOT-23-5 package. The TC1270AN is only available in the SOT-23-5 package.

Low supply current makes these devices suitable for battery powered applications.

Device specific block diagrams are shown in Figure 4-4 through Figure 4-6.

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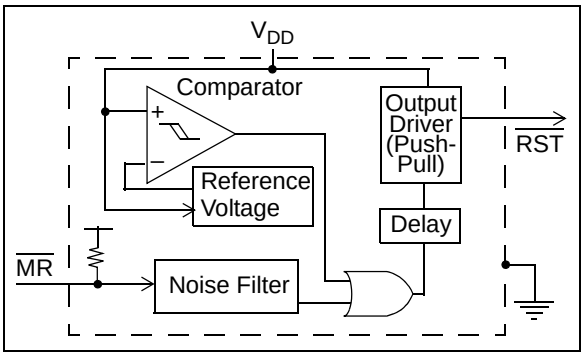

FIGURE 4-4: *TC1270A Block Diagram.*

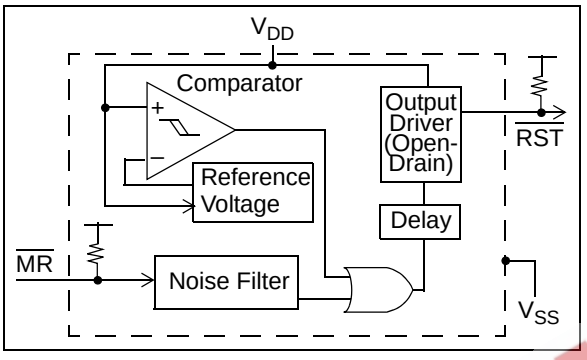

FIGURE 4-5: *TC1270AN Block Diagram.*

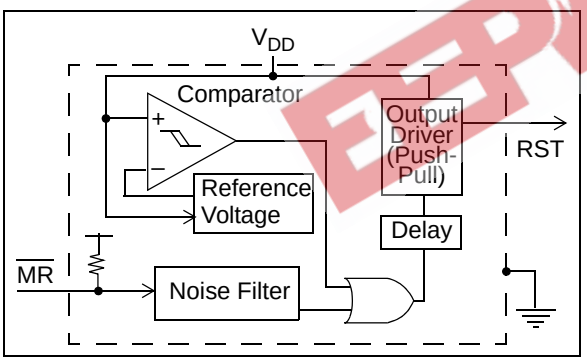

FIGURE 4-6: *TC1271A Block Diagram.*

4.2 Voltage Detect Circuit

The Voltage Detect Circuit monitors V_{DD}. The device's Reset voltage trip point (V_{TRIP}) is selected when the device is ordered. The voltage on the device's V_{DD} pin determines the output state of the $\overline{RST}$/RST pin.

V_{DD} voltages above the $V_{TRIP(MAX)}$ force the $\overline{RST}$/RST pin inactive. V_{DD} voltages below the $V_{TRIP(MIN)}$ force the $\overline{RST}$/RST pin active. The state of the $\overline{RST}$/RST pin is unknown for V_{DD} voltages between $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$. This is shown in Table 4-1

TABLE 4-1: V_{DD} LEVELS TO $\overline{RST}$/RST OUTPUT STATES

V_{DD} Voltage Level	Output State	
	$\overline{RST}$	RST
$V_{DD} \geq V_{TRIP(MAX)}$	H (1, 2)	L (1)
$V_{TRIP(MIN)} < V_{DD} < V_{TRIP(MAX)}$	U	U
$V_{DD} \leq V_{TRIP(MIN)}$	L	H

Legend: H = Driven High L = Driven Low
U = Unknown, driven either High or Low

Note 1: The $\overline{RST}$/RST pin will be driven inactive after the Reset Delay Timer (t_{RST}) times out.

2: The TC1270AN $\overline{RST}$ pin will be floated after the Reset Delay Timer (t_{RST}) times out.

The term V_{TRIP} will be used as the general term for the trip point voltage where the device actually trips.

In the case where V_{DD} is falling (for voltages starting above $V_{TRIP(MAX)}$):

- Voltages above $V_{TRIP(MAX)}$ will never cause the $\overline{RST}$/RST output pin to be driven Active.
- Voltages below $V_{TRIP(MIN)}$ will always cause the $\overline{RST}$/RST output pin to be driven Active.

Now in the case where V_{DD} is rising (for voltages starting below $V_{TRIP(MIN)}$):

- Voltages above $V_{TRIP(MAX)}$ will always cause the $\overline{RST}$/RST output pin to be driven Inactive, (or floated - TC1270AN) after the Reset Delay Timer (t_{RST}), times out.

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Table 4-2 shows the various device trip point options and their $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$ voltages. Also the negative percentage change from common regulated voltages is shown.

In the case where V_{DD} is falling from the regulated voltage, as the V_{DD} crosses the V_{TRIP} voltage the $\overline{RST}$/RST pin is driven active. Now the desired circuitry is in reset, or the circuitry has the indication that the V_{DD} is below the selected V_{TRIP}.

In the case where V_{DD} is rising. As the V_{DD} crosses the V_{TRIP} voltage, the $\overline{RST}$/RST pin is driven inactive after the Reset Delay Timer elapses. Now the desired circuitry is released from reset and will start to operate in its normal mode, or the circuitry has the indication that the V_{DD} is above the selected V_{TRIP}.

TABLE 4-2: SELECTING THE TRIP POINT

Trip Voltage Selection	$V_{TRIP(MAX)}$ (1) / $V_{TRIP(MIN)}$ (2)	- % From Regulated Voltage		
		5.0V	3.3V	3.0V
L	4.75V	5.0%	—	—
	4.50V	10.0%	—	—
M	4.50V	10.0%	—	—
	4.25V	15.0%	—	—
T	3.15V	—	4.5%	—
	3.00V	—	9.2%	—
S	3.00V	—	9.2%	—
	2.85V	—	13.7%	—
R	2.70V	—	—	10.0%
	2.55V	—	—	15.0%

Note 1: Voltage regulator circuit must have tighter tolerance (%) than $V_{TRIP(MAX)}$ % from regulated voltage.

2: Circuitry being reset must have a wider tolerance (%) than $V_{TRIP(MIN)}$ % from regulated voltage.

The TC1270A/TC1270AN/TC1271A devices are optimized to reject fast transient glitches on the V_{DD} line. If the low input signal (which is below V_{TRIP}) is not rejected, the Reset output is driven active within 50 µs of V_{DD} falling through the Reset voltage threshold.

After the device exits the Reset condition, the delay circuitry will hold the $\overline{RST}$/RST pin active until the appropriate Reset delay time (t_{RST}) has elapsed.

During device power up, the input voltage is below the Trip Point voltage. The device must enter the valid operating range for the device to start operation.

4.2.1 HYSTERESIS

There is also a minimal hysteresis (V_{HYS}) on the trip point. This is so that small noise signals on the device voltage (V_{DD}) do not cause the Reset pin ($\overline{RST}$/RST) to "jitter" (change between driving an active and inactive).

The characterization graphs shown in Figures 2-13 through 2-15 shows the device hysteresis as a percentage of the voltage trip point (V_{TRIP}).

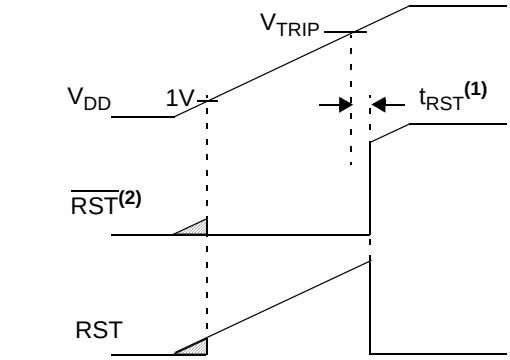
The Reset Delay Timer (t_{RST}) gives a time based hysteresis for the system.

4.2.2 POWER-UP/RISING V_{DD}

As the device V_{DD} rises, the device's Reset circuit will remain active until the voltage rises above the "actual" trip point (V_{TRIP}).

Figure 4-7 shows a power-up sequence and the waveform of the $\overline{RST}$ and RST pins. As the device powers up, the voltage will start below the valid operating voltage of the device. At this voltage, the $\overline{RST}$/RST output is not valid. Once the voltage is above the minimum operating voltage (1V) and below the selected V_{TRIP}, the Reset output will be active.

Once the device voltage rises above the V_{TRIP} voltage, the Reset delay timer (t_{RST}) starts. When the Reset delay timer times out, the Reset output ($\overline{RST}$/RST) is driven inactive.



Note 1: Additional system current is consumed during the t_{RST} time.

2: The TC1270AN requires an external pull-up resistor.

FIGURE 4-7: *$\overline{RST}$/RST pin Operation Power-up.*

4.2.3 POWER-DOWN/BROWN-OUTS

As the device powers-down/brown-outs, the V_{DD} falls from a voltage above the devices trip point (V_{TRIP}). The device will trip at a voltage between the maximum trip point ($V_{TRIP(MAX)}$) and the minimum trip point ($V_{TRIP(MIN)}$). Once the device voltage (V_{DD}) goes below this voltage, the $\overline{RST}$/RST pin will be forced to the active state.

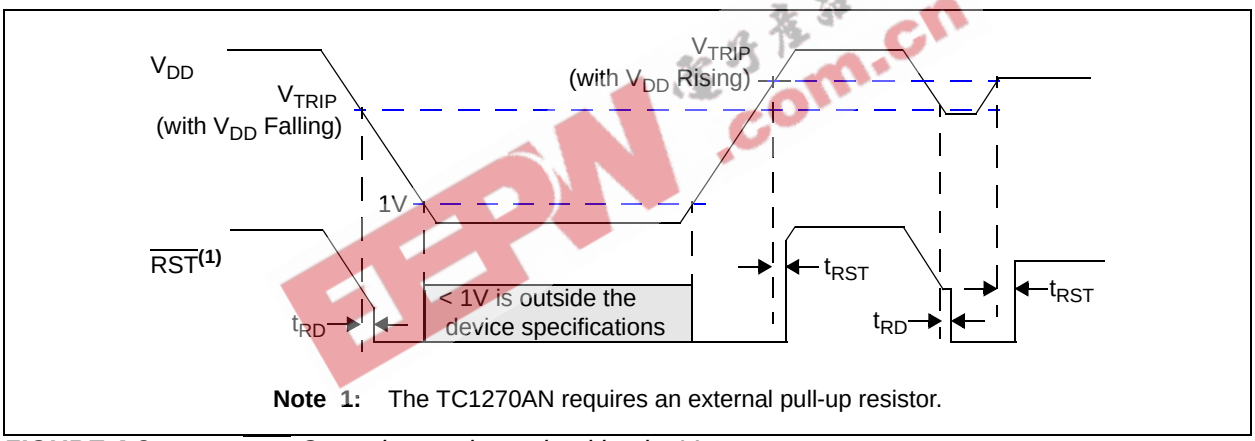
Figure 4-8 shows the waveform of the $\overline{RST}$ pin as determined by the V_{DD} voltage. As the V_{DD} voltage falls from the normal operating point, the device "enters" reset by crossing the V_{TRIP} voltage (between $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$). Then when V_{DD} voltage rises, the device "exits" reset by crossing the V_{TRIP} voltage (below or at $V_{TRIP(MAX)}$). After the "exit" state has been detected, the Reset Delay Timer (t_{RST}) starts. Once the t_{RST} time completes, the Reset pin is driven inactive.

Table 4-3 shows the state of the $\overline{RST}$ or RST pins.

TABLE 4-3: RESET PIN STATES

Device	State of $\overline{RST}$ Pin when:		State of RST Pin when:		Output Driver
	$V_{DD} < V_{TRIP}$	$V_{DD} > V_{TRIP}$ (1)	$V_{DD} < V_{TRIP}$	$V_{DD} > V_{TRIP}$ (1)	
TC1270A	L	H	—	—	Push-Pull
TC1271A	—	—	H	L	Push-Pull

Note 1: The $\overline{RST}$/RST pin will be driven inactive after the Reset Delay Timer (t_{RST}) times out.



Note 1: The TC1270AN requires an external pull-up resistor.

FIGURE 4-8: *$\overline{RST}$ Operation as determined by the V_{TRIP}*

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4.3 Negative Going V_{DD} Transients

The minimum pulse width (time) required to cause a Reset may be an important criteria in the implementation of a Power-on Reset (POR) circuit. This time is referred to as transient duration. The TC127XA devices are designed to reject a level of negative-going transients (glitches) on the power supply line.

Transient duration is the amount of time needed for these supervisory devices to respond to a drop in V_{DD}. The transient duration time (t_{TRAN}) is dependent on the magnitude of $V_{TRIP} - V_{DD}$ (overdrive). Any combination of duration and overdrive that lies under the duration/overdrive curve will not generate a Reset signal. Generally speaking, the transient duration time decreases with an increase in the $V_{TRIP} - V_{DD}$ voltage.

Figure 4-9 shows an example transient duration vs. Reset comparator overdrive. It shows that the farther below the trip point the transient pulse goes, the duration of the pulse required to cause a Reset gets shorter. So any combination of duration and overdrive that lays **under** the curve will **not** generate a Reset signal. Combinations **above** the curve are detected as a brown-out or power-down.

Transient immunity can be improved by adding a bypass capacitor (typically 0.1 µF) as close as possible to the V_{DD} pin of the TC127XA device.

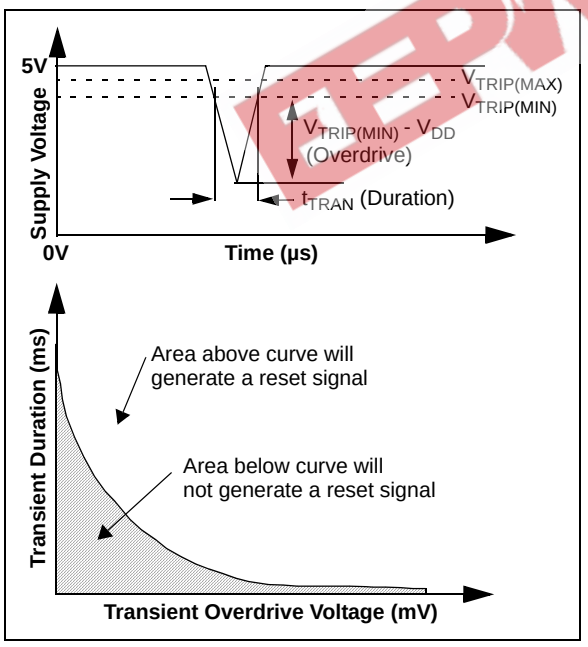

FIGURE 4-9: *Example of Typical Transient Duration Waveform.*

4.4 Manual Reset with Glitch Filter Circuit

The Manual Reset input pin ($\overline{MR}$) allows the Reset pins ($\overline{RST}$/RST) to be manually forced to their active states. The $\overline{MR}$ pin has circuitry to filter noise pulses that may be present on the pin. Figure 4-10 shows a block diagram for using the TC127XA with a push button switch. To minimize the required external components, the $\overline{MR}$ input has an internal pull-up resistor.

A mechanical push button or active logic signal can drive the $\overline{MR}$ input.

Once $\overline{MR}$ has been low for a time, t_{MD} (the Manual Reset delay time), the Reset output pins are forced active. The Reset output pins will remain in their active states for the Reset delay timer time out period (t_{RST}).

Figure 4-11 shows a waveform for the Manual Reset switch input and the Reset pins output.

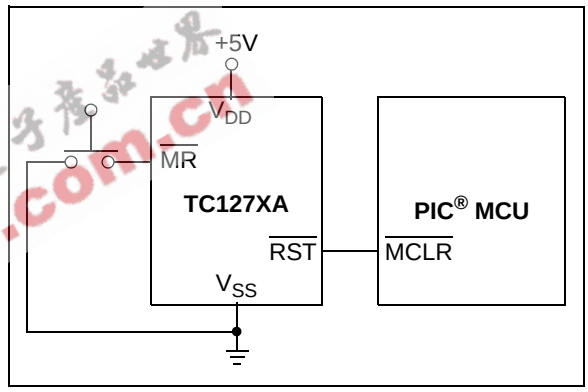

FIGURE 4-10: *Push Button Reset.*

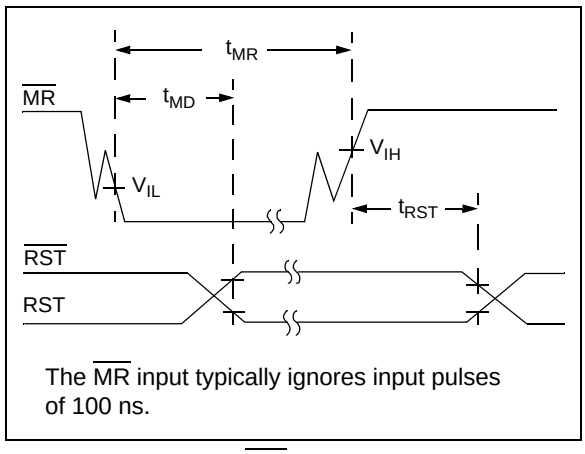

FIGURE 4-11: *$\overline{MR}$ Input – Push Button.*

4.4.1 NOISE FILTER

The noise filter filters out noise spikes (glitches) on the Manual Reset pin ($\overline{MR}$). Noise spikes less than 100 ns (typical) are filtered.

4.5 Reset Generator Circuit

The output signals from the Voltage Detect Circuit and the Manual Reset with Glitch Filter Circuit are OR'd together and is used to activate the Reset Generator Module.

After the reset conditions have been removed (the $\overline{MR}$ pin is no longer forced low and the input voltage is greater than the Trip Point voltage), the Reset Generator circuit determines the reset delay timeout required.

There are three options for the delay circuit. These are:

- 2.19 ms (typical) delay
- 35 ms (typical) delay
- 280 ms (typical) delay

4.5.1 RESET DELAY TIMER

The Reset delay timer ensures that the TC127XA device will "hold" the embedded system in Reset until the system voltage has stabilized. The Reset delay timer time out is shown in Table 4-4.

The Reset Delay Timer starts once the Voltage Detector Circuit output AND the Manual Reset with Glitch Filter Circuit output become inactive. While the Reset Delay Timer is active, the $\overline{RST}$ or RST pin is driven to the active state. Once the Reset Delay Timer times-out, the $\overline{RST}$ or RST pin is driven inactive.

The Reset delay timer (t_{RST}) starts after the device voltage rises above the "actual" trip point (V_{TRIP}). When the Reset delay timer times out, the Reset output pin (RST/$\overline{RST}$) is driven inactive.

The Reset Delay Timer is cleared, if either (or both) the Voltage Detector Circuit output OR the Manual Reset with Glitch Filter Circuit output become active. The $\overline{RST}$ or RST pin continues to be driven to the active state.

Figure 4-12 illustrates when the Reset Delay Timer (t_{RST}) is active or inactive.

4.5.2 EFFECT OF TEMPERATURE ON RESET POWER-UP TIMER (t_{RPU})

The Reset delay timer time out period (t_{RST}) determines how long the device remains in the Reset condition. This time out is affected by both the device V_{DD} and temperature. Typical responses for different V_{DD} values and temperatures are shown in Figures 2-28, 2-29 and 2-30.

TABLE 4-4: RESET DELAY TIMER TIME OUTS

t_{RST}			Units
Min	Typ	Max	
1.09	2.19	4.38	ms
17.5	35	70	ms
140	280	560	ms
↑ This is the minimum time that the Reset Delay Timer will "hold" the Reset pin active after V_{DD} rises above V_{TRIP}		↑ This is the maximum time that the Reset Delay Timer will "hold" the Reset pin active after V_{DD} rises above V_{TRIP}	

Note 1: Shaded rows are custom ordered time outs.

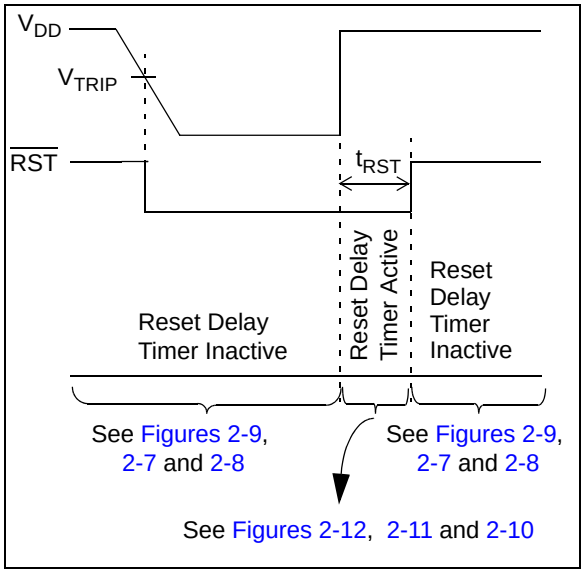

FIGURE 4-12: *Reset Power-up Timer Waveform.*

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5.0 APPLICATION INFORMATION

This section shows application related information that may be useful for your particular design requirements.

5.1 Supply Monitor Noise Sensitivity

The TC127XA devices are optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays) may require a 0.01 µF or 0.1 µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC127XA as possible to keep the capacitor lead length short.

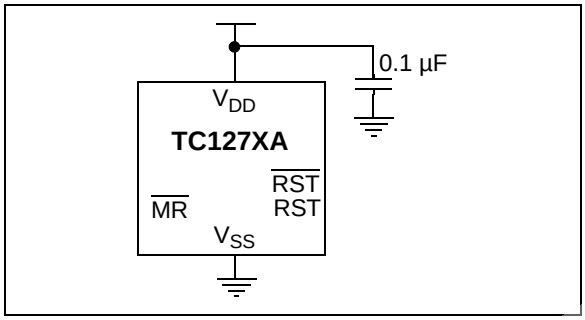

FIGURE 5-1: *Typical Application Circuit with Bypass Capacitor.*

5.2 Conventional Voltage Monitoring

Figure 5-2 and Figure 5-3 show the TC127XA in conventional voltage monitoring applications.

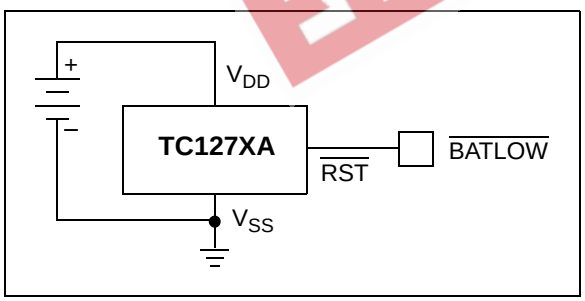

FIGURE 5-2: *Battery Voltage Monitor.*

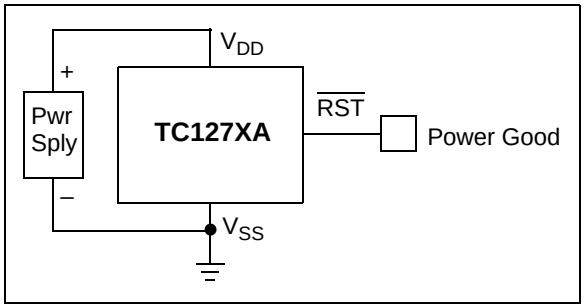

FIGURE 5-3: *Power Good Monitor.*

5.3 Using in PIC® Microcontroller, ICSP™ Applications

Note: This operation can only be done using the device with the Open-Drain $\overline{RST}$ pin (TC1270AN).

Figure 5-4 shows the typical application circuit for using the TC1270AN for voltage supervisory function when the PIC microcontroller will be programmed via the In-Circuit Serial Programming™ (ICSP™) feature. Additional information is available in TB087, *"Using Voltage Supervisors with PICmicro® Microcontroller Systems which Implement In-Circuit Serial Programming™"*, DS91087.

Note: It is recommended that the current into the $\overline{RST}$ pin be current limited by a 1 kΩ resistor.

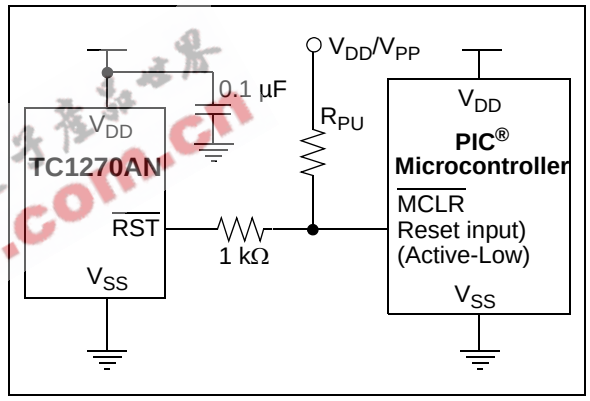

FIGURE 5-4: *Typical Application Circuit for PIC® Microcontroller with the ICSP™ Feature.*

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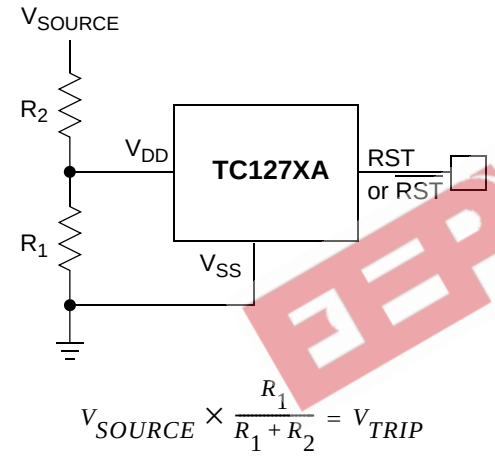
5.4 Modifying The Trip Point, V_{TRIP}

Although the TC127XA device has a fixed voltage trip point (V_{TRIP}), it is sometimes necessary to make custom adjustments. This can be accomplished by connecting an external resistor divider to the TC127XA V_{DD} pin. This causes the V_{SOURCE} voltage to be at a higher voltage than when the TC127XA input equals it's V_{TRIP} voltage (Figure 5-5).

To maintain detector accuracy, the bleeder current through the divider should be significantly higher than the 15 µA maximum operating current required by the TC127XA. A reasonable value for this bleeder current is 1 mA (67 times the 10 µA required by the TC127XA). For example, if V_{TRIP} = 2V and the desired trip point is 2.5V, the value of $R_1 + R_2$ is 2.5 kΩ (2.5V/1 mA). The value of $R_1 + R_2$ can be rounded to the nearest standard value and plugged into the equation of Figure 5-5 to calculate values for R_1 and R_2. 1% tolerance resistors are recommended.



$$V_{SOURCE} \times \frac{R_1}{R_1 + R_2} = V_{TRIP}$$

Where:

V_{SOURCE} = Voltage to be monitored

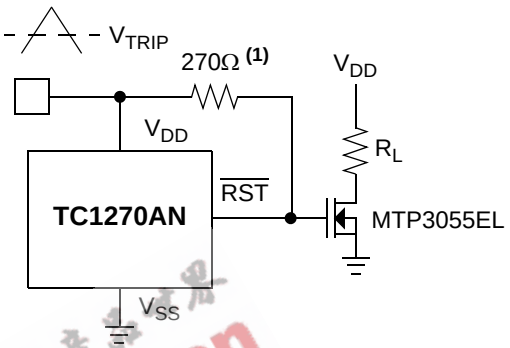
V_{TRIP} = Threshold Voltage setting

Note: In this example, V_{SOURCE} must be greater than (V_{TRIP}).

FIGURE 5-5: *Modify Trip-Point using External Resistor Divider.*

5.5 MOSFET Low-Drive Protection

Low operating power and small physical size make the TC1270AN series ideal for many voltage detector applications. Figure 5-6 shows a low-voltage gate drive protection circuit that prevents overheating of the logic-level MOSFET due to insufficient gate voltage. When the input signal is below the threshold of the TC1270AN, its output grounds the gate of the MOSFET.



Note 1: This resistance needs to be properly sized for the selected Trip point voltage related to the V_{OL} operation.

FIGURE 5-6: *MOSFET Low-Drive Protection.*

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5.6 Controllers and Processors With Bidirectional I/O Pins

Some microcontrollers have bidirectional Reset pins. Depending on the current drive capability of the controller pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a 4.7 kΩ resistor in series with the output of the TC127XA (Figure 5-7). If there are other components in the system that require a Reset signal, they should be buffered so as not to load the Reset line. If the other components are required to follow the Reset I/O of the microcontroller, the buffer should be connected as shown with the solid line.

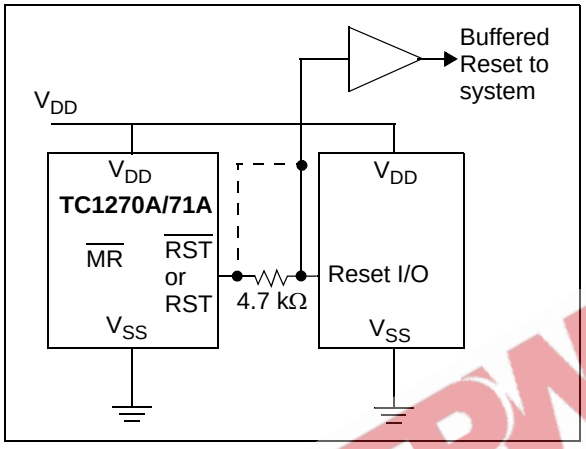

FIGURE 5-7: *Interfacing the TC1270A or TC1271A Push-Pull Output to a Bidirectional Reset I/O pin.*

5.7 Migration Paths

Figure 5-8 shows the 5-pin SOT-23 footprint of the TC1270A, TC1270AN and TC1271A devices. Devices that are in the 3-pin SOT-23 package could be used in that circuit with the loss of the Manual Reset functionality. Examples of compatible footprint devices in the SOT-23-3 package are the MCP111, MCP112, TC54, and TC51 devices. This allows the system to be designed to offer a "base" functionality and a higher end system with the "enhanced" functionality, which includes a manual reset.

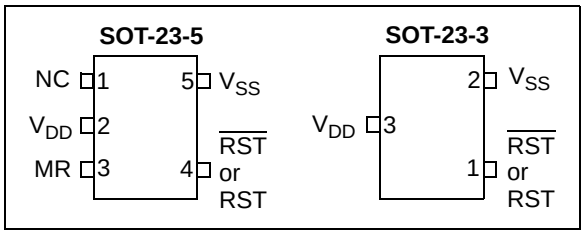

FIGURE 5-8: *SOT-23 5-pin to 3-pin Comparison.*

5.8 Reset Signal Integrity During Power-Down

The TC1270A and TC1271A reset output is valid down to V_{DD} = 1.0V. Below this voltage the output becomes an "open circuit" and does not sink current. This means CMOS logic inputs to the Microcontroller will be floating at an undetermined voltage. Most digital systems are completely shut down well above this voltage. However, in situations where the Reset signal must be maintained valid to V_{DD} = 0V, external circuitry is required.

For devices where the Reset signal is active-low, a pull-down resistor must be connected from the TC1270A $\overline{RST}$ pin to ground to discharge stray capacitances and hold the output low (Figure 5-9).

Similarly for devices where the Reset signal is active-high, a pull-up resistor to V_{DD} is required to ensure a valid high RST signal for V_{DD} below 1.0V (Figure 5-10).

This resistor value, though not critical, should be chosen such that it does not appreciably load the Reset pin under normal operation (100 kΩ will be suitable for most applications).

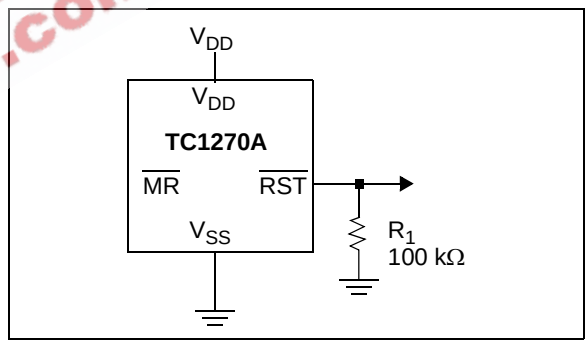

FIGURE 5-9: *Ensuring a valid active-low Reset pin output state as V_{DD} approaches 0V.*

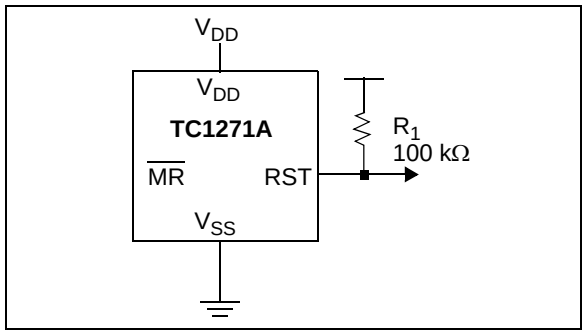

FIGURE 5-10: *Ensuring a valid active-high Reset pin output state as V_{DD} approaches 0V.*

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6.0 STANDARD DEVICES

Table 6-1 shows the standard devices and their order number that are available and their respective configuration.

The configuration includes the:

- Voltage Trip Point (V_{TRIP})
- Reset Time Out (t_{RST})

TABLE 6-1: STANDARD VERSIONS

Device	Reset Threshold (V)				Reset Time Out (ms)				Package	Order Number	Replaces
	Minimum	Typical	Maximum	Code	Minimum	Typical	Maximum	Code (1)			
TC1270A	4.50	4.63	4.75	L	140	280	560	“blank”	SOT-23-5	TC1270ALVCTTR	—
									SOT-143	TC1270ALVRCTR	TC1270LERC / TCM811LERC
TC1270A	4.25	4.38	4.50	M	140	280	560	“blank”	SOT-23-5	TC1270AMVCTTR	—
									SOT-143	TC1270AMVRCTR	TC1270MERC / TCM811MERC
TC1270A	3.00	3.08	3.15	T	140	280	560	“blank”	SOT-23-5	TC1270ATVCTTR	—
									SOT-143	TC1270ATVRCTR	TC1270TERC / TCM811TERC
TC1270A	2.85	2.93	3.00	S	140	280	560	“blank”	SOT-23-5	TC1270ASVCTTR	—
									SOT-143	TC1270ASVRCTR	TC1270SERC / TCM811SERC
TC1270A	2.55	2.63	2.70	R	140	280	560	“blank”	SOT-23-5	TC1270ARVCTTR	—
									SOT-143	TC1270ARVRCTR	TC1270RERC / TCM811RERC
TC1270AN	4.50	4.63	4.75	L	140	280	560	“blank”	SOT-23-5	TC1270ANLVCT	—
TC1270AN	4.25	4.38	4.50	M	140	280	560	“blank”	SOT-23-5	TC1270ANMVCT	—
TC1270AN	3.00	3.08	3.15	T	140	280	560	“blank”	SOT-23-5	TC1270ANTVCT	—
TC1270AN	2.85	2.93	3.00	S	140	280	560	“blank”	SOT-23-5	TC1270ANSVCT	—
TC1270AN	2.55	2.63	2.70	R	140	280	560	“blank”	SOT-23-5	TC1270ANRVCT	—
TC1271A	4.50	4.63	4.75	L	140	280	560	“blank”	SOT-23-5	TC1271ALVCTTR	—
									SOT-143	TC1271ALVRCTR	TC1271LERC / TCM812LERC
TC1271A	4.25	4.38	4.50	M	140	280	560	“blank”	SOT-23-5	TC1271AMVCTTR	—
									SOT-143	TC1271AMVRCTR	TC1271MERC / TCM812MERC
TC1271A	3.00	3.08	3.15	T	140	280	560	“blank”	SOT-23-5	TC1271ATVCTTR	—
									SOT-143	TC1271ATVRCTR	TC1271TERC / TCM812TERC
TC1271A	2.85	2.93	3.00	S	140	280	560	“blank”	SOT-23-5	TC1271ASVCTTR	—
									SOT-143	TC1271ASVRCTR	TC1271SERC / TCM812SERC
TC1271A	2.55	2.63	2.70	R	140	280	560	“blank”	SOT-23-5	TC1271ARVCTTR	—
									SOT-143	TC1271ARVRCTR	TC1271RERC / TCM812RERC

Note 1: “A” timeout delay options are only standard in the SOT-23-5 package. SOT-143 package is a custom request.

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7.0 CUSTOM CONFIGURATIONS

The following Custom Reset Trip Point is available (see Table 7-1).

TABLE 7-1: CUSTOM TRIP POINT

Trip Voltage Selection	$V_{TRIP(MAX)}$ / $V_{TRIP(MIN)}$	- % From Regulated Voltage
		3.0V
(1)	2.85V	5.0%
	2.70V	10.0%

Note 1: Contact factory for additional information.

Table 7-2 shows the codes that specify the desired Reset time out (t_{RST}) for custom devices

TABLE 7-2: DELAY TIME OUT ORDERING CODES

Code	Reset Delay Time (Typ) (ms)	Comment
B	2.19	**Note 1**
C	35	**Note 1**
“blank”	280	Delay timings for standard device offerings

Note 1: This delay timing option is not the standard offering. For information on ordering devices with these delay times, contact your local Microchip sales office. Minimum purchase volumes are required.

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8.0 DEVELOPMENT TOOLS

8.1 Evaluation/Demonstration Boards

The SOT-23-5/6 Evaluation Board (VSUPEV2) can be used to evaluate the characteristics of the TC127XA devices.

This blank PCB has footprints for:

- Pull-up Resistor
- Pull-down Resistor
- Loading Capacitor
- In-line Resistor

There is also a power supply filtering capacitor.

For evaluating the TC127XA devices, the selected device should be installed into the Option A footprint.

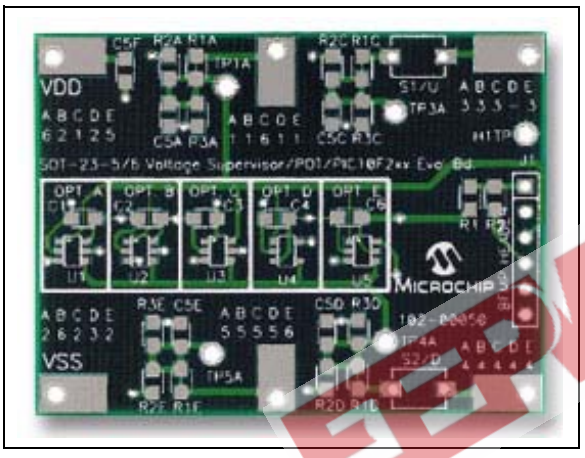

FIGURE 8-1: *SOT-23-5/6 Voltage Supervisor Evaluation Board (VSUPEV2).*

The SOIC14-EV (102-00094) board has a SOT-23-6 footprint, that can be jumpered into any portion of the circuit. This will allow any footprint that the TC1270A requires in the SOT-23-5 package.

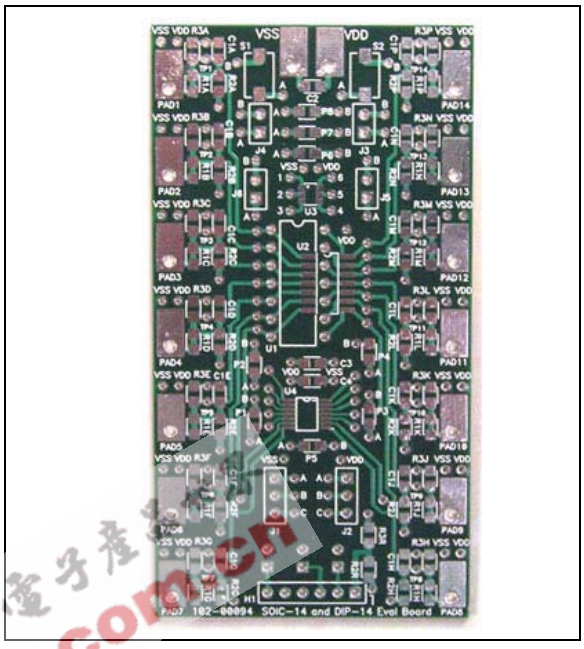

FIGURE 8-2: *SOIC-14 Evaluation Board (SOIC14EV).*

These boards may be purchased directly from the Microchip web site at www.microchip.com.

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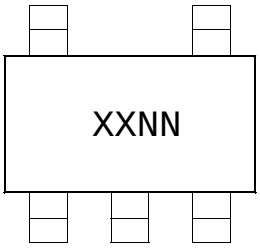
9.0 PACKAGING INFORMATION

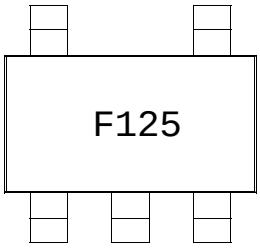
9.1 Package Marking Information

5-Pin SOT-23

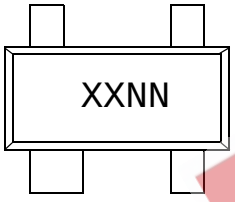


Part Number	Code	Part Number	Code
TC1270ALVCTTR	F1NN	TC1271ALVCTTR	J1NN
TC1270AMVCTTR	F2NN	TC1271AMVCTTR	J2NN
TC1270ATVCTTR	F3NN	TC1271ATVCTTR	J3NN
TC1270ASVCTTR	F4NN	TC1271ASVCTTR	J4NN
TC1270ARVCTTR	F5NN	TC1271ARVCTTR	J5NN
TC1270ANLVCTTR	FSNN		
TC1270ANMVCTTR	FTNN		
TC1270ANTVCTTR	FUNN		
TC1270ANSVCTTR	FVNN		
TC1270ANRVCTTR	FWNN		

Example:

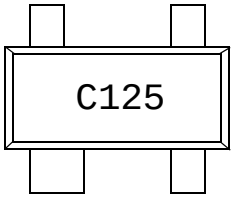


4-Lead SOT-143



Part Number	Code	Part Number	Code
TC1270ALVRCTR	D1NN	TC1271ALVRCTR	C1NN
TC1270AMVRCTR	D2NN	TC1271AMVRCTR	C2NN
TC1270ATVRCTR	D3NN	TC1271ATVRCTR	C3NN
TC1270ASVRCTR	D4NN	TC1271ASVRCTR	C4NN
TC1270ARVRCTR	D5NN	TC1271ARVRCTR	C5NN
TC1270ANLVRCTR	E1NN		
TC1270ANMVRCTR	E2NN		
TC1270ANTVRCTR	E3NN		
TC1270ANSVRCTR	E4NN		
TC1270ANRVRCTR	E5NN		

Example:

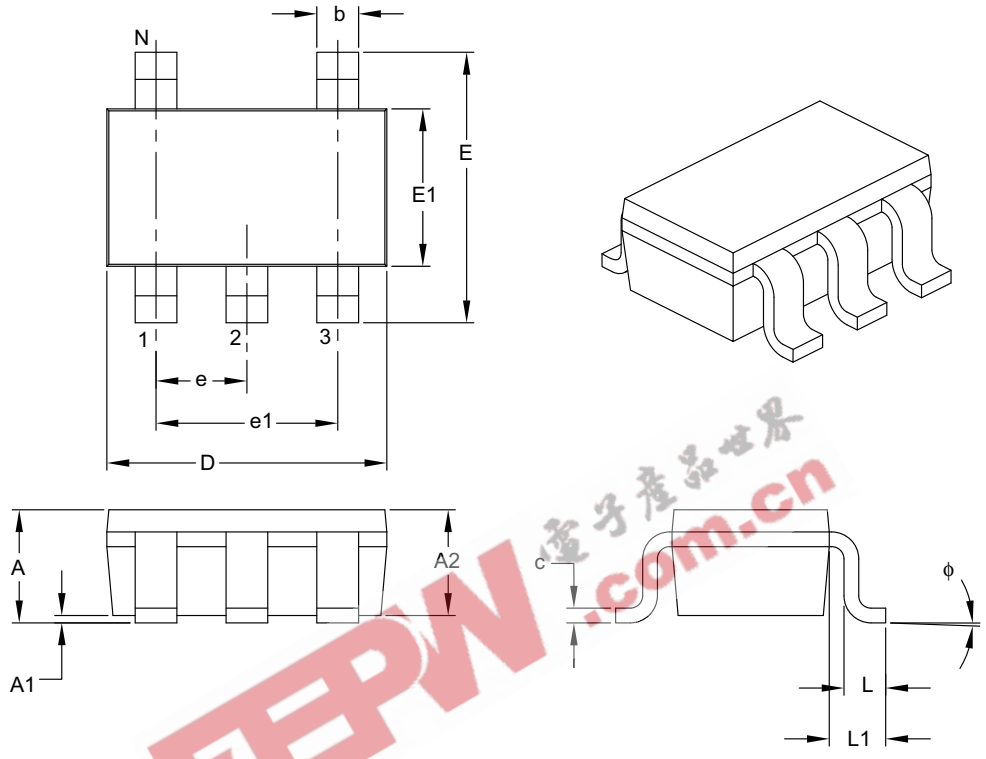


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (CT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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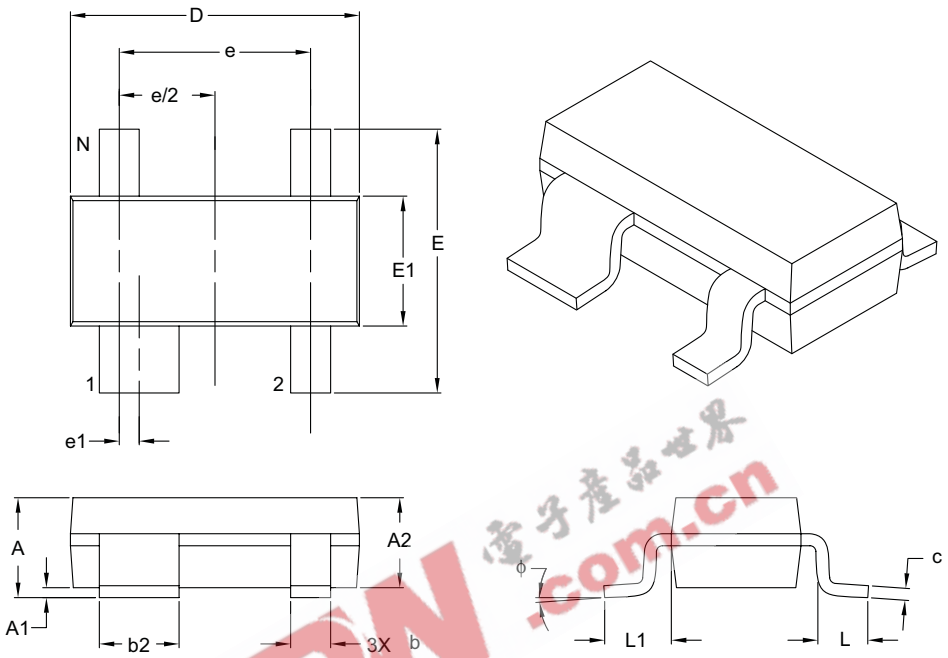
4-Lead Plastic Small Outline Transistor (RC) [SOT-143]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		4	
Pitch	e		1.92 BSC	
Lead 1 Offset	e1		0.20 BSC	
Overall Height	A	0.80	–	1.22
Molded Package Thickness	A2	0.75	0.90	1.07
Standoff §	A1	0.01	–	0.15
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.20	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Footprint	L1		0.54 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.20
Lead 1 Width	b1	0.76	–	0.94
Leads 2, 3 & 4 Width	b	0.30	–	0.54

Notes:

1. § Significant Characteristic.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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9.2 Product Tape and Reel Specifications

FIGURE 9-1: EMBOSSED CARRIER DIMENSIONS (8 MM TAPE ONLY)

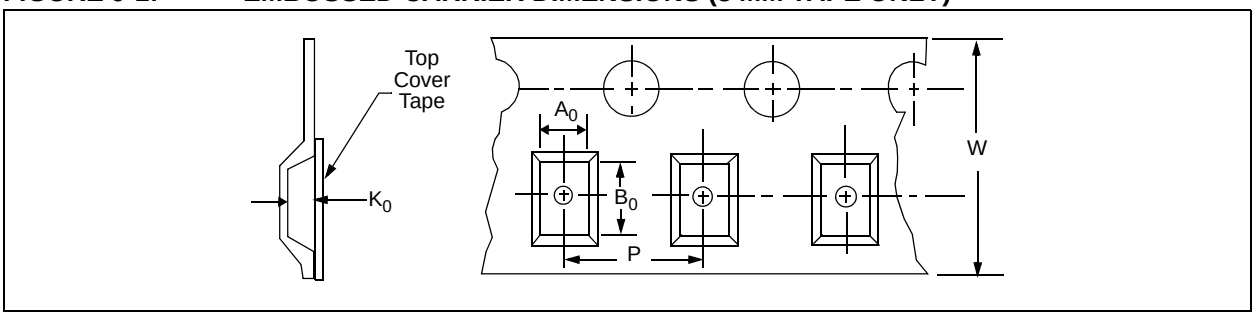

TABLE 1: CARRIER TAPE/CAVITY DIMENSIONS

Case Outline	Package Type		Carrier Dimensions		Cavity Dimensions			Output Quantity Units	Reel Diameter in mm
			W mm	P mm	A0 mm	B0 mm	K0 mm		
OT	SOT-23	5L	8	4	3.2	3.2	1.4	3000	180
RC	SOT-143	4L	8	4	3.1	2.69	1.3	3000	180

FIGURE 9-2: 5-LEAD SOT-23 DEVICE TAPE AND REEL SPECIFICATIONS

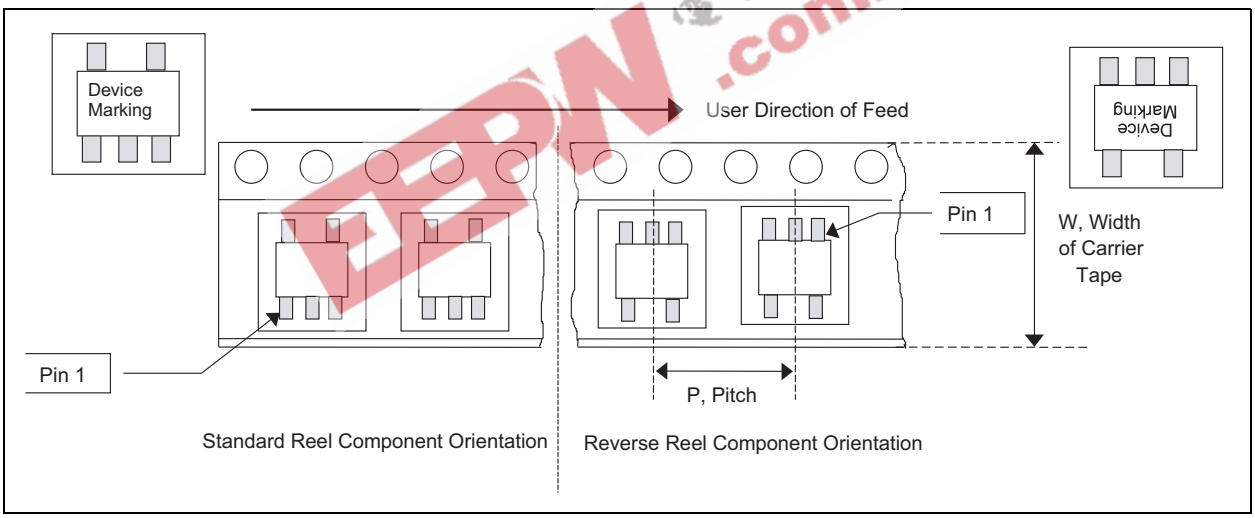

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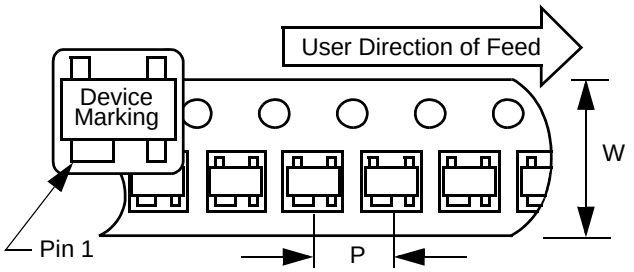
FIGURE 9-3: 4-LEAD SOT-143 DEVICE TAPE AND REEL SPECIFICATIONS

Component Taping Orientation for 4-Pin SOT-143 Devices



Standard Reel Component Orientation
for TR Suffix Device
(Mark Right Side Up)

Carrier Tape, Number of Components Per Reel and Reel Size:

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
4-Pin SOT-143	8 mm	4 mm	3000	7 in.

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APPENDIX A: REVISION HISTORY

Revision B (June 2007)

- Added new options:
  - Open-Drain output
  - New Reset Delay timeouts.
- Updated Package Outline Drawings
- Updated Revision History
- Added new options to Product Identification System

Revision A (March 2007)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	XX	X
Device	V_{TRIP} Options	Reset Delay Options	Temperature Range	Package	Tape/Reel Option

Device:	TC1270A:	Voltage Supervisor with Manual Reset
	TC1270AN:	Voltage Supervisor with Manual Reset
	TC1271A:	Voltage Supervisor with Manual Reset
V_{TRIP} Options:	R =	2.55V (min.) / 2.63V (typ.) / 2.70V (max.)
	S =	2.85V (min.) / 2.93V (typ.) / 3.00V (max.)
	T =	3.00V (min.) / 3.08V (typ.) / 3.15V (max.)
	M =	4.25V (min.) / 4.38V (typ.) / 4.50V (max.)
	L =	4.50V (min.) / 4.63V (typ.) / 4.75V (max.)
Time Out Options:	B =	t_{RST} = 2.19 ms (typ)
	C =	t_{RST} = 35 ms (typ)
	"blank" =	t_{RST} = 280 ms (typ)
Temperature Range:	V =	-40°C to +125°C
Package:	CT =	Plastic Small Outline Transistor, SOT-23, 5-lead
	RC =	Plastic Small Outline Transistor, SOT-143, 4-lead
Tape/Reel Option:	TR =	Tape and Reel

Examples:

a) TC1270ASVCTTR:
2.85V min. / 2.93V typ. / 3.00V max. voltage trip point,
Push-pull active low reset,
Reset Delay Timer = 280 ms,
5-LD SOT-23, Tape and Reel,
-40°C to +125°C

b) TC1270ALVRCTR:
4.50V min. / 4.63V typ. / 4.75V max. voltage trip point,
Push-pull active low reset,
Reset Delay Timer = 280 ms,
4-LD SOT-143, Tape and Reel,
-40°C to +125°C

c) TC1270ANMBVCTTR:
4.25V min. / 4.38V typ. / 4.50V max.
Open-drain active low reset,
Reset Delay Timer = 2.19 ms,
5-Lead SOT-23, Tape and Reel,
-40°C to +125°C

d) TC1270ANLCVCT:
4.50V min. / 4.63V typ. / 4.75V max.
Open-drain active low reset,
Reset Delay Timer = 35 ms,
5-Lead SOT-23,
-40°C to +125°C

e) TC1271ARVCTTR:
2.55V min. / 2.63V typ. / 2.70V max. voltage trip point,
Push-pull active high reset,
Reset Delay Timer = 280 ms,
5-LD SOT-23, Tape and Reel,
-40°C to +125°C

f) TC1271ATVRCTR:
3.00V min. / 3.08V typ. / 3.15V max. voltage trip point,
Push-pull active high reset,
Reset Delay Timer = 280 ms,
4-LD SOT-143, Tape and Reel,
-40°C to +125°C

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