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## TC3000 Turbo Product Code decoders

Introducing turbo product codes with BCH "t=2" codes  
Customisable bitrate : 7 to 25 Mbits/s

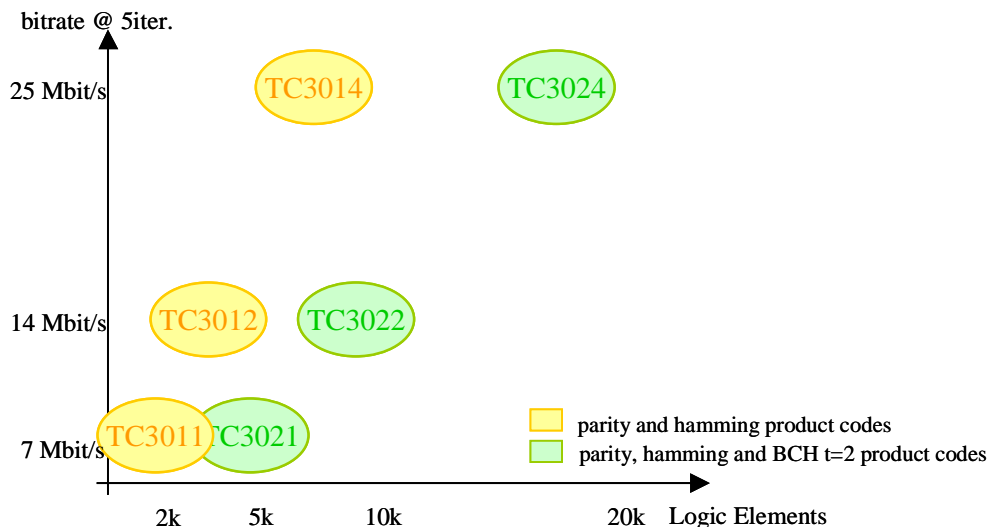
Turbo codes improves a transmission link by an additional gain of 2 to 3 decibels, compared to classical FEC solutions.

TC3000 is a family of IP Cores offering powerful and flexible turbo product codes. TC3000 is the first IP Core implementing Hamming and double-error-correcting BCH product codes. A highly generic approach allows TC3000 to be precisely optimised for a target application.

### Features

- Very High FEC performance : **Hamming and "BCH-t=2"** codes
- Bitrate customisable : **7 to 25 Mbits/s** typical @ 5 iterations
- Large block sizes : **up to 65 kbits**
- On-the-fly change of the code
- Shortening facilities to adjust packet size and coding rate
- Single-chip PLD IP Core : Altera APEX, no external memory required
- Latency reduction by bank-swapping
- Two selectable configuration interface

### Bitrate/Complexity trade-off



## Flexibility

TC3000 family offers 3 levels of flexibility :

<b>TC3000 family member</b>	<ul style="list-style-type: none"> <li>✓ BCH t=2 code support (YES/NO)</li> <li>✓ Choice on bitrate</li> </ul>
<b>VHDL generic parameters</b> <i>before synthesis</i>	<ul style="list-style-type: none"> <li>✓ Maximum row code length</li> <li>✓ Maximum column code length</li> <li>✓ Input Quantization width</li> <li>✓ 1 or 2 input buffers</li> </ul>
<b>On-the fly parameters</b> <i>from block to block</i>	<ul style="list-style-type: none"> <li>✓ Row code</li> <li>✓ Column code</li> <li>✓ Shortening values</li> <li>✓ Max. number of iterations</li> <li>✓ Stopping feature enabled</li> </ul>

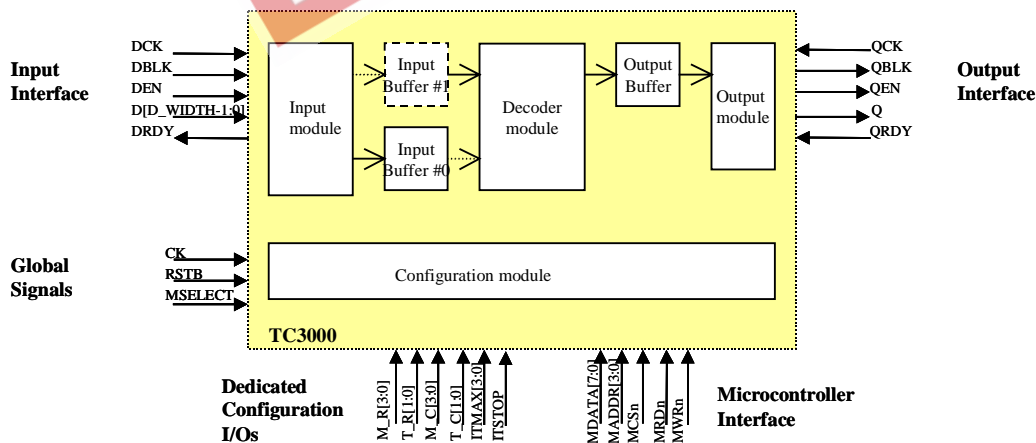
## FEC performance

Very high FEC performance are obtained for various block sizes and coding rates. The FEC behaviour of the “BCH t=2” codes makes them particularly attractive for quasi-error free applications.

⇒ Gaussian channel and QPSK modulation. Results given with 5 iterations.

Product Code	Rate	Eb/N0 @BER=10 <sup>-5</sup>	Eb/N0 @BER=10 <sup>-8</sup>
(32,26) x (32,26)	0.660	2.9 dB	3.6 dB
(32,21) x (32,21)	0.431	2.4 dB	N.A.
(64,57) x (64,57)	0.793	3.2 dB	3.6 dB
(64,51) x (64,51)	0.635	2.6 dB	2.9 dB
(128,120) x (128,120)	0.879	3.8 dB	4.2 dB
(128,113) x (128,113)	0.779	3.3 dB	3.4 dB
(256,247) x (256,247)	0.931	4.5 dB	4.8 dB
(256,239) x (256,239)	0.872	4.0 dB	N.A.

## Block Diagram



## Implementation results

Product	Codes supported		Generic parameter setting				Implementation results				
	Hamming	BCH t=2	Row max. length	Column max. length	Data width	bank swap	LE	ESB	APEX20K device	Fmax MHz	Typical Bitrate @ (64,57) <sup>2</sup> , 5 iterations
TC3011	✓		64	64	4	NO	2025	22	200 C7	82	8 Mbits/s
TC3014	✓		64	64	4	NO	6926	36	200 C7	72	25 Mbits/s
			128	128	4	NO	8115	88	400 C7	67	23.5 Mbits/s
TC3022	✓	✓	64	64	4	NO	8932	24	400 C7	79	14 Mbits/s