TEMIC

TELEFUNKEN Semiconductors

TEA2029CV

Timing Processor (LINE, FRAME, SMPS) for TV Sets

General Description

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing. Timing signals are obtained from a Voltage-Controlled Oscillator (VCO) operating at 500 kHz by means of a cheap ceramic resonator.

A chain of dividers and appropriate logic functions are producing very accurately defined sampling pulses and the necessary timing signals. This avoids the frequency adjustment normally required with line and frame oscillators.

Features

- 500 kHz VCO and appropriate logic avoids adjustment of timing pulses
- Identical line and Switch Mode Power Supply (SMPS) frequency avoids visible interference on screen
- Multistandard capability by automatic 50/60 Hz identification
- Low power dissipation by controlling a frame thyristor (or class D output transistor stage)
- Video identification circuit
- Super sandcastle

Case: DIP 28

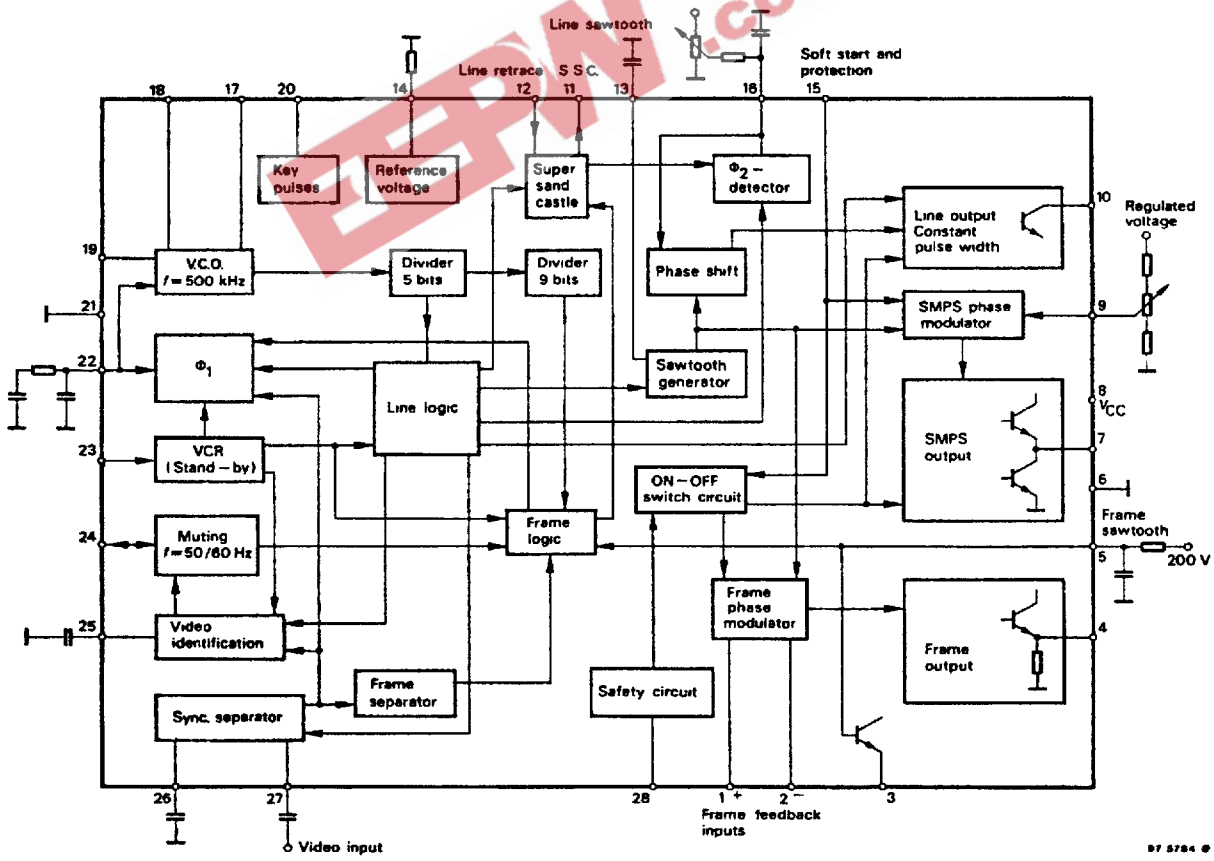

Figure 1. Block diagram

Absolute Maximum Ratings

T_{amb} = 25°C, unless otherwise specified.

Parameters		Symbol	Value	Unit
Supply voltage	Pin 8	V_S	14	V
AGC current	Pin 20	I_{20}	5	mA
Video identification current	Pin 24	I_{24}	10	mA
Line retrace current Line output current	Pin 12 Pin 10	$\pm I_{12}$ $+I_{10}$ $-I_{10}$	10 40 10	mA
Frame sawtooth generator	Pin 3	I_S	20	mA
Frame output current	Pin 4	I_4	100	mA
SMPS output current	Pin 7	$\pm I_7$	50	mA
Safety input current	Pin 28	I_{28}	5	mA
Safety input voltage	Pin 28	V_{28}	V_{CC}	
Ambient temperature range		T_{amb}	0 to +70	°C
Storage temperature range		T_{stg}	-25 to +150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	55	K/W

Electrical Characteristics

$V_S = V_{CC}$ = 12 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	Frame, line and SMPS output without load Pin 8	I_S		60	80	mA
Sync. separator	Pins 26 and 27					
Positive video input signal, ac coupled	Source impedance ≤ 200 Ω Pin 27	V_{27}	0.2	1.8	3	V_{pp}
Negative clamping current during sync. pulse		$-I_{27}$	25	40	55	µA
Clamping current, continuously		I_{27}	3	5	9	µA
Slicing level decoupling 50 % of sync. amplitude	Negative current Pin 26	$-I_{26}$		640	1000	µA
	Positive current	I_{26}	12	25	36	µA
Pulse for keyed AGC	Pin 20					
Output current		I_0			5	mA
Output separation voltage	I_0 = 5 mA	V_0			0.4	V
Delay time from the key pulse leading edge to the middle of the sync. pulse		t_{d1}		3.4		µs
Delay time from the middle of the sync. pulse to the key pulse trailing		t_{d2}		4.8		µs

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Voltage control oscillator, VCO $V_S = V_{CC}$ = 11 V to 13 V	Pin 17, 18, 19 Ceramic resonator type: CSB 503 B					
Operating voltage	Pin 8	V_S	5		13.2	V
Frequency control range after H. divider	Low-end High-end	f_{low} f_{high}		15.3 16.1		kHz
Control current	Pin 22	$\pm I_{22}$			10	µA
Phase detector $\emptyset_1$	Pin 22					
Output current	Low loop gain High loop gain	$\pm I_0$	0.35 1	0.5 1.5	0.65 2	mA
Ratio of charging and discharging current		I_{ch}/I_{dis}		1		
Transfer gain	Low loop gain High loop gain	G_{TL} G_{TH}		1.2 3.6		kHz/µs
Window pulse width (only in low loop gain, video identif. is "ON")		t$\emptyset$1		10		µs
Delay time between middle of key pulse and $\emptyset_1$ comparison edge		t_d		0		µs
VCR and STAND-BY switching input	Pin 23					
Threshold voltage VCR (VCR switch is in ON position below this value)		V_T	1.6	2.1	2.6	V
Threshold voltage STAND-BY (STAND-BY switch is in ON position above this level)		V_T	3.2	4	4.8	V
Input current		$-I_I$	0.030		1	mA
Video identification, see figure 2	Pins 24 and 25					
Input current	Pin 24	I_I			10	mA
Output saturation voltage	I_I = 5 mA, no video signal	V_{Osat}			0.6	V
Output voltage	f = 60 Hz, Pin 24 $I_{i(Video)}$ = 2.5 mA	V_0	5.5	6	7.5	V
Input current	f = 50 Hz Pin 24	I_I			10	µA
Output current, charging the capacitor	Pin 25	I_{ch}	0.5	0.75	1	mA
Ratio between the charging and discharging current	Pin 25	I_{ch}/I_{dis}	1.7		4.0	
Identification sampling time	Pin 25	t_{25}	1.3		2.2	µs
Threshold voltage	Pin 25 lower to higher value (low means no video)	V_T	4	4.5	5	V
Hysteresis voltage	Pin 25	V_{hyst}		350		mV
H. ramp generator, see figure 3	Pin 13					
Saw-tooth amplitude synchronized state	peak to peak	v	3	3.5	4	V
Charge current		I_{ch}	185	200	215	µA
Saw-tooth base voltage		V_{min}			0.5	V
Discharging time		t_{dis}			4	µs
Delay time between $\emptyset_2$ comparing edge and leading edge of discharging pulse		t_d		1.95		µs

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Super sandcastle, SSC	Pin 11					
Output current		I_{11}	-10		+ 10	mA
Output voltage levels; Burst key pulse Horizontal blank pulse	I_{11} = 5 mA	 V_{Burst} V_{HB}	 9 4	 4.5	 5	V
Frame blank pulse	I_{11} = 5mA frame out of function	V_{VB}	2	2.5	3	V
Delay time between middle of sync. pulse (pin 27) and leading edge of burst key pulse		t_d	2.3		3	µs
Duration of burst key pulse			3.7	4	5	µs
Delay time	between SSC cutting level at pin 12 and line blank pulse	t_d			0.5	µs
Frame retrace blanking duration				24		lines
Line retrace input	Pin 12					
First threshold for blanking		V_b	11		12	V
Second threshold for $\emptyset_2$		$V_{\emptyset 2}$	-1	1.3	2.3	V
Input currents:	V_{12} =12 V V_{12} = 5 V V_{12} = 0 V V_{12} = 1 V	I_{12}	 -2	550 200 -50 -1		µA µA µA mA
Operating input voltage		$-V_{12}$			1	V
Phase detector Ø2,	Pin 16					
Charging current		I_{ch}	0.4	0.6	0.8	mA
Ratio of charging and discharging current		I_{ch}/I_{dis}		1		
Delay time between the comparing edges of $\emptyset_1$ and $\emptyset_2$ f_o (VCO) = 500 kHz		t_d	1.5	2	2.8	µs
Input current of internal error amplifier for $\emptyset_2$ phase shift		I_{16}			3	µA
Time difference between $\emptyset_2$ comparing edge and middle of line retrace (without external phase tuning circuit)		Δt		0		µs
Horizontal output (Open collector),	Pin 10					
Output saturation voltage	I_O = 20 mA	V_O			1	V
Output current		I_O			40	mA
Output pulse duration	f_0 = 500 kHz	t_p	24	26	28	µs
$\emptyset_2$ phase range	without external phase shift	$t_\emptyset$	14	16	19	µs
Frame logic						
Free running period video identification = 0		N		315		lines
Search window		N	247		361	lines
50 Hz window		N	309		315	lines
60 Hz window		N	247		277	lines
VCR mode window		N	247		361	lines
Frame saw-tooth generator	Pin 5					

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Saw-tooth amplitude	peak to peak	v	2	3	4	V
60 Hz internal current generator		I_0	12	14	16	µA
Discharge time	C = 0.47 µF, ΔV_C = 4 V	t_{dis}			70	µs
Delay time	between beginning of discharging and leading edge of the first main equalizing pulse which appears during internal sync. pulse	t_d		5		µs
Saw tooth base voltage	I_3 = 0.to 10 mA Pin 3	V_{min}	1	1.26	1.4	V
Frame feed back inputs	Pins 1 and 2					
Input current		$I_{1,2}$			10	µA
Common mode range		CMR	2		10	V
Frame output, see figure 4	Pin 4					
Operating output current		$-I_0$			80	mA
Limit value		$-I_{0M}$			100	mA
Max. "ON" time		t_{on}		40		µs
Output phase range		t_ϕ	0		t_{onmax}	µs
Negative over current	limit value	I_{NO}		10		mA
Output voltage	I_4 = –80 mA	V_O	10			V
Switch mode power supply, SMPS						
Input current	Pin 9	I_I			10	µA
Internal reference voltage		V_{ref}	1.2	1.26	1.35	V
SMPS Output, see figure 5	Pin 7					
Output current limit value		I_0	–50		50	mA
Output voltage	I_0 = –20 mA I_0 = +20 mA	V_0	10		2	V
t_{on} time		t_{onmax}	27	28	29	µs
Position of trailing edge of SMPS pulse			3 µs before middle of H sync. pulse			
Negative over current limit value		I_{NO}			50	mA
Safety input,	Pin 28					
Threshold voltage		V_T	1.15	1.26	1.37	V
Input current	$V_T = V_{ref}$	I_I			3	µA
Input voltage		V_{28max}			V_{CC}	
Soft starting input and SMPS – $T_{"ON"}$ limitation (see figure 6), Pin 15						
Charging current	t = 4 µs	I_{ch}	70		130	µA
Ratio of charging and discharging current		I_{ch} / I_{dis}		1		
Charging time		t_{ch}		4		µs
Ratio of charging and discharging time		t_{ch} / t_{dis}		2		

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Switch-ON, Switch-OFF processing	Pins 4, 7 and 10					
SMPS	frame and line V_{CC} starting	V_S	5.25 + V_{hyst}		6.5 + V_{hyst}	V
	V_{CC} stopping		5.25		6.25	
Hysteresis between switch on- and off level		V_{hyst}		500		mV
Voltage reference	Pin 14	V_{ref}	1.2	1.26	1.35	V

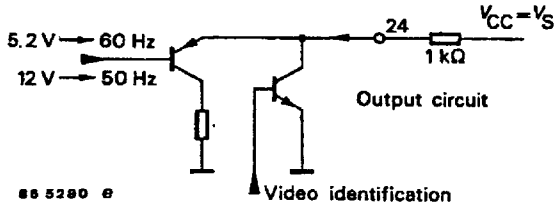

Figure 2.

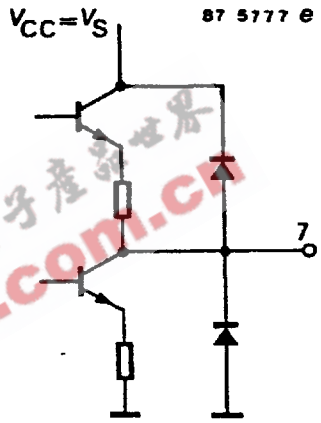

Figure 5.

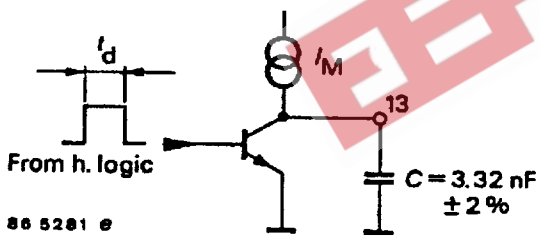

Figure 3.

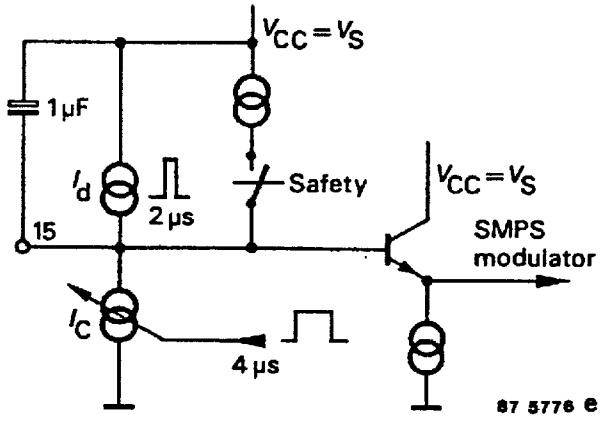

Figure 6.

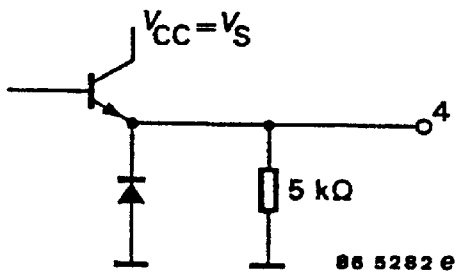

Figure 4.

I_C = charge current (I_{ch})

I_d = discharge current (I_{dis})

t_d = discharge time (t_{dis})

Application

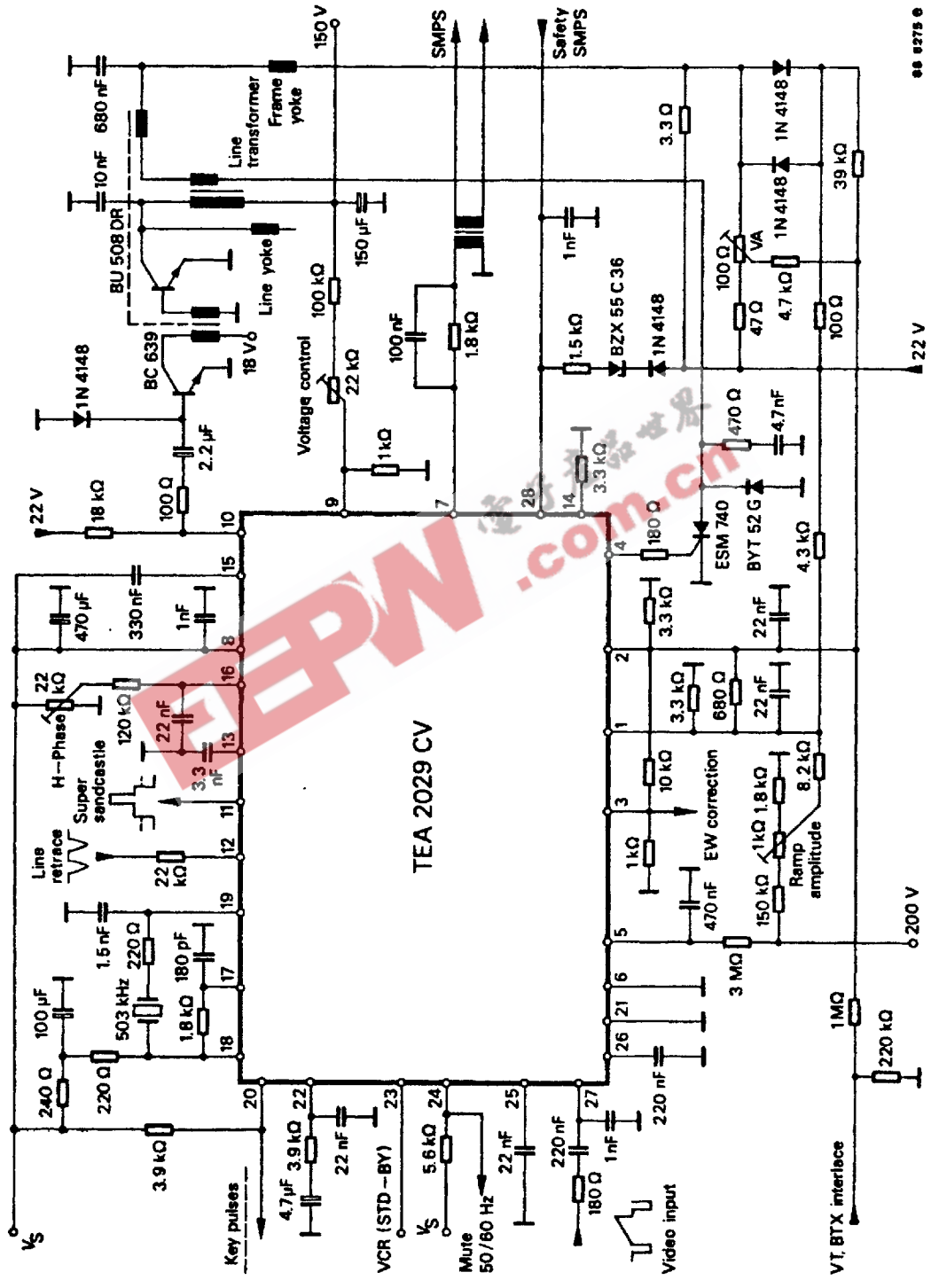

Figure 7.

Dimension in mm

Package: DIP 28