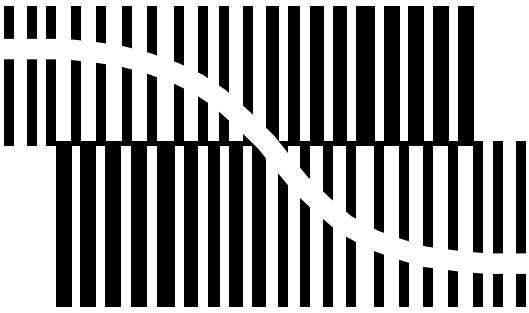
DATA SHEET



BITSTREAM CONVERSION

TDA1307
High-performance bitstream digital filter

Preliminary specification
Supersedes data of July 1993
File under Integrated Circuits, IC01

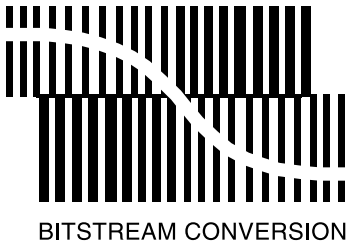
1996 Jan 08

Philips Semiconductors

PHILIPS

High-performance bitstream digital filter TDA1307

FEATURES



- Multiple format inputs: I^2S, Sony 16, 18 and 20-bit
- 8-sample interpolation error concealment
- Digital mute, attenuation –12 dB
- Digital audio output function (biphase-mark encoded) according to IEC 958
- Digital silence detection (output)
- Digital de-emphasis (selectable, FS-programmable)
- 8 × oversampling finite impulse response (FIR) filter
- DC-cancelling filter (selectable)
- Peak detection (continuous) and read-out to microprocessor
- Fade function: sophisticated volume control
- Selectable 3rd/4th order noise shaping
- Selectable dither generation and automatic scaling
- Dedicated TDA1547 1-bit output
- Differential mode bitstream: complementary data outputs available
- Simple 3-line serial microprocessor command interface
- Flexible system clock oscillator circuitry
- Power-on reset
- Standby function
- SDIP42 package.

QUICK REFERENCE DATA

Voltages are referenced to V_{SS} (ground = 0 V); all V_{SS} and all V_{DD} connections should be connected externally to the same supply.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDC1,2,3}$	supply voltage (pins 21, 41 and 8)		4.5	5.0	5.5	V
V_{DDOSC}	supply voltage (pin 24)		4.5	5.0	5.5	V
V_{DDAR}	supply voltage (pin 32)		4.5	5.0	5.5	V
V_{DDAL}	supply voltage (pin 29)		4.5	5.0	5.5	V
$I_{DDC1,2,3}$	supply current (pins 21, 41 and 8)	V_{DD} = 5 V	–	75	–	mA
I_{DDOSC}	supply current (pin 24)	V_{DD} = 5 V	–	2	–	mA
I_{DDAR}	supply current (pin 32)	V_{DD} = 5 V	–	2	–	mA
I_{DDAL}	supply current (pin 29)	V_{DD} = 5 V	–	1	–	mA
f_{XTAL}	oscillator clock frequency		–	33.8688	–	MHz
T_{amb}	operating ambient temperature		–20	–	+70	°C
P_{tot}	total power consumption		–	400	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1307	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

GENERAL DESCRIPTION

The TDA1307 is an advanced oversampling digital filter employing bitstream conversion technology, which has been designed for use in premium performance digital audio applications. Audio data is input to the TDA1307 through its multiple-format interface. Any of the four formats (I^2S, Sony 16, 18 or 20-bit) are acceptable. By using a highly accurate audio data processing structure, including 8 times oversampling digital filtering and up to 4th order noise shaping, a high quality bitstream is produced which, when used in the recommended combination with the TDA1547 bitstream DAC, provides the optimum in dynamic range and signal-to-noise performance. With the TDA1307, a high degree of versatility is achieved by a multitude of functional features and their easy accessibility; error concealment functions, audio peak data information and an advanced patented digital fade function are accessible through a simple microprocessor command interface, which also provides access to various integrated system settings and functions.

TDA1307 plus TDA1547 high-performance bitstream digital filter plus DAC combination:

For many features:

- Highly accessible structure
- Intelligent audio data processing.

For optimum performance:

- 4th order noise shaping
- Improvement dynamic range (113 dB)
- Improvement signal-to-noise (115 dB).

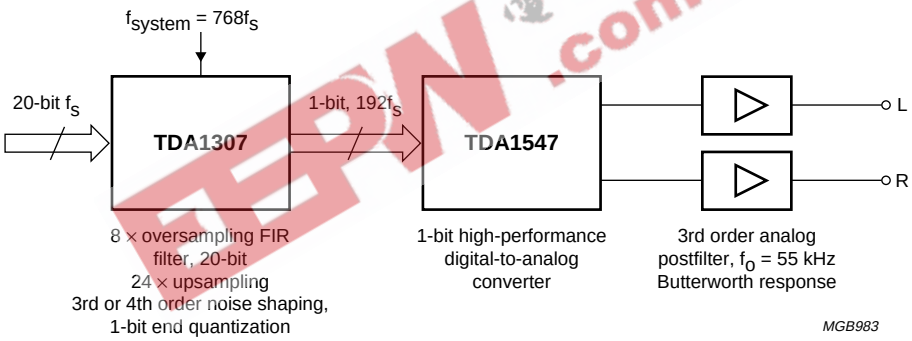


Fig.1 High performance bitstream reconstruction system.

BLOCK DIAGRAM

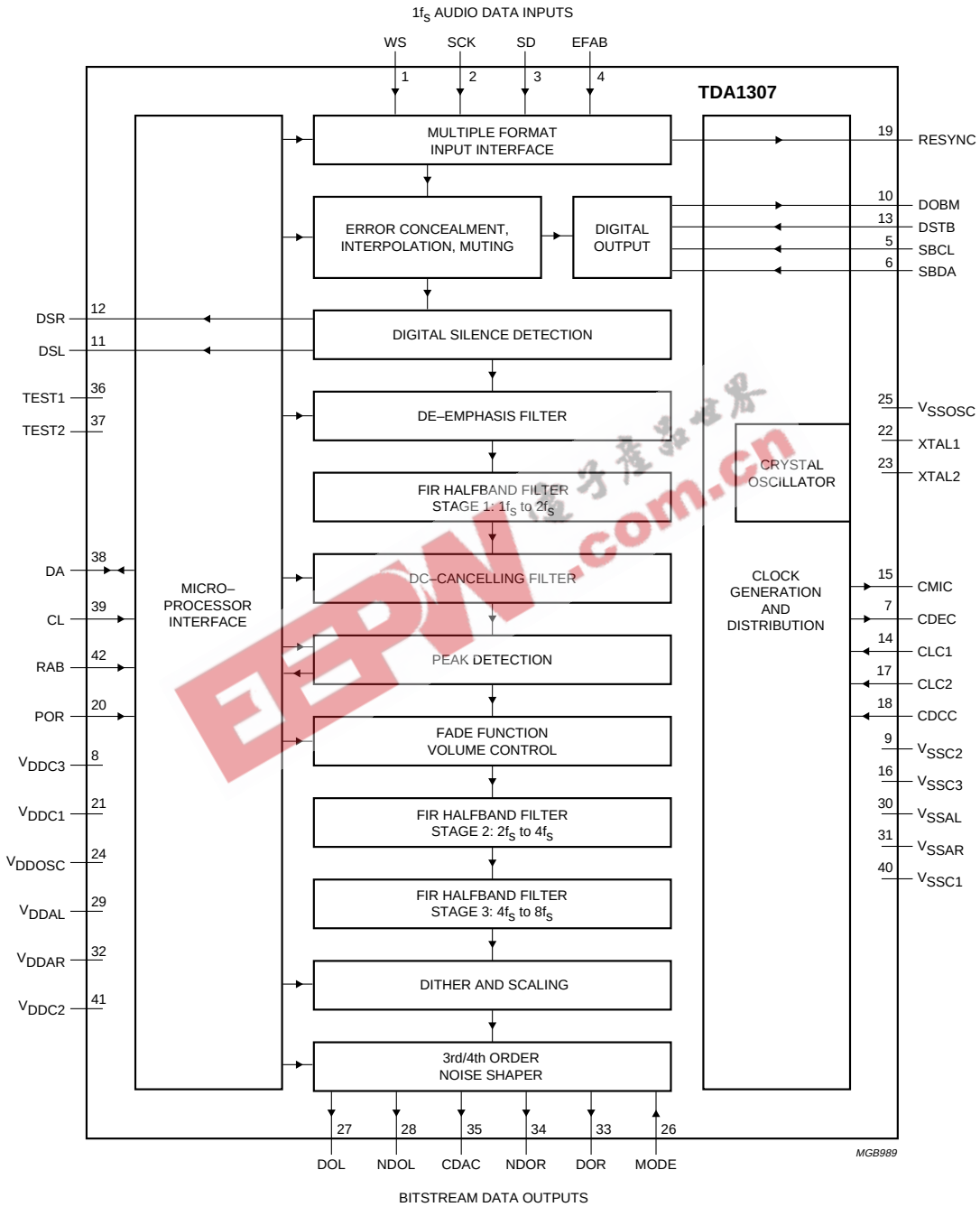


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
WS	1	I	word select input to data interface
SCK	2	I	clock input to data interface
SD	3	I	data input to interface
EFAB	4	I(1)	error flag (active HIGH): input from decoder chip indicating unreliable data
SBCL	5	I	subcode clock: a 10-bit burst clock (typ. 2.8224 MHz) input which synchronizes the subcode data
SBDA	6	I	subcode data: a 10-bit burst of data, including flags and sync bits, serially input once per frame, clocked by burst clock input SBCL
CDEC	7	O	decoder clock output: frequency division programmable by means of pins 14 (CLC1) and 17 (CLC2) to output 192, 256, 384 or 768 times f_s
V_{DDC3}	8		positive supply 3
V_{SSC2}	9		ground 2
DOBM	10	O	digital audio output: this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data; transmission is in biphase-mark code
DSL	11	O	digital silence detected (active LOW) on left channel
DSR	12	O	digital silence detected (active LOW) on right channel
DSTB	13	I(2)	DOBM standby mode enforce pin (active HIGH)
CLC1	14	I	application mode programming pin for CDEC (pin 7) frequency division
CMIC	15	O	clock output, provided to be used as running clock by microprocessor (in master mode only), output $96f_s$
V_{SSC3}	16		ground 3
CLC2	17	I	application mode programming pin for CDEC (pin 7) frequency division
CDCC	18	I	master / slave mode selection pin
RESYNC	19	O	resynchronization: out-of-lock indication from data input section (active HIGH)
POR	20	I(2)	power-on reset (active LOW)
V_{DDC1}	21		supply voltage 1
XTAL1	22	I	crystal oscillator terminal: local crystal oscillator sense forced input in slave mode
XTAL2	23	O	crystal oscillator output: drive output to crystal
V_{DDOSC}	24		positive supply connection to crystal oscillator circuitry
V_{SSOSC}	25		ground connection to crystal oscillator circuitry
MODE	26	I(2)	evaluation mode programming pin (active LOW); in normal operation, this pin should be left open-circuit or connected to the positive supply
DOL	27	O	data output left channel to bitstream DAC TDA1547
NDOL	28	O	complementary data output left channel to TDA1547 in double differential mode
V_{DDAL}	29		positive supply connection to output data driving circuitry, left channel
V_{SSAL}	30		ground connection to output data driving circuitry, left channel
V_{SSAR}	31		ground connection to output data driving circuitry, right channel
V_{DDAR}	32		positive supply connection to output data driving circuitry, right channel
DOR	33	O	data output right channel to TDA1547

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
NDOR	34	O	complementary data output right channel to TDA1547 in double differential mode
CDAC	35	O	clock output to bitstream DAC TDA1547
TEST1	36	I(1)	test mode input; in normal operation this pin should be connected to ground
TEST2	37	I(1)	test mode input; in normal operation this pin should be connected to ground
DA	38	I/O(2)	bidirectional data line intended for control data from the microprocessor and peak data from the TDA1307
CL	39	I(2)	clock input, to be generated by the microprocessor
V_{SSC1}	40		ground 1
V_{DDC2}	41		supply voltage 2
RAB	42	I(2)	command / peak data request line

Notes

1. These pins are configured as internal pull-down.
2. These pins are configured as internal pull-up.

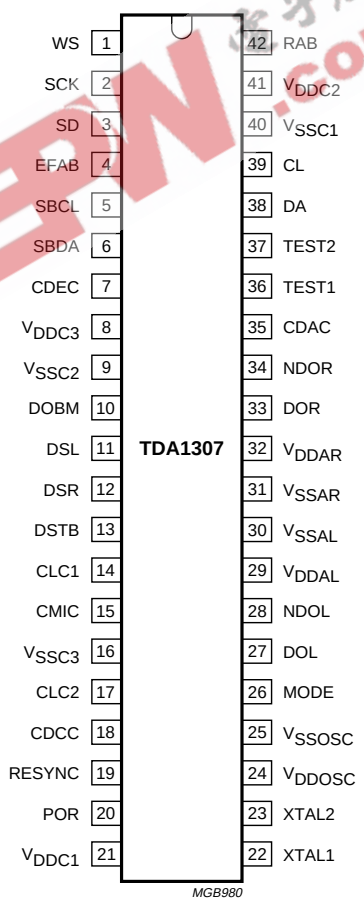


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

In the block diagram, Fig.1, a general subdivision into three main functional sections is illustrated. The actual signal processing takes place in the central sequence of blocks, a representation of the audio data path from top to bottom. The two blocks named “Microprocessor Interface” and “Clock Generation and Distribution” fulfil a general auxiliary function to the audio data processing path. The Microprocessor Interface provides access to all the blocks in the audio path that require or allow for configuration or selection, and manipulates data read-out from the Peak Detection block, all via a simple three-line interface. The Clock Generation and Distribution section, driven either by its integrated oscillator circuit with external crystal or by an externally provided master clock, provides the data processing blocks with timebases, manages the system mode dependent frequency settings, and conveniently generates clocks for external use by the system decoder IC and microprocessor. Following are detailed explanations of the functions of each block in the audio data processing path and their setting options manipulated by the microprocessor interface, the use of the microprocessor interface, and the functions of the clock section with its various system settings.

Clock generation and distribution

The clock generation section of the TDA1307 is designed to accommodate two main modes. The master mode, in which the TDA1307 is the master in the digital audio system, and for which the clock is generated by connecting a crystal of $768f_s$ (33.8688 MHz) to the crystal oscillator pins XTAL1 (pin 22) and XTAL2 (pin 23); and the slave mode, in which the TDA1307 is supplied a clock by the IC in the system that acts as the master (e.g. the digital audio interface receiver). In this event a clock signal frequency of $256f_s$ is input to pin XTAL1. Master or slave mode is programmed by means of pin CDCC (pin 18) logic 1 for master and logic 0 for slave mode. The circuit diagram of Fig.4 shows the typical connection of the external oscillator circuitry and crystal resonator for master mode operation. Note that the positive supply V_{DDOSC} is the reference to the oscillator circuitry. The LC network is used for suppression of the fundamental frequency component of the overtone crystal. Figure 5 shows how to connect for slave mode operation. A clock frequency of typical $256f_s$ and levels of 0 V/+5 V is input to XTAL1 via AC coupling. The 100 kΩ resistor and the 10 nF capacitor are required to provide the necessary biasing for XTAL2 by filtering and feeding back the output signal of XTAL1.

Besides generating all necessary internal clocks for the audio data processing blocks and the clock to the DAC, the clock generation block further provides two clocks for external use when operating in master mode. Pin CDEC (pin 7) is used as the running clock for the system decoder IC, and pin CMIC (pin 15) is used as the running clock for the system microprocessor. CMIC outputs, by a fixed divider ratio to XTAL2, a clock signal at $96f_s$. For CDEC the divider ratio is programmable by means of pins CLC1 (pin 14) and CLC2 (pin 17). Table 1 gives the clock divider programming relationships.

Table 1 Clock divider programming

CLC1	CLC2	CDEC OUTPUT FREQUENCY
0	0	$256f_s$
0	1	$384f_s$
1	0	$768f_s$
1	1	$192f_s$

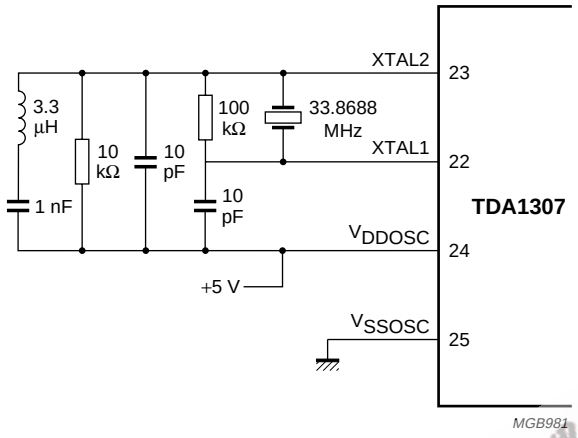


Fig.4 External crystal oscillator circuit.

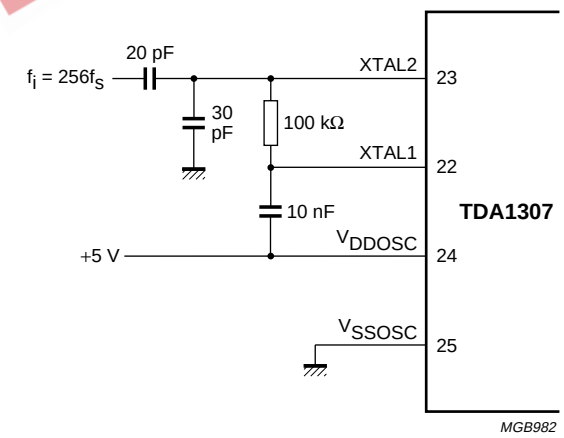


Fig.5 External clock input connections.

Microprocessor interface

The microprocessor interface provides access to virtually all of the functional blocks in the audio data processing section. Its destination is two-fold: system constants (such as input format and sample frequency) as well as system variables (attenuation, muting, de-emphasis, volume control data etc.) can be ‘written to’ the respective blocks (command mode), and continuously collected stereo peak data ‘read from’ the peak detection block (peak request). The system settings are stored in the TDA1307 in an internal register file. Peak data is read from the stereo peak value register.

THREE-LINE MICROPROCESSOR INTERFACE BUS

Communication is realized by a three-line bus, consisting of the following signals (see Fig.6):

- Clock input CL (pin 39), to be generated by the microprocessor
- Command/request input RAB (pin 42), by which either of the two mode commands (RAB = 0) and peak request (RAB = 1) are invoked
- Bidirectional data line DA (pin 38), which either receives command data from the microprocessor or outputs peak data from the peak detection block.

CL and RAB both default HIGH by internal pull-up, DATA is 3-state (high impedance, pull-up, pull-down).

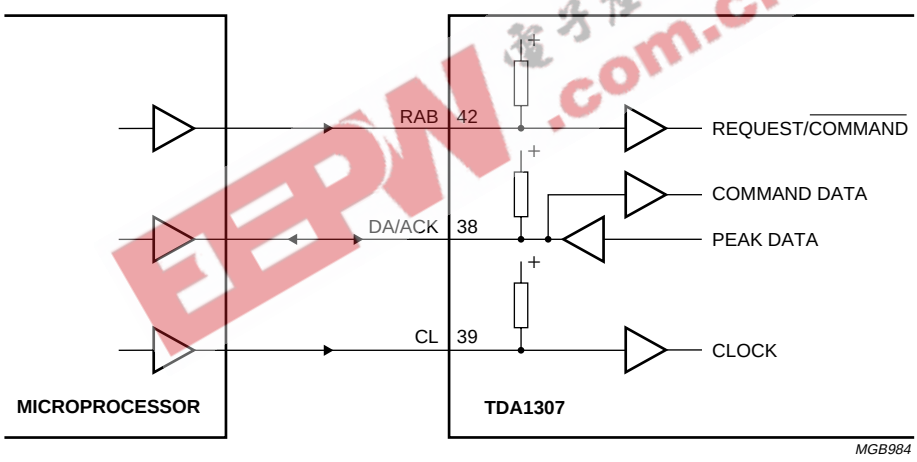


Fig.6 Three-line microprocessor interface bus.

Initialization of the bus receiver

The microprocessor interface section is initialized automatically by the power-on reset function, POR (pin 20). A LOW input on POR will initiate the reset procedure, which encompasses a functional reset plus setting of the initial states of the control words in the command register file. A wait time of at least one audio sample time after a LOW-to-HIGH transition of POR must be observed before communication can successfully be established between the TDA1307 and the microprocessor. In addition to the POR function, a software reset function issued from the microprocessor is provided (see section “Organization and programming of the internal register file”), which has the sole function of reinstating the initial values of the microprocessor control register. More information on initializing the TDA1307 can be found under “Application Information”.

Command protocol

The protocol for writing data to the TDA1307 is illustrated in Fig.7. The command mode is invoked by forcing RAB LOW. A unit command is given in the form of an 8-bit burst on the DA line, clocked on the rising edge of CL. The command consists of 4 address bits followed by 4 control data bits (both MSB first). A next command may be immediately issued while keeping RAB forced LOW. Only commands for which the MSB of the address bits is LOW are accepted; of the remaining set of addresses, only four have meaning (see section “Organization and programming of the internal register file”). The command input receiver is provided with a built-in protection against erroneous command transfer due to spikes, by a 2-bit debounce mechanism on lines DA and CL. The waveforms on these lines are sampled by the receiver at the internal system clock rate $256f_s$. A state transition on DA or CL is accepted only when the new state perseveres for two consecutive sampled waveform instants.

Organization and programming of the internal register file

Command data received from the microprocessor is stored in an internal register file (see Table 2), which is organized as a page of 10 registers, each containing a 4-bit command data word (D3 to D0). Access to the words in the register file involves two controls: selection of the address of a set of registers (by means of A3, A2, A1 and A0) and setting the number of the bank in which the desired register is located (by means of the ‘bank bits’ B0 and B1). First the desired bank is selected by programming the command word at address 0000 (supplying the bank bits plus refreshing bits ATT and DIM). A subsequent addressing (one of three addresses, 1H, 4H and 6H) will yield access to the register corresponding to the last set bank.

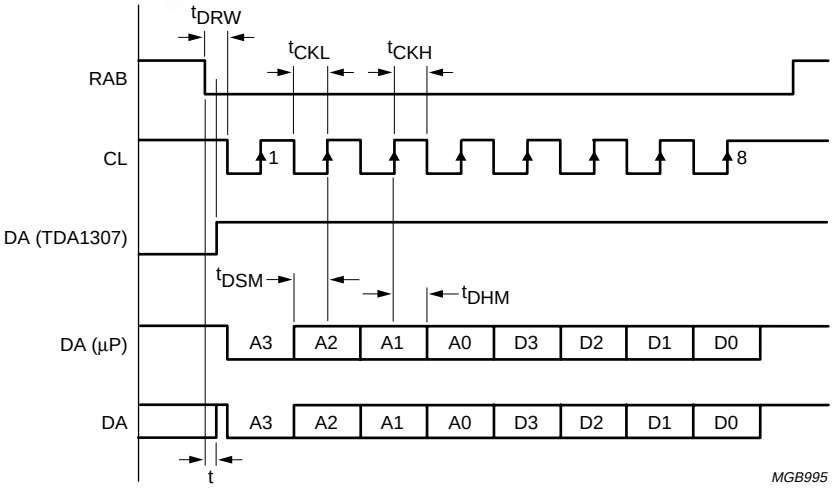


Fig.7 Microprocessor command protocol.

Table 2 Microprocessor control register file

ADDRESS						D3	D2	D1	D0	INITIAL STATE
A3	A2	A1	A0	BANK						
				B0	B1					
0	0	0	0	X	X	BANK B0	BANK B1	ATT	DIM	0 0 1 1
0	0	0	1	0	1	FCON	DIT	FSS9	FSS8	0 0 0 0
				1	0	FSS7	FSS6	FSS5	FSS4	0 0 1 0
				1	1	FSS3	FSS2	FSS1	FSS0	1 0 0 0
0	1	0	0	0	1	DCEN	DCSH	FN9	FN8	0 1 1 1
				1	0	FN7	FN6	FN5	FN4	0 0 0 0
				1	1	FN3	FN2	FN1	FN0	1 1 0 1
0	1	1	0	0	1	DEMC1	DEMC0	RES0	RES1	0 0 0 0
				1	0	INS1	INS0	FS1	FS0	0 0 0 0
				1	1	RES2	NS	RST	STBY	1 0 0 0

Following is a list of the programming values for the various control words in the register file. Information on the meaning of the different controls can be found under the sections covering the corresponding signal processing blocks (see sections “Multiple format input interface” to “Third and fourth order noise shaping”).

BANK B0, BANK B1

Programming of the bank bits is given in Table 2. The bank bits can be changed by addressing register location 0000. Subsequent addressing will result in access of locations according to the last selected bank.

ATT

Attenuation control bit: logic 1 to activate –12 dB attenuation, logic 0 to deactivate. As the attenuate control bit shares a control word with the bank bits, ATT has to be refreshed each time a new bank is selected.

DIM

Digital mute control bit: logic 1 to activate mute, logic 0 to deactivate. An active digital mute will override the attenuation function. As with ATT, DIM needs to be refreshed with each change in bank selection.

FCON

Fade function control bit: logic 1 to activate the fade function, logic 0 to deactivate.

DIT

Dither control bit: logic 1 to activate dither addition, logic 0 deactivates.

FSS9 to FSS0

Fade function 10-bit control value to program fade speed, in number of samples per fade step.

DCEN

DC-filter enable bit: logic 1 enables subtraction of the DC-level from the input signal, logic 0 disables.

DCSH

DC-filter sample or hold control bit: when DCSH = 0 the DC-level of the input signal is continuously evaluated. When DCSH = 1 the once acquired DC value, to be subtracted from the input signal, is held constant.

FN9 to FN0

Fade function 10-bit control value to program volume level.

DEMC1, DEMC0

De-emphasis function enable and f_s selection bits.

Table 3 De-emphasis mode programming

DEMC1	DEMC0	DE-EMPHASIS FUNCTION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32.0 kHz
1	0	de-emphasis for f_s = 44.1 kHz
1	1	de-emphasis for f_s = 48.0 kHz

Table 4 Input format programming

INS1	INS0	INPUT FORMAT
0	0	I^2S up to 20 bits
0	1	Sony format 16 bits
1	0	Sony format 18 bits
1	1	Sony format 20 bits

Table 5 Sample frequency indication programming

FS1	FS0	DOBM SAMPLE FREQUENCY INDICATION
0	0	f_s = 44.1 kHz
0	1	f_s = 48.0 kHz
1	0	no meaning
1	1	f_s = 32.0 kHz

RES2 to RES0

These are reserved locations and have no functional meaning in the TDA1307.

INS1, INS0

Input format selection control bits.

FS1, FS0

Sample frequency indication control bits for the digital output section.

NS

Control bit for Noise Shaper section. When NS = 0, 3rd order noise shaping is selected; when NS = 1, 4th order noise shaping is selected.

RST

Software reset function. When RST = 1 the contents of the microprocessor control registers will immediately be preset to their initial values as shown in Table 2. As part of this reset action, bit RST is automatically returned to its initial state 0, that being normal operation.

STBY

Standby mode control bit. When STBY = 1 the standby mode will be initiated (explained under the section treating the Digital Output block). STBY = 0 for normal activity.

PEAK DATA OUTPUT PROTOCOL

The peak data read-out protocol is illustrated in Fig.8. A peak request is performed by releasing RAB (which will be pulled HIGH by TDA1307) while CL = HIGH, and maintaining RAB = 1 throughout the peak data transmission. TDA1307 will acknowledge the peak request by returning a LOW state on the DA line. Upon this peak acknowledge, the microprocessor may commence collecting data from the internal peak data output register (16-bit Left, 16-bit Right channel peak data) by sending a clock onto the CL line. The contents of the peak data output register will not change during the peak request. The first peak bit, the MSB of the Left channel peak value, is output upon the first LOW-to-HIGH transition of CL. To access Right channel peak value, all 16 bits of channel Left have to be read out, after which up to 16 bits of Right channel peak data may be read out. The peak data read out procedure may be aborted at any instant by returning RAB LOW, marking the end of the peak request: the internal peak register will be reset and the peak detector will start collecting new peak data and transferring this to the peak data output register.

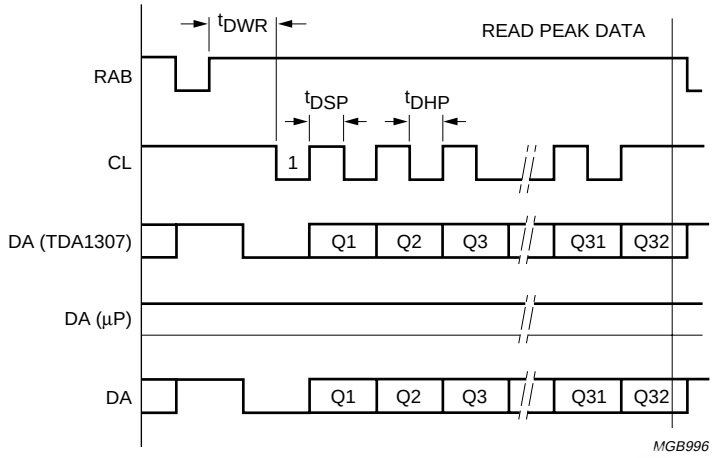


Fig.8 Peak data output protocol.

Multiple format input interface

Data input to the TDA1307 is accepted in four possible formats, I^2S (with word lengths of up to 20 bits), and Sony formats of word lengths 16, 18 and 20-bit. The general appearance of the allowed formats is given in Fig.9. The selection of a format is achieved through programming of the appropriate bits in the microprocessor register file. Characteristic timing for the input interface is given in the diagram of Fig.10.

SYNCHRONIZATION

For correct data input to reach the central controller of TDA1307, synchronization needs to be achieved to the incoming $1f_s$ I^2S or Sony format input signals.
The incoming WS signal is sampled to detect whether its phase transitions occur at the correct synchronous timing instants. This sampling occurs at the TDA1307 internal clock rate, $256f_s$. After one phase transition of WS, the next is expected after a fixed delay, otherwise the condition is regarded as out-of-lock and a reset is performed, this operation is repeated until synchronization is achieved. To allow for slight disturbances causing unnecessary frequent resets, the critical WS transitions are expected within a tolerance window (–4 to +4 periods of the $256f_s$ internal sampling clock instants).

The reset action is flagged on the RESYNC (pin 19) output, which may be optionally used for muting or related purposes. RESYNC becomes HIGH the instant a reset is initiated, and remains in that state for at least one sample period ($1/f_s$).

ERROR FLAG INPUT EFAB

The error flag input EFAB (pin 4) is intended as request line from the system decoder to the digital filter to indicate erroneous audio samples requiring concealment.
A detected HIGH on input EFAB will be relayed by the input interface block to the error concealment block, where the samples flagged as erroneous will be processed accordingly.

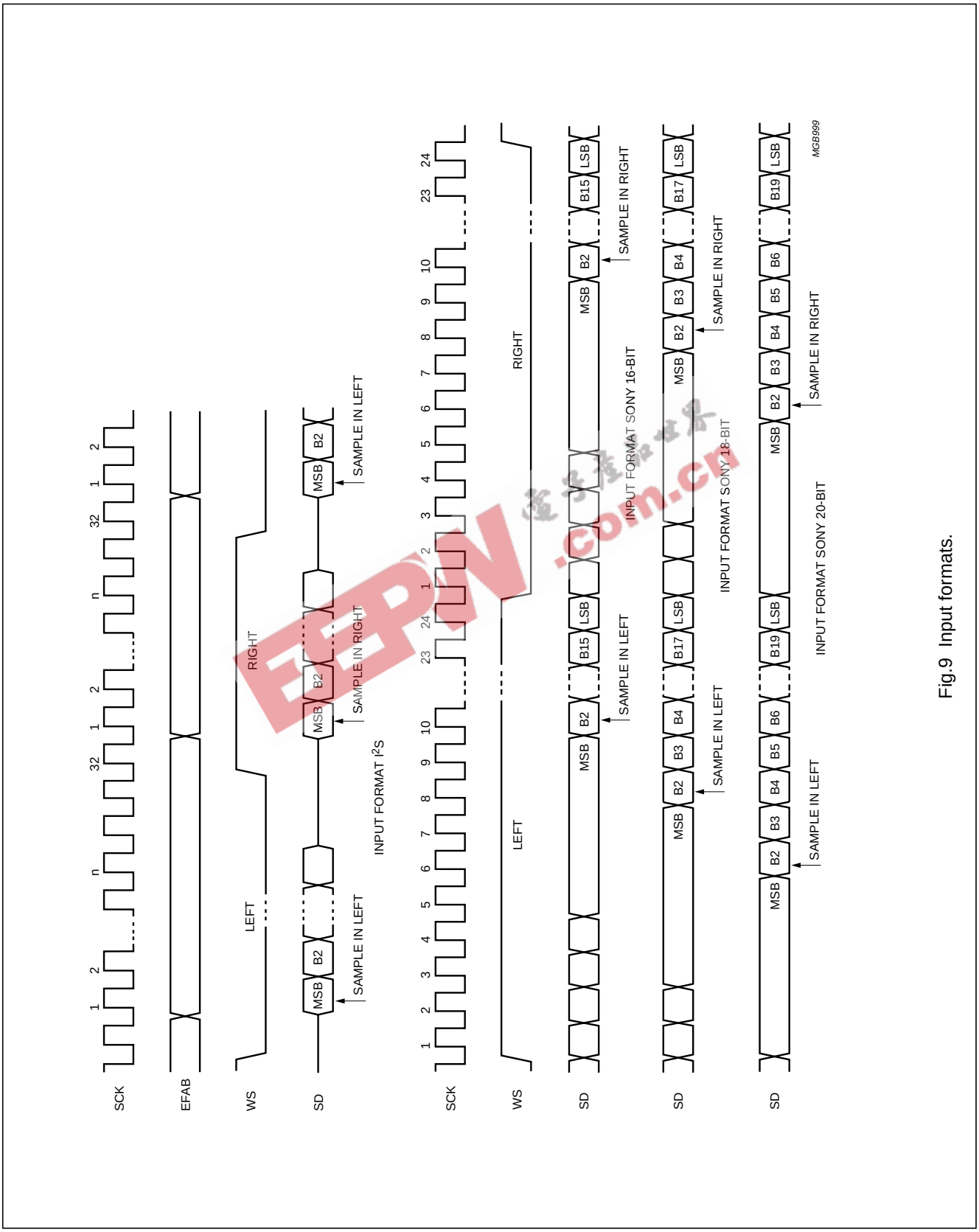


Fig.9 Input formats.

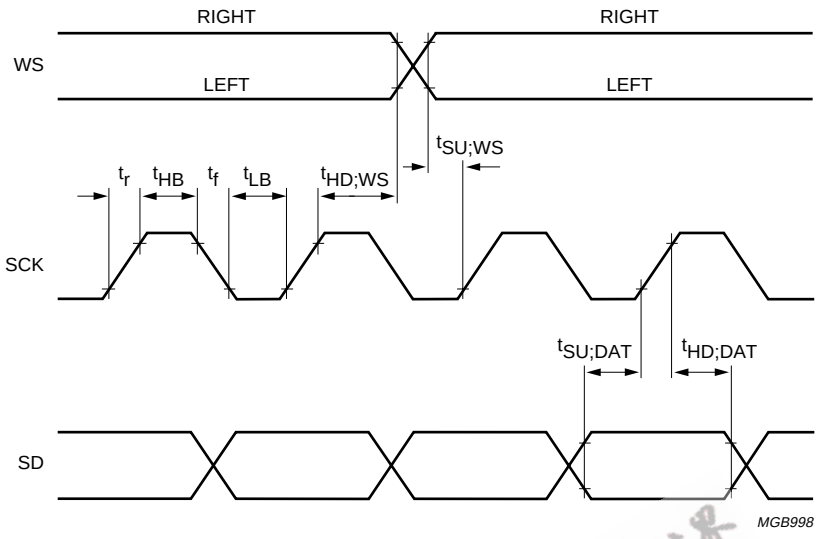


Fig.10 Typical I²S-bus data waveforms.

Error concealment, interpolation and muting

The error concealment functional block performs three functions:

1. interpolation of up to eight consecutive erroneous audio samples flagged as such by input EFAB
2. attenuation
3. muting of incoming audio, both the latter if so activated by means of the microprocessor registers.

Furthermore, as these functions constitute error processing functions, operation of any of these functions is reported to the digital output DOBM by setting the validity flag.

EIGHT-SAMPLE INTERPOLATION

Incoming audio samples may be visualized as entering a memory pipeline, nine audio sample instants in depth, upon entering the error concealment block. Any audio samples marked as erroneous by the flag input EFAB will be reconstructed by linear approximation from the values of the adjacent correct samples (the last correct sample still available, and the next correct sample). The linear interpolation is started as soon as a correct sample becomes available within nine sampling instants. Should a flagged erroneous condition persevere for over eight sampling instants, then the last correct sample will be held for as long as necessary, i.e. until the next correct sample enters the pipeline. The linear approximation is then initiated over the maximum interpolation interval of eight sampling instants.

ATTENUATION

The concealment block incorporates a digital –12 dB attenuation function intended to be used in program search or other player actions that may generate audible transitional effects such as loud clicks. The attenuate function is activated by means of bit ATT in the microprocessor register file. Setting this bit to logic 1 causes the next audio sample (attenuate never takes action on incomplete samples) to be attenuated with immediate effect (the validity flag of the digital audio output DOBM is set).

The interpolation facility is called upon when an attenuate command is given while the incoming data is flagged as invalid by EFAB. If no more than eight samples in succession are invalid, attenuate may take immediate effect (this causes the output value to ramp linearly to the final attenuated level). If nine or more samples in a row are flagged erroneous, attenuation is postponed and the last good sample held, until the next good sample becomes available. Upon that instant, the output ramps linearly, over the maximum interpolation time span, to the attenuated first correct sample. Releasing attenuate (bit ATT reset to 0) always has immediate effect (i.e. the next complete audio sample will pass unattenuated).

MUTING

The digital mute of the error concealment block immediately (i.e. on the next whole audio sample) sets the input to the digital filter to all zeros, regardless of any other current action in the error concealment block. The digital mute function is activated by means of bit DIM in the microprocessor register file. Setting this bit to logic 1 causes the next audio sample to be muted (the validity flag of the digital audio output DOBM is set).

Releasing the digital mute function (resetting bit DIM to 0) will cause the output of the error concealment block to approach the unaffected audio sample value by linear approximation, on the condition that the mute action spanned at least 8 consecutive audio samples. If there are samples in error at the time of releasing mute, the release action is postponed until good data becomes available, after which the linear ramp can be made over the maximum interpolation time span.

Digital output (DOBM)

The DOBM block constructs a biphase modulated digital audio output signal which complies to the IEC standard 958, to be used as a digital transmission link between digital audio systems. A variety of inputs are combined, arranged and modulated to finally form the output biphase-mark sequence. The inputs are the following:

- left and right audio data, word length 20-bit, as delivered by the error concealment block
- the Validity flag as output by the error concealment block
- subcode information, as acquired by input via pins SBDA (pin 6) and SBCL (pin 5)
- sampling frequency information as set by means of bits FS1 and FS0 in the microprocessor register file.

As the digital output function is not always required, and can give rise to interference problems in high-quality audio conversion systems, the DOBM output can be switched **on** or **off** by means of pin DSTB (digital output standby, 13). Leaving DSTB open-circuit will cause it to pull HIGH and deactivate the DOBM output; tying DSTB LOW enables the digital output function.

The programming of bits FS1 and FS0 is specified in Table 5 under section “Microprocessor interface”. The DOBM block of TDA1307 translates the settings of these bits to the appropriate corresponding information in the digital audio output sequence (as specified by IEC 958).

The inputs SBDA (subcode data, 6) and SBCL (subcode clock, 5) allow for the merging of subcode data into the output DOBM signal. The input sequence via these inputs is defined as 10-bit burst words, arranged as illustrated in Fig.11; the bit nomenclature corresponds to that used in the IEC standard 958. Both subcode data and clock signals are normally supplied by the decoder of the digital audio system (e.g. SAA7310).

For set-up and hold timing of the SBDA and SBCL inputs, restrictions identical to the audio data inputs are valid.

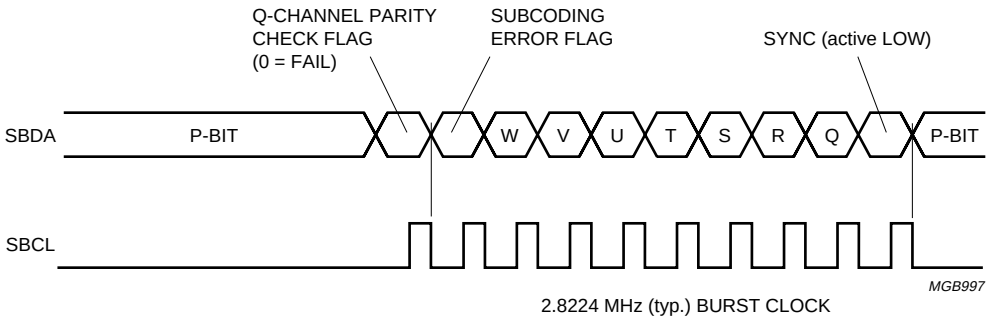


Fig.11 Format of subcode data input.

Digital silence detection

The TDA1307 is designed to detect digital silence conditions in channels left and right, separately, and report this via two separate output pins, one for each channel, DSL (pin 11) and DSR (pin 12). This function is implemented to allow for external manipulation of the audio signal upon absence of program material, such as muting or recorder control. The TDA1307 itself does not influence the audio signal as a result of digital silence; the sole function of this block is detection, and any further treatment must be accomplished externally.

An active LOW output is produced at these pins if the corresponding channel carries either all zeroes for at least 8820 consecutive audio samples
(200 ms for f_s = 44.1 kHz).

The digital silence detection block receives its left and right audio data from the error concealment block (implying that a digital mute action will produce detection of a digital silence condition), and passes it unaffected to the next signal processing stage, the de-emphasis block.

De-emphasis filter

The TDA1307 incorporates selectable digital de-emphasis filters, dimensioned to produce, with extreme accuracy, the de-emphasis frequency characteristics for each of the three possible sample rates 32, 44.1 and 48 kHz. As a 20-bit dynamic range is maintained throughout the filter, considerable margin is kept with respect to the normal CD resolution of 16-bit i.e. the digital de-emphasis of TDA1307 is a truly valid alternative to analog de-emphasis in high-performance digital audio systems.

Selection of the de-emphasis filters is performed via the microprocessor interface, bits DEMC1 and DEMC0, for which the programming is given in Table 3.

Oversampling digital filter

The oversampling digital filter in the digital audio reconstruction system is of paramount influence to the fidelity of signal reproduction. Not only must the filter deliver a desired stop-band suppression while sustaining a certain tolerated pass-band ripple, but it must also be capable of faithfully reproducing signals of high energy content, such as signals of high level and frequency, square wave-type signals and impulse-like signals (all of these examples have their counterparts in actual music program material). Filters optimized only towards pass-band ripple and stop-band suppression are capable of entering states of overload because of the clustered energy content of these signals, thus introducing audible degradations in processing the mentioned types of excitations. To dimension a high-fidelity digital filter, a balance must be established between filter steepness and overload susceptibility.

The oversampling digital filter function in the TDA1307 is designed, in combination with the noise shaper, to deliver the highest fidelity in signal reproduction possible. Not only are stop-band suppression and pass-band ripple parameters to the design, but also the prevention of detrimental artifacts of too extreme filtering: impulse and high-level overload responses. The outcome is a patented design excelling in natural response to most conceivable audio stimuli. It is realized as a series of three half-band filters, each oversampling by a ratio of two, thus achieving an eight times oversampled and interpolated data output to be input to the noise shaper. Each stage has a finite impulse response with symmetrical coefficients, which makes for a linear phase response. Filter stages 1, 2 and 3 incorporate 119, 19 and 11 delay taps respectively. To maintain an output accuracy of 20 bits, an internal data path word length of 39 bits is used to supply the required headroom in multiplications. Requantization back to 20-bit word length is performed by noise shaping (thus effectively preventing rounding errors in so far as they have effect in the audio frequency band), at the output of each filter section.

The successive half-band filter stages are, for efficiency, distributed over the audio data processing path: DC-filtering, peak value reading and volume control are performed between stages 1 and 2 (the $2f_s$ domain).

DC-cancelling filter

A mechanism for optionally eliminating potential DC content of incoming audio data is implemented in the TDA1307 for three main reasons. Most importantly because it is called for by the implementation of volume control in the TDA1307. An audio signal that is to be subjected to volume control (multiplication by a controlled attenuation factor) should be free of offset, otherwise the controlled multiplication will produce the undesired side effect of modulating the average DC content. The second reason is supplied by the implementation of audio peak data read-out in the TDA1307. As the peak value is obtained from the absolute value of the audio data referenced to zero DC level, its accuracy is impaired by the presence of residual DC information, progressively so for lower audio levels. The third reason is brought about by application of the noise shaper. To optimize the dynamic behaviour of the noise shaper especially for low-level signals, it is supplied a predefined offset, sometimes referred to as DC dither. Taking no precautions against DC

content of the source audio data may render the DC dither potentially ineffective.

In applications where the DC content of the audio information may be expected, application of the selectable DC filter may be opted for. It is implemented as a first-order high-pass filter with a corner frequency of 2 Hz. Control of the DC filter is achieved by accessing the appropriate bits DCEN (DC filter enable) and DCSH (DC filter sample or hold) in the microprocessor register file. The principle of operation is illustrated in Fig.12. The output of the DC filter, referred to in the diagram as 'audio output' always equals the audio input subtracted by the output of the low-pass branch. Depending on the control bit DCSH, this subtraction value is either the last value held constant or a value continuously adapting to incoming DC content. The DC filter is effectively switched **on** or **off** via control bit DCEN, which selects the input of the low-pass section either to be the audio input data (the output of the low-pass section will settle to the low frequency content of the audio data so that the filter is **on**) or a preset value of zero (low-pass output will settle to zero meaning 'filter **off'**). The constant mode is implemented to provide a mode in which a stable subtraction value is guaranteed; in this mode however the high-pass function is inhibited so there is no adaptation to changes in the DC content of the incoming source information.

Peak detection

The TDA1307 provides a convenient way to monitor the peak value of the audio data, for left and right channels individually, by way of read-out via the microprocessor interface. Peak value monitoring has its applications mainly in digital volume unit measurement and display, and in automatic recording level control. The peak level measurement of the TDA1307 occurs with a resolution of 16-bit, providing a dynamic range amply suitable for all practical applications.

The output of the peak detection block is a register of two 16-bit words, one for each channel, representing the absolute value of the accumulated peak value, accessible via the microprocessor interface. The peak detection block continuously monitors the audio information arriving from the DC-cancelling filter, comparing its absolute value to the value currently stored in the peak register. Any new value greater than the currently held peak value will cause the register to assume the new, greater value. Upon a peak request (for which the protocol is described in section "Peak data output protocol"), the contents of the peak register are transferred to the microprocessor interface. After a read action, the peak register will be reset, and the collection of new peak data started.

The peak detection block receives data that has been processed by the first half-band stage of the oversampling interpolating digital filter (in the $2f_s$ domain, but the peak detection 'samples' at $1f_s$ for efficiency). This means that the scaling applied in this first half-band stage is noticeable in the measured peak value. The frequency-independent attenuation factor of the first half-band filter equals 0.175 dB - this results in a possible range for the output peak value of 0 to 32114. When the audio signal may be expected to carry DC content, use of the DC cancelling filter of TDA1307 is recommended, to ensure correct and accurate peak detection.

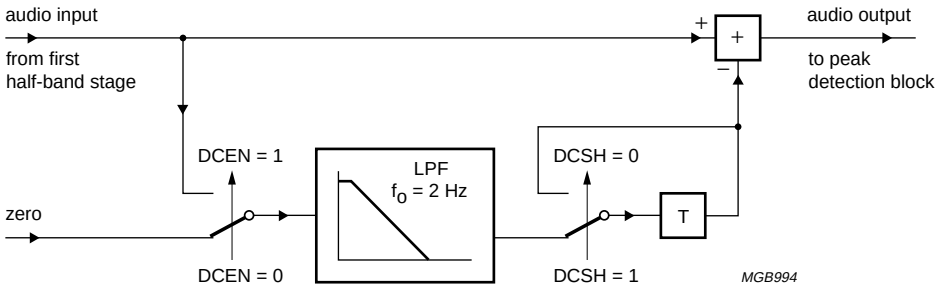


Fig.12 Schematic diagram of the DC filter.

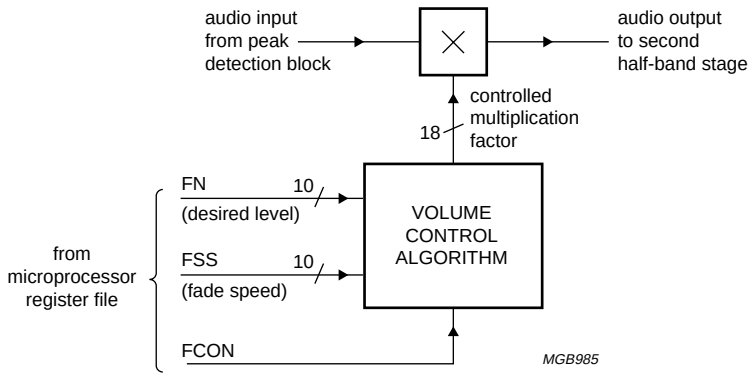


Fig.13 Schematic diagram of the volume control block.

Fade function and volume control

One of the main features of TDA1307 is a patented, advanced digital volume control with inherent fading function, exhibiting an accuracy and smoothness unsurpassed in presently available digital filters. Only the desired volume and the fade speed need to be instructed to the TDA1307, which can be realized in a single instruction via the microprocessor interface. The volume control function then autonomously performs automatic fade in or fade out to the desired volume by a natural, exponential approach. It allows for volume control to an accuracy of 0.1 dB over the range from 0 dB of full scale to beyond −100 dB. The speed of approach can be set over a wide range, varying from less than one second to over 23 seconds for a complete fade. Furthermore the fade algorithm manages the additional fading resolution, in excess of the 0.1 dB available for the volume desired level, needed to ensure gradual changes in volume at all times. Figure 13 illustrates the volume control block.

Three data entities in the microprocessor register file pertain to the volume control block: a 10-bit control value for the desired volume (bits FN9 to FN0), a 10-bit control value for the fade speed (bits FSS9 to FSS0), and the fade function override bit, FCON. The volume control word ranges from 0 (representing a desired volume level or 0 dB) to 1023 (representing maximum desired volume level of zero or −∞ dB). For values 1 to 1023, an LSB change of the volume control word represents 0.1 dB change of volume level. In changing from one volume level to the next desired volume level, the volume control block calculates and applies intermediate volume levels according to an exponential approach curve. The speed at which the approach curve progresses is determined by the value of the fade speed control word, FSS. FSS + 2 is the amount of time delay applied, in units of audio sample instants, before a next value on the exponential curve is calculated and applied.

The total duration of an exponential fade operation is the product of the desired amount of volume change FN (in LSBs of the 10-bit control word) and the amount of delay per fade step FSS (in LSB times seconds), expressed as follows:

$$t_{fade,\ exp,\ total} = \Delta FN \times \frac{(FSS + 2)}{f_s},$$

where f_s is the base-band sampling frequency.

Thus the longest fade time achievable, occurring in the event of maximum desired volume change $\Delta FN = 1023$, slowest speed setting FSS = 1023, and in the event that f_s = 44.1 kHz, is 23.7 seconds.

To smooth out fast volume changes however, the TDA1307 fade function adds extra resolution to the volume control by gradually changing from one exponential step to the next, by a linear transition. Whereas the 10-bit FN-value could not accomplish discrete attenuation steps finer than 0.1 dB, the linear transitional approach enhances volume change resolution to 15-bit. The volume level therefore never changes faster than one LSB of the 15-bit attenuation factor per audio sample. As soon as the linear transition reaches the value

determined by the exponential approach, the attenuation value remains stable until the next exponential value is due, which will again initially be approached linearly. For exponential fade speeds higher than the linear approach can follow, the approach remains linear unless the exponential approach curve is intersected. For fast volume decrease, the start of the approach will be linear, whereas for a fast volume increase, the course of the fade approach will be exponential at first, then saturating to linear.

The fastest fade speed, for large volume changes, is therefore determined by the linear approach. For a maximum volume change at maximum speed, follows a fade time of $(2^{15} - 1)/44100 = 0.74$ seconds.

For immediate return to the maximum volume level without altering the volume and fade speed settings, bit FCON in the register file can be used. With this bit set to 1, the fade function is active and operates as described above. Resetting FCON to 0 will immediately deactivate the fade function, that is, return the volume level to maximum at the start of the next audio sample. Changing state of FCON from 0 to 1 will cause a fade according to the current settings of volume and speed control words FN and FSS.

In Fig.14, a few fading examples illustrate the operation of the TDA1307 advanced digital volume control.

Dither and scaling

Prior to input to the noise shaper, final preprocessing is performed upon the eight times oversampled and interpolated audio data stream in the form of scaling and dither addition. The fixed scaling factor, a frequency-independent attenuation of 3 dB, is applied to the signal in order to provide the noise shaper with sufficient headroom. The application of dither is optional, selectable by means of bit DIT in the microprocessor register file.

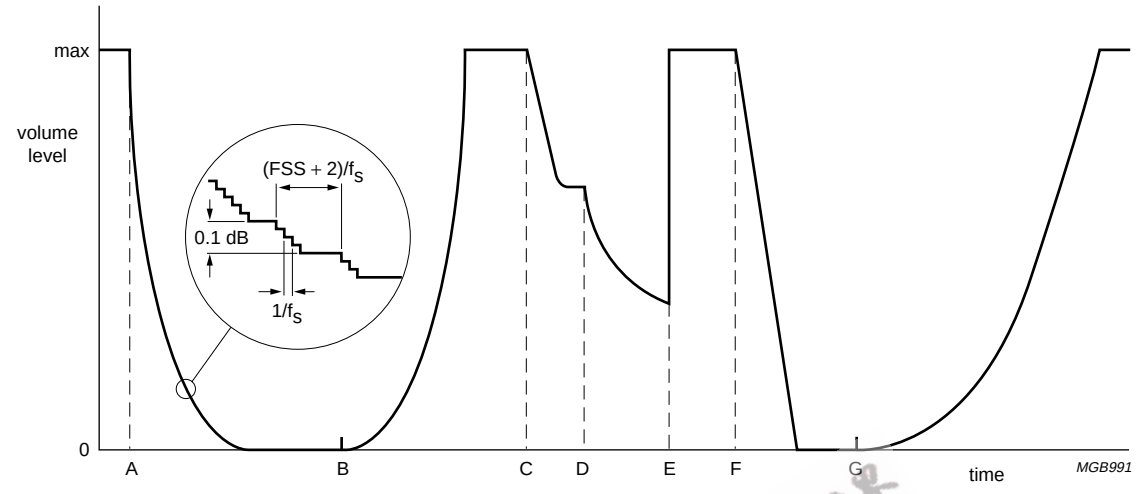
With DIT set to 1, fixed dither levels of value $2^{-6} + 2^{-5}$ and $2^{-6} - 2^{-5}$ are added alternately to the audio signal, at an alternation rate of $4f_s$. This amounts to a combination of an AC dither signal of frequency $4f_s$ and amplitude –24 dB of full-scale, with a DC dither (offset) of 3.125% of full-scale peak amplitude. With DIT set to 0, no dithering, AC or DC, is performed.

Although the addition of dither is made selectable in the TDA1307, it is generally recommended for use always, as dither is essential to the accurate conversion of low-level signals and reproduction of silence conditions by noise-shaping circuits.

Third and fourth order noise shaping

The noise shaper constitutes the final audio processing stage of TDA1307, which takes the eight times oversampled and interpolated audio data stream from the digital filter as input, and by extreme oversampling and 1-bit end quantization processes the signal so that it can be converted to analog by a one-bit digital-to-analog converter. The order of the noise shaper is selectable, between 3rd and 4th order, by means of the register file bit NS (NS = 0: 3rd order, NS = 1: 4th order). Together with the final oversampling ratio, the noise shaper order determines the dynamic range (or accuracy) that the noise shaper can achieve (the oversampling ratio will depend on the system clock frequency and application mode used). Table 6 gives the dynamic range of the noise shaper as a function of these two parameters.

Figures 15 and 16 show noise spectral density simulations of the third and fourth order noise shaper respectively, with a stimulus frequency of 1 kHz at a level of –10 dBf_s, for 192×44.1 kHz oversampling. From the slope of the shaped noise spectrum outside the audio band, the order of noise shaping is apparent. It is important to note that, in contrast to normal fourth-order noise shaping, where an audio post-filter of equal order would be needed to compensate the slope of the quantization noise, the fourth-order noise shaper of the TDA1307 actually only needs third order post-filtering to obtain the same amount of stop-band suppression as with third order. The noise density of the fourth order noise shaper starts at a lower level for low frequencies, and only slightly exceeds the third-order curve in the 200 to 300 kHz region.



A: Fade out to zero (FN = 0).
B: Fade in to maximum volume (FN = 1023).
C: Fast volume decrease resulting in initial linear regulation.
D: Slow volume decrease predominantly exponential.
E: Volume regulation overridden by resetting FCON to 0.
F: FN = 0, FSS = 0, FCON to 1 causes fastest maximum fade with linear regulation.
G: Medium speed volume increase starts exponential, ends linear.

Fig.14 Volume control examples.

Table 6 Noise shaper dynamic range

OVERSAMPLING/ORDER	3rd ORDER	4th ORDER
$128f_s$	105 dB	118 dB
$192f_s$	117 dB	134 dB

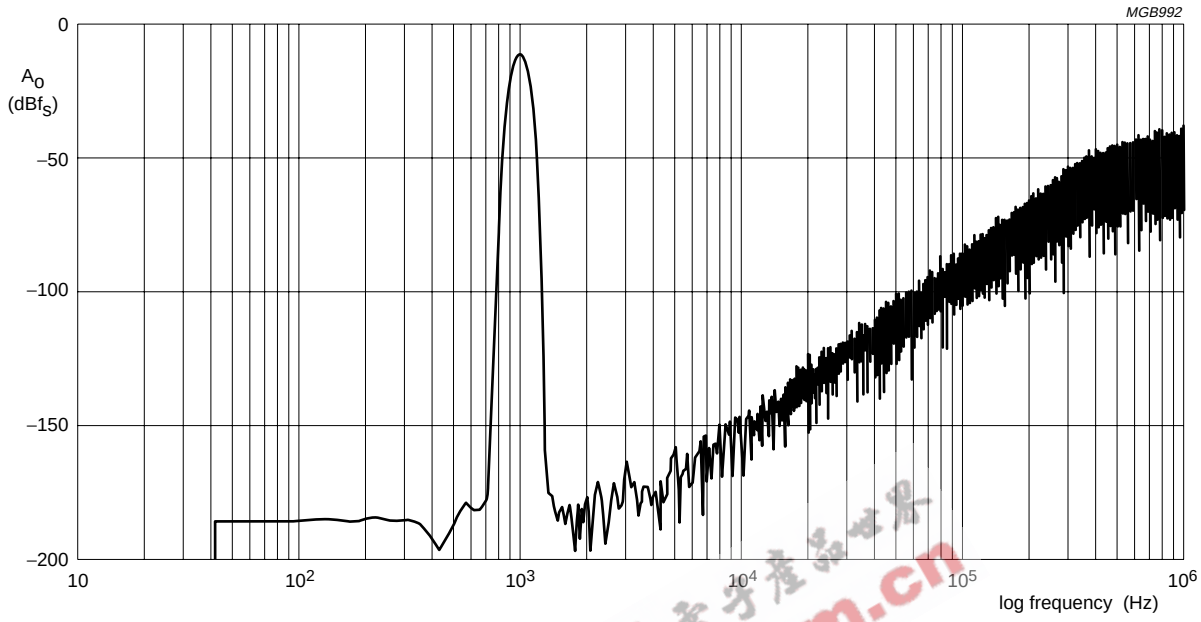


Fig.15 Noise shaper output spectrum (N = 3; 192f_s).

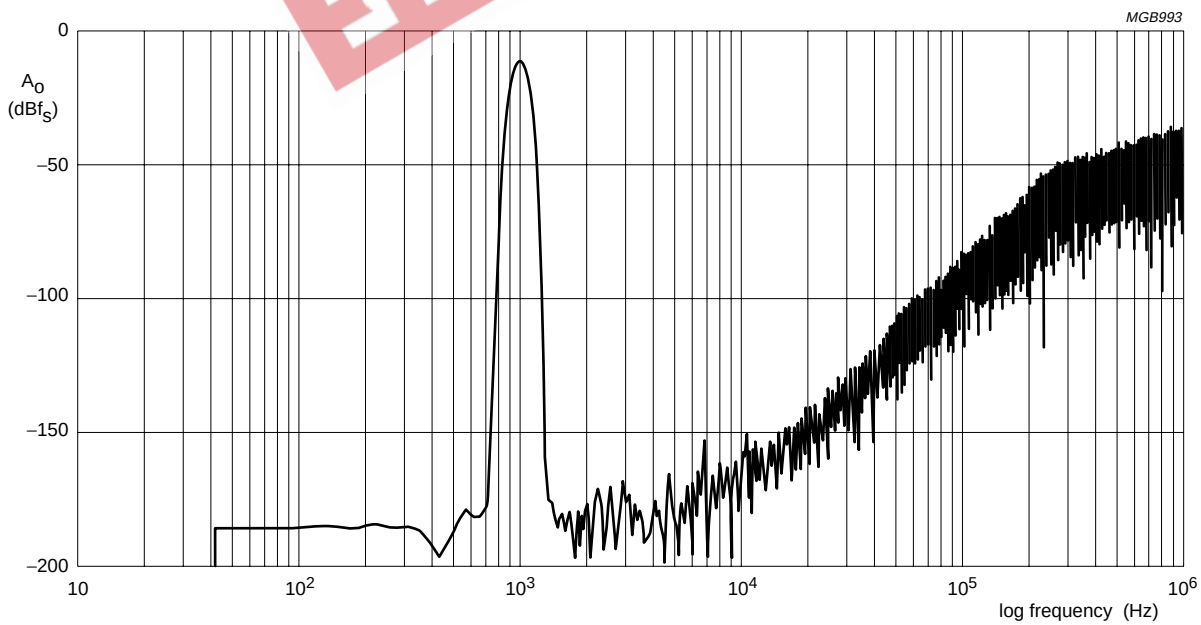


Fig.16 Noise shaper output spectrum (N = 4; 192f_s).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltages (pins 8, 21, 24, 29, 32 and 41)		–0.5	+6.5	V
V_I	maximum input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{IK}	DC clamp input diode current	$V_I < –0.5$ V or $V_I > V_{DD}$ + 0.5 V	–	±10	mA
I_{OK}	DC output clamp diode current; (output type 4 mA)	$V_O < –0.5$ V or $V_O > V_{DD}$ + 0.5 V	–	±20	mA
I_O	DC output source or sink current; (output type 4 mA)	$–0.5 \text{ V} < V_O < V_{DD}$ + 0.5 V	–	±20	mA
I_{DD}, I_{SS}	DC V_{DD} or GND current per supply pin		–	±50	mA
$P_{O, cell}$	power dissipation per output (type 4 mA)		–	50	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	100 pF; 1.5 kΩ	–2000	+2000	V

Note

1. Input voltage should not exceed 6.5 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	39	K/W

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to +70 °C and oscillator frequency 33.8688 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDC1,2,3}$	supply voltage (pins 8, 21 and 41)		4.5	5.0	5.5	V
V_{DDOSC}	supply voltage (pin 24)		4.5	5.0	5.5	V
V_{DDAR}	supply voltage (pin 32)		4.5	5.0	5.5	V
V_{DDAL}	supply voltage (pin 29)		4.5	5.0	5.5	V
V_{diff}	maximum difference between supplies		–	–	tbf	V
$I_{DDC1,2,3}$	supply current (pins 8, 21 and 41)	V_{DD} = 5 V	–	75	–	mA
I_{DDOSC}	supply current (pin 24)	V_{DD} = 5 V	–	2	–	mA
I_{DDAR}	supply current (pin 32)	V_{DD} = 5 V	–	2	–	mA
I_{DDAL}	supply current (pin 29)	V_{DD} = 5 V	–	1	–	mA
Inputs						
CLC1, CLC2, EFAB, SCK, WS, SD, SBCL, DA, SBDA, CDCC, TEST1 AND TEST2						
V_{IL}	LOW level input voltage	note 1	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	note 2	–1	–	+1	µA
R_I	input resistance	note 3	17	–	134	kΩ
C_I	input capacitance		–	–	10	pF
CL, RAB, POR, DSTB AND MODE						
V_{IL}	LOW level input voltage	note 1	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.8V_{DD}$	–	–	V
R_I	input resistance	note 3	17	–	134	kΩ
C_I	input capacitance		–	–	10	pF
Outputs						
CDEC AND CMIC (TYPE 4 MA)						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −4 mA	V_{DD}−0.5	–	–	V
C_L	load capacitance		–	–	30	pF
CDAC (TYPE TBF MA)						
V_{OL}	LOW level output voltage	I_{OL} = 8 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −8 mA	V_{DD}−0.5	–	–	V
C_L	load capacitance		–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DOR, DOL, NDOR AND NDOL (TYPE CUSTOM MA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	100	pF
DOBM (TYPE 12 MA)						
V_{OL}	LOW level output voltage	I_{OL} = 12 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –12 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
DSR, DSL AND RESYNC (TYPE 2 MA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
DA (TYPE 2 MA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
R_{Lint}	internal load resistance		17	–	134	kΩ
Crystal oscillator						
INPUT: XTAL1						
gm	mutual conductance	f = 2 MHz	–	0.4	–	mS
G_v	small-signal voltage gain	$G_v = gm \times R_O$	–	72	–	
I_{LI}	input leakage current	note 2	–1	–	+1	μA
C_I	input capacitance		–	10	–	pF
Timing						
f_{XTAL}	operating frequency		33.8688			MHz
SCK, WS, DATA, SBDA, SBCL AND EFAB (SEE FIGS 8 AND 9)						
f_{CL}	SBCL clock frequency	note 3	–	–	$64f_s$	Hz
f_{SCK}	SCK clock frequency		–	–	$64f_s$	Hz
f_{WS}	WS clock frequency		–	$f_{XTAL}/768$	–	Hz
t_{LB}	clock time LOW		110	–	–	ns
t_{HB}	clock time HIGH		110	–	–	ns
t_r	input rise time		–	–	20	ns
t_f	input fall time		–	–	20	ns
$t_{SU:DAT}$	data set-up time		20	–	–	ns
$t_{HD:DAT}$	data hold time		0	–	–	ns
$t_{SU:WS}$	WS set-up time		20	–	–	ns
$t_{HD:WS}$	WS hold time		0	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MICROCONTROLLER INTERFACE (SEE FIGS 6 AND 7)						
f_{CK}	CL input clock frequency		–	–	$46f_s$	kHz
t_{CKL}	input clock time LOW		2.0	–	–	µs
t_{CKH}	input clock time HIGH		2.0	–	–	µs
t_{DSM}	microprocessor data set-up time after CL LOW-to-HIGH transition		1.0	–	–	µs
t_{DHM}	microprocessor data hold time after CL LOW-to-HIGH transition		2.0	–	–	µs
t_{DSP}	peak data set-up time after CL LOW-to-HIGH transition		2.0	–	–	µs
t_{DHP}	peak data hold time after CL LOW-to-HIGH transition		2.0	–	–	µs
t_{dRW}	delay to write after read		2.0	–	–	µs
t_{dWR}	delay to read after write		2.0	–	–	µs
DOBM CIRCUIT						
f_{DOBM}	data output frequency		–	$128f_s$	–	Hz
t_r	output rise time	C_L = 50 pF	–	–	10	ns
t_f	output fall time	C_L = 50 pF	–	–	10	ns
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		5	–	–	ns
CLOCK GENERATOR CIRCUIT (NOTE 4)						
f_{XTAL1}	XTAL1 input clock frequency	slave mode	–	$256f_s$	–	Hz
f_{CDEC}	CDEC output clock frequency		–	$256f_s$	–	Hz
f_{CMIC}	CMIC output clock frequency		–	$96f_s$	–	Hz

Notes

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{I(min)}$ measured at V_I = 0 V; $I_{I(max)}$ measured at $V_I = V_{DD}$; not valid for pins with pull-up/pull-down resistors.
3. $I_{I(min)}$ measured at V_I = 0 V (pull-up); $I_{I(max)}$ measured at $V_I = V_{DD}$ (pull-down); valid for pins with pull-up/pull-down resistors.
4. Crystal frequency: 33.8688 MHz ($768f_s$), the oscillator circuit oscillates at a frequency that is approximately 0.01% above the crystal frequency.

QUALITY SPECIFICATION

In accordance with “SNW-FQ-611E”. The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. This handbook can be ordered using the code 9397 750 00192.

APPLICATION INFORMATION

Application modes

TDA1307 can be used as a digital reconstruction filter for CD, DCC, DAB and DAT applications. The configuration for these different applications is given in Table 7.

Table 7 Application modes

MODE	CDCC	CRYSTAL	CLOCK INPUT	BITSTREAM OUTPUT	SAMPLING FREQUENCY
CD	1	$768f_s$	–	$192f_s$	44.1 kHz
DCC	0	–	$256f_s$	$128f_s$	32.0 or 44.1 or 48.0 kHz
DAB	0	–	$256f_s$	$128f_s$	32.0 kHz
DAT	0	–	$256f_s$	$128f_s$	32.0 or 44.1 or 48.0 kHz

The crystal frequency for TDA1307, when operating in master mode, is $768f_s$ (f_s = 44.1 kHz). TDA1307 can also operate in slave mode, in which the clock input receives a clock signal of $256f_s$ (f_s = 32.0, 44.1 or 48.0 kHz). In the latter configuration, no resonator is connected to TDA1307.

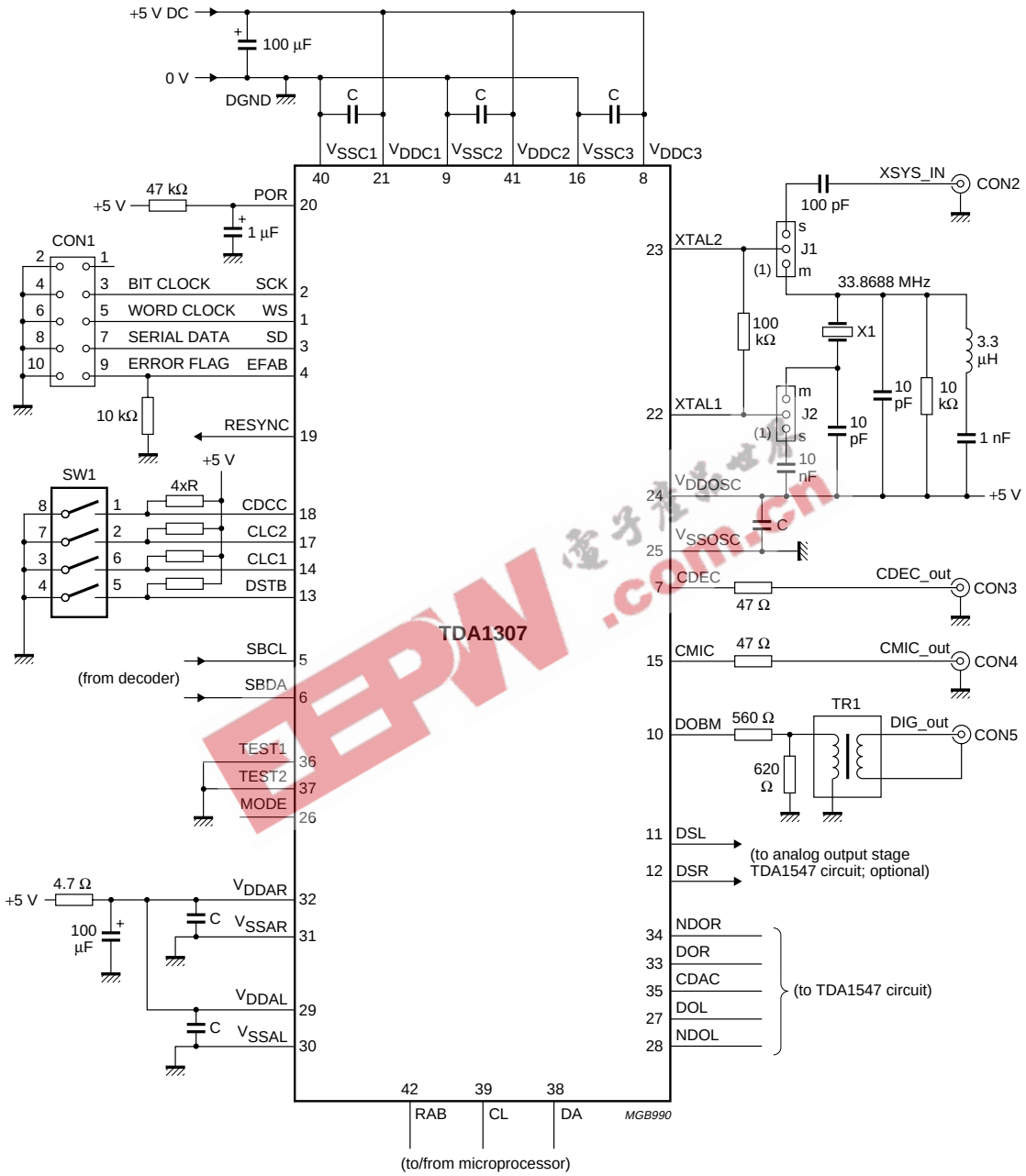
Basic application

Figures 17 to 20 show the connections for an example of a complete bitstream reconstruction system, using TDA1307 together with TDA1547, as implemented in a demonstration application printed-circuit board. Figure 15 shows the connections pertaining to TDA1307. Both master and slave operation is possible, by setting of switches J1 and J2, and by programming the desired mode and frequency divisions by switch block SW1. Both test pins of TDA1307 are tied to ground in order to obtain immunity to crosstalk from the adjacent clock output CDAC. At pin POR (pin 20), an RC-timing network presets a typical power-on-reset LOW-time (10 ms for an instantaneously setting 5 V supply).

Typical application with TDA1547 Bitstream DAC

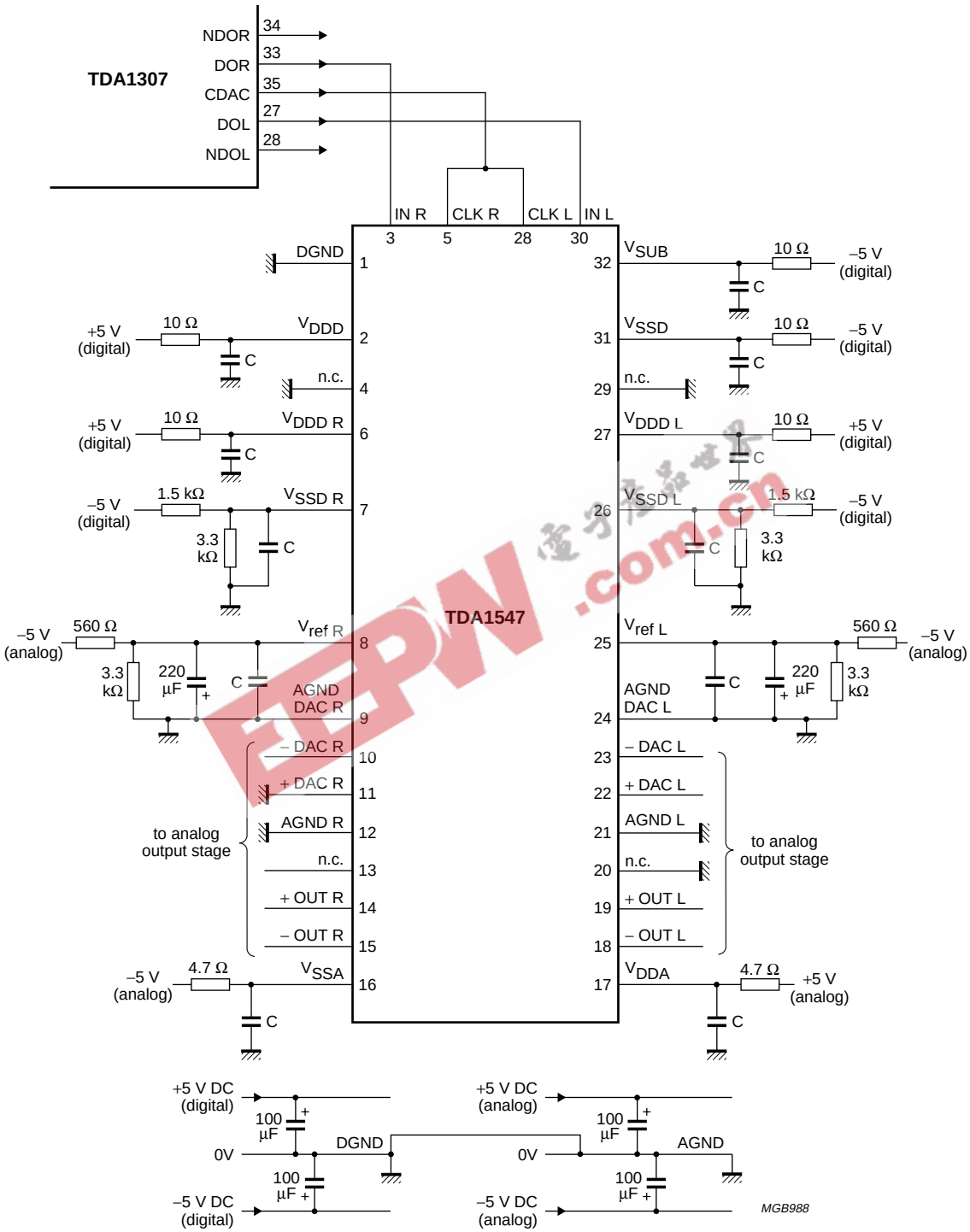
The high-quality one-bit audio data stream produced by the TDA1307 is optimumly converted to analog using the TDA1547 high-performance bitstream digital-to-analog converter. The TDA1547 takes the data outputs DOL (pin 27) and DOR (pin 33) of the TDA1307 as input, clocked by TDA1307 output CDAC (pin 35), and converts the digital data to ‘one-bit’ analog values (positive reference value and negative reference value) through a differentially configured high-speed, high-accuracy switched capacitor network.

This differential application can be further enhanced to a double-differential application, combining the assertive data outputs with the complementary data outputs NDOL (pin 28) and NDOR (pin 34) into a set of two TDA1547s, by which it is possible to achieve additional noise margin. The application of Figs 17 to 19 is an example of a differential application. A schematic diagram of the double differential mode application is illustrated in Fig.20.



C = 100 nF chip capacitor.
R = 10 kΩ chip resistor.
(1) s = slave mode switch position.
m = master mode switch position.

Fig.17 Basic connections TDA1307.



C = 100 nF chip capacitor.

Fig.18 Connections for TDA1307.

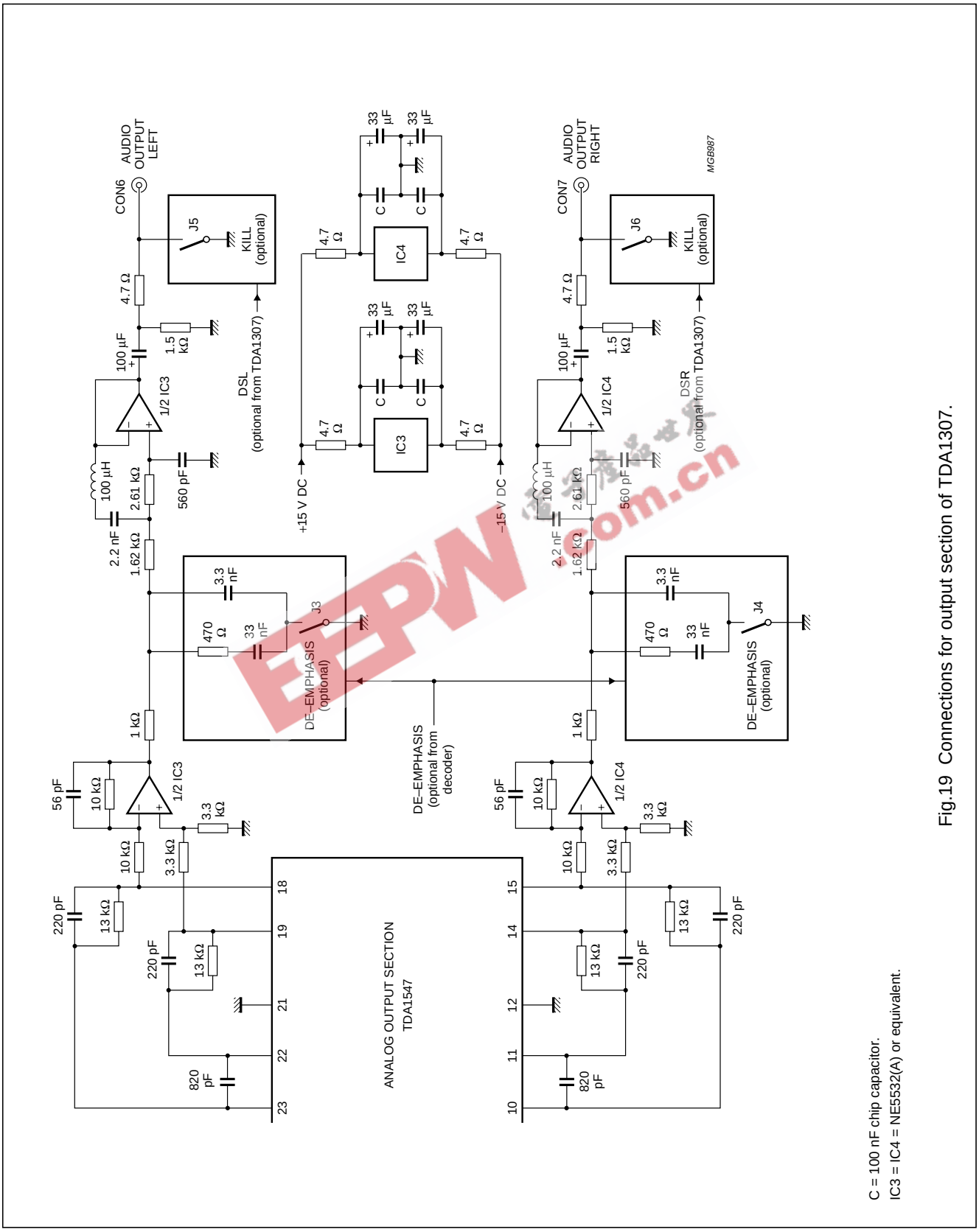


Fig.19 Connections for output section of TDA1307.

C = 100 nF chip capacitor.
IC3 = IC4 = NE5532(A) or equivalent.

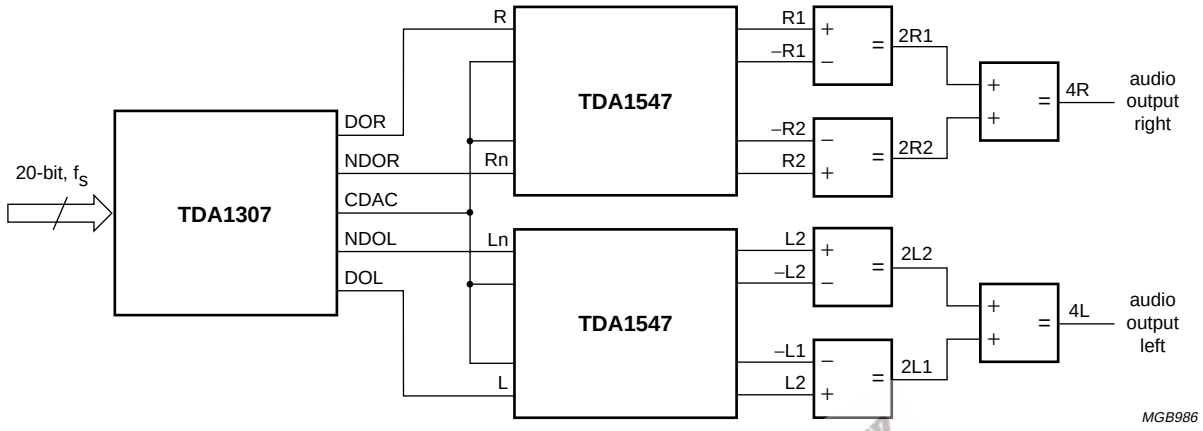
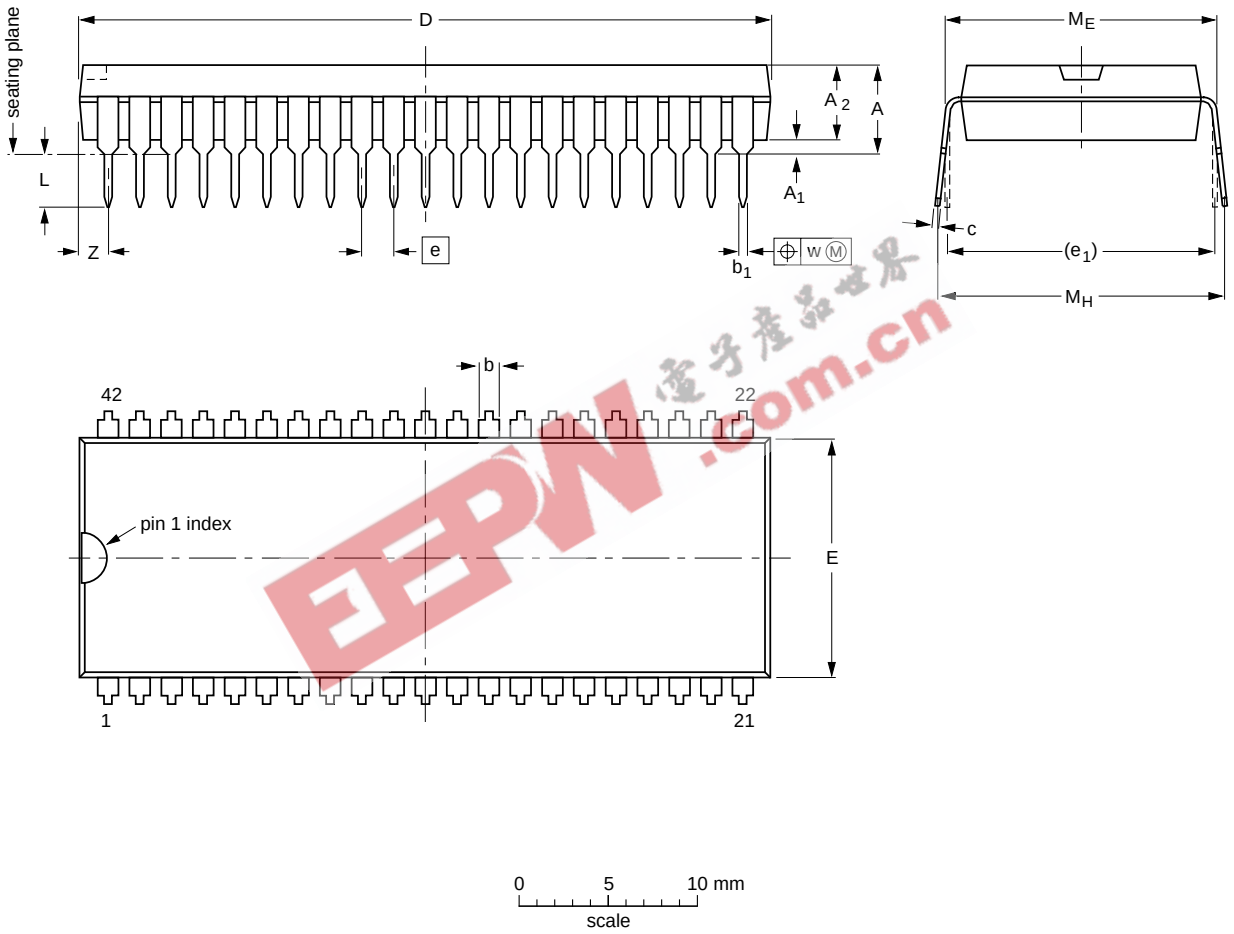


Fig.20 Schematic diagram for double differential application.

PACKAGE OUTLINE

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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