DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA3576B

SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

GENERAL DESCRIPTION

The TDA3576B is a monolithic integrated circuit for use in colour television receivers. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

Features

- Horizontal sync separator (including noise inverter) with sliding bias such that the sync pulse is always sliced between top sync level and blanking level
- Phase detector which compares the horizontal sync pulse with the oscillator voltage; this phase detector is gated
- Phase detector which compares the horizontal flyback pulse with the oscillator voltage
- Horizontal oscillator (31,25 kHz)
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals)
- Burst key pulse generator (sandcastle pulse with three levels)
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Vertical sync pulse separator
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

QUICK REFERENCE DATA

Supply voltage (pin 17)	$V_P = V_{17-10}$	typ.	12	V
Supply current (pin 17)	I_{17}	typ.	70	mA
Sync separator				
input voltage level (peak-to-peak value)	$V_{5-10(p-p)}$		0,1 to 1	V
slicing level		typ.	50	%
Phase-locked-loop				
control sensitivity sync to flyback pulse		typ.	4	kHz/μs
holding range	Δf	typ.	± 1000	Hz
catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{11-10(p-p)}$	min.	11,3	V
Vertical output pulse (peak-to-peak value)	$V_{3-10(p-p)}$	min.	10	V
Burst key output pulse (peak-to-peak value)	$V_{2-10(p-p)}$	min.	9	V
Video transmitter identification circuit output voltage (pin 1)				
sync pulse present	V_{1-10}	typ.	8,4	V
no sync pulse	V_{1-10}	max.	1	V
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE4).

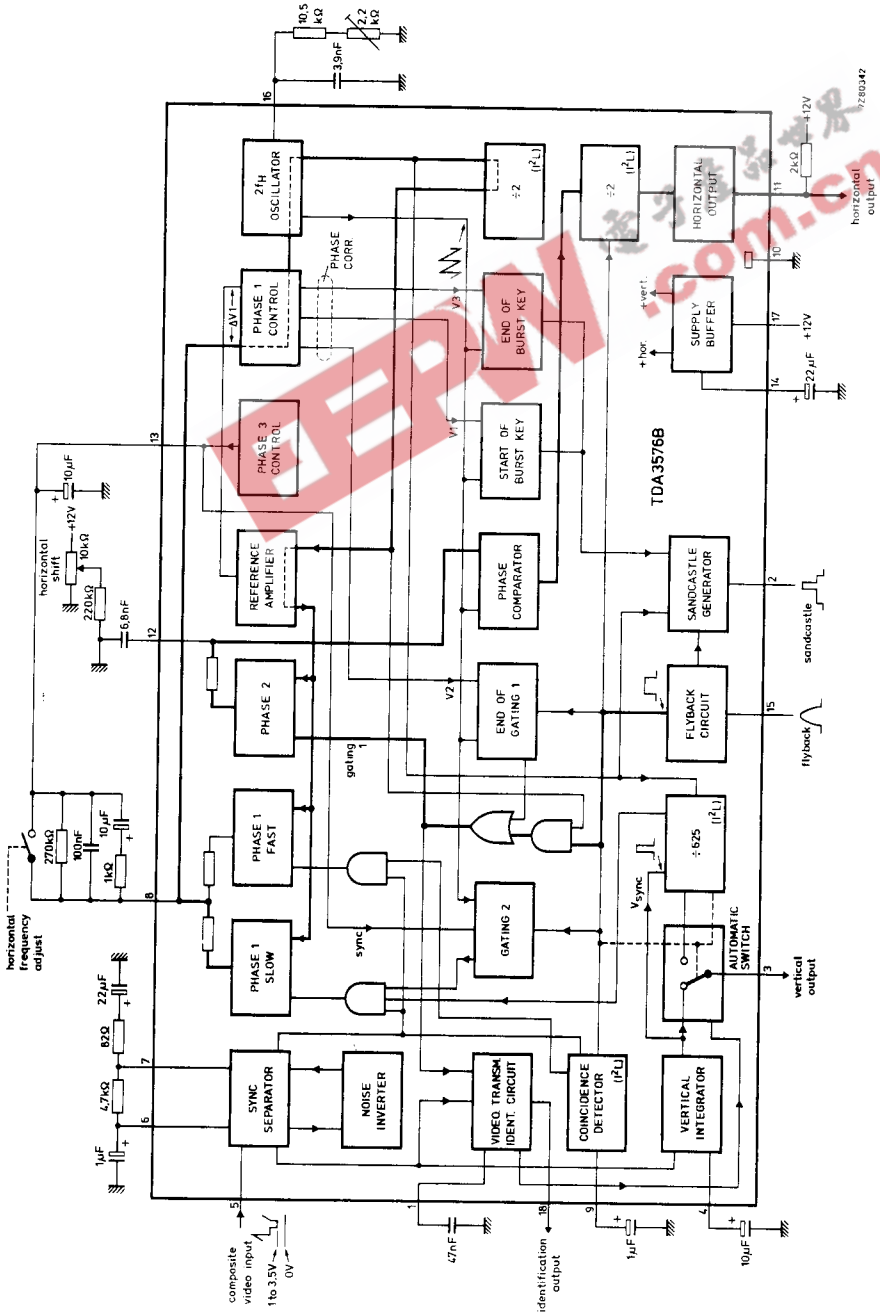

Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540 and TDA2541.

The slicing level of the sync separator is determined by the value of the resistor between pins 6 and 7. A 4,7 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 5.

The nominal top sync level at pin 5 is 3 V, and the amplitude selective noise inverter is activated at 0,7 V.

To obtain good stability the circuit contains three control loops. In the first loop the phase of the horizontal sync pulse is compared with a reference output pulse from the horizontal oscillator. In the second loop the phase of the flyback pulse is compared with the same reference output pulse. The first loop is designed for good noise immunity and the second loop has a fast time constant to compensate quickly for storage variations of the output stage. The second loop also generates a gating signal of about 5,5 μs for use in the transmitter identification circuit. The third control loop generates a second gating signal which is used in the first phase detector. The pulse width is typically 14 μs.

For a short catching time the output current of the first phase detector is not gated but is increased by 5 times during catching. This is caused by the voltage of the coincidence detector at pin 9. For VCR playback conditions the first control loop must be forced to a fast time constant, this is achieved by applying an external voltage of $\geqslant$ 2,7 V to pin 9.

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output to pin 11.

The sandcastle pulse is generated at pin 2 and has three levels. The burst key pulse is of short duration, typically 4 μs, with an amplitude of 10 V and is the highest level. The second level has a pulse duration equal to the horizontal flyback pulse with an amplitude of 4,5 V and is used for horizontal blanking. The third level, amplitude 2,5 V, is used for vertical blanking and has a pulse duration of 1,34 ms. The last pulse is internally generated by the divider circuit and is only available when a standard video input signal is received. An external vertical blanking pulse can be added to this pin via a suitable series resistor. This pulse will be automatically clamped to 2,5 V.

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite video signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The video part of the signal helps to build up a vertical sync when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fourteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fourteen pulses to be in phase to keep the system in sync. When the fifteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 3 (direct sync vertical output).

At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.

In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. A non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

FUNCTIONAL DESCRIPTION (continued)

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync.

When an external voltage between 2,7 V and 8,2 V is applied via pin 9 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical sync. A voltage level on pin 9 between 9,2 V and 12 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational. Thus when standard signals are received vertical sync pulses are generated by the divider system.

To avoid disturbance of the horizontal phase detector by the vertical sync pulse the 625 divider system generates an anti-top-flutter pulse. This pulse is applied to the phase 1 detector when a standard video signal is received. The anti-top-flutter pulse is also active for standard VCR signal conditions, voltage at pin $9 \geqslant 9{,}2$ V.

The video transmitter identification circuit detects when a sync pulse occurs during the internal 5,5 μs gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 1 being charged to 8,4 V. When no sync pulse is present the capacitor discharges to < 1 V. The voltage at pin 1 is compared with an internal d.c. voltage. The identification output at pin 18 is active when pin 1 is $\leqslant 1{,}5$ V (no video transmitter) and inactive (high impedance) when pin 1 is $> 3{,}5$ V, this information can be used for search tuning.

The vertical sync output pulse at pin 3 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information for tuning systems.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17\text{-}10}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1200	mW
Storage temperature range	T_{stg}	−55 to	+125	°C
Operating ambient temperature range	T_{amb}	−25 to	+65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{17-10} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 17)					
Supply voltage range	$V_P = V_{17-10}$	10,5	12	13,2	V
Supply current ($V_{17-10} = 12$ V)	I_{17}	50	70	85	mA
Buffer voltage ($V_{17-10} = 12$ V)	V_{14-10}	10,5	11	11,5	V
Sync separator and noise gate (pin 5)					
Top sync level (note 1)	V_{5-10}	1,0	3,0	3,5	V
Sync pulse amplitude (note 2) (peak-to-peak value)	$V_{5-10(p-p)}$	0,1	0,6	–	V
Slicing level (note 3)		35	50	65	%
Delay between sync input at pin 5 and phase detector output at pin 8*	t_d	–	0,35	–	µs
Noise gate switching level	V_{5-10}	–	0,7	1,0	V
Phase detector (pin 8)					
Control voltage	V_{8-10}	0,4	2,7	5,2	V
Control sensitivity (note 7)					
with slow time constant		–	1,0	–	V/µs
with fast time constant		–	1,0	–	V/µs
with slow time constant ▲		–	0,7	–	V/µs
Phase-locked-loop (pins 8 and 13)					
Holding range (note 4)	Δf	–	± 1000	–	Hz
Catching range (note 4)	Δf	–	± 900	–	Hz
Control sensitivity video					
with respect to oscillator**		–	2,0	–	kHz/µs
with respect to oscillator ▲		–	1,5	–	kHz/µs
with respect to burst key pulse		–	7,5	–	kHz/µs
with respect to flyback pulse		–	4	–	kHz/µs
Phase modulation due to hum on the supply line; pin 17 (note 4)		–	–	1,0	µs/V

DEVELOPMENT SAMPLE DATA

* See waveforms Fig. 2.

** Without resistor between pins 8 and 13.

▲ 270 kΩ between pins 8 and 13.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase detector (pin 12)					
Control voltage (t_d = 10 µs)	$V_{12\text{-}10}$	–	4,0	–	V
Control sensitivity		–	30	–	V/µs
Loop gain phase control *	$\Delta t_d/\Delta t_o$	–	250	–	µs/µs
Control range					
C = 6,8 nF (pin 12)*	t_d	6,5	–	24	µs
C = 100 nF (pin 12)*	t_d	2,2	–	24	µs
Phase adjustment					
control sensitivity		–	12	–	µA/µs
control range		−1,5	–	+3	µs
Horizontal oscillator (pin 16)					
Output frequency; C_{osc} = 3,9 nF; R_{osc} = 11,5 kΩ					
free running	f_o	–	31,250	–	kHz
at pin 11	f_{11}	–	15,625	–	kHz
Temperature coefficient	TC	–	$+3\times10^{4}$	–	K^{-1}
Frequency variation					
without tolerance of external components	Δf_o	–	–	±4	%
when supply voltage (pin 17) increases from 10 V to 13,2 V	Δf_o	–	0,2	–	%
at minimum supply voltage	Δf_o	–	1,5	5,0	%
Horizontal output (pin 11; note 5)					
Maximum supply voltage	$V_{17\text{-}10}$	–	–	13,2	V
Voltage at which output is started	$V_{17\text{-}10}$	6,2	6,7	7,2	V
Output voltage high level	$V_{11\text{-}10}$	–	–	13,2	V
Output voltage low level					
I_{11} = 10 mA	$V_{11\text{-}10}$	–	200	400	mV
I_{11} = 50 mA	$V_{11\text{-}10}$	–	500	700	mV
Output current at voltage low level	I_{11}	–	–	50	mA
Duration of the output pulse	t_p		see note 6		µs
Rise time of the output pulse	t_r	0,05	–	0,3	µs
Protection voltage (pin 11)		13	14,5	15,5	V

* See waveforms Fig. 2.

DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 2)*					
Output voltage during burst key pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	9	10	–	V
Duration of upper level of output pulse	t_p	3,6	4,0	4,4	μs
Amplitude of second level of output pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	4,0	4,5	5,0	V
Duration of second level of output pulse	t_p		flyback pulse		μs
Amplitude of lower level of output pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	2,0	2,5	3,0	V
Duration of lower level of output pulse during standard signals (note 8)	t_p	–	1,34**	–	ms
Amplitude at zero level of output pulse	$V_{2\text{-}10}$	–	–	1	V
Delay between start of the sync pulse at pin 5 and the rising edge of the burst key pulse at pin 2	t_b	4,6	4,9	5,2	μs
Phase detector (pin 13)					
Output voltage	$V_{13\text{-}10}$	–	2,8	–	V
Charge current	I_{13}	–	0,9	–	mA
Discharge current	I_{13}	–	0,9	–	mA
Vertical sync pulse (pin 3)					
Output voltage (peak-to-peak value)	$V_{3\text{-}10(p\text{-}p)}$	10	–	–	V
Output current	I_3	–	–	5	mA
Duration of output pulse during indirect synchronization	t_p	–	190	–	μs
Phase variation between first vertical sync pulse and start of output pulse in divider mode		–	–	±2,5	lines
Coincidence detector (pin 9)					
Switching level (note 7)	$V_{9\text{-}10}$	2,1	2,4	2,7	V
Voltage					
normal conditions (in-sync)	$V_{9\text{-}10}$	–	1,3	–	V
out-of-sync	$V_{9\text{-}10}$	–	2,7	–	V
during noise	$V_{9\text{-}10}$	–	2,1	–	V

* See waveforms Fig. 2.
** 21 lines.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Switching levels for VCR (pin 9)					
Fast time constant for phase 1					
switching level	$V_{9\text{-}10}$	2,1	2,4	2,7	V
input current	I_9	1,0	–	2,0	mA
Vertical sync output indirect/direct with divider system active					
switching level*	$V_{9\text{-}10}$	8,2	8,7	9,2	V
input current	I_9	3,0	–	4,0	mA
Flyback input pulse (pin 15)					
Switching level	$V_{15\text{-}10}$	–	0,85	1,0	V
Input pulse (peak-to-peak value)	$V_{15\text{-}10(p\text{-}p)}$	–	–	12	V
Input resistance	$R_{15\text{-}10}$	–	3,5	–	kΩ
Input current	I_{15}	0,2	–	3,0	mA
Delay between the start of the sync pulse at the video input and the leading edge of the flyback pulse	t_d	–	0,5	–	μs
Video transmitter identification circuit					
Pin 1					
Sync pulse present					
charge current	I_1	–	+100	–	μA
output voltage	$V_{1\text{-}10}$	–	8,4	–	V
No sync pulse					
discharge current	I_1	–	−100	–	μA
output voltage	$V_{1\text{-}10}$	–	–	1	V
Switching level output stage					
pin 18 active when:	$V_{1\text{-}10}$	1,7	2,0	2,2	V
pin 18 inactive when:	$V_{1\text{-}10}$	3,0	3,5	4,0	V
Pin 18 (note 9)					
Sync pulse present					
output current inactive	I_{18}	–	–	1	μA
No sync pulse					
minimum available output current active ($V_{18\text{-}10}$ = 7 V)	I_{18}	4,0	–	–	mA
maximum allowed output current	I_{18}	–	–	10	mA
output voltage active (I_9 = 1 mA)	$V_{9\text{-}13}$	10,5	11,0	$V_{17\text{-}10}$	V

* The maximum allowed voltage at pin 9 is V_P (pin 17).

Notes to characteristics

1. The video signal at pin 5 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 6 and pin 7. The 50% figure is obtained with a 4,7 kΩ resistor. The slicing level P is determined by the formula:

   $P = \frac{R_S}{4880 + R_S} \times 100\%$; where R_S is the resistor between pins 6 and 7.
4. Values of external circuitry as shown in Fig. 1; the voltage in this ratio has a peak-to-peak value.
5. The horizontal output configuration is an open collector with internal high voltage protection during the off-state of the output transistor.
6. The horizontal output pulse width is determined by the horizontal flyback pulse. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback. Thus t_p = switch-off delay of horizontal output stage plus flyback time.
7. When the voltage level at pin 9 is $< 2,1$ V, phase detector 1 (pin 8) is gated. When the level is $> 2,7$ V, the dynamical control sensitivity of the phase detector is raised such that the output current is increased by five times the original amount and the phase detector is not gated.
8. An external vertical blanking pulse can be applied to pin 2 via a series resistor. The required input current is 2 mA. This external pulse is clamped to 2,5 V by internal circuitry.
9. The video transmitter identification output stage at pin 18 consists of a p-n-p current source with an n-p-n emitter-follower.

DEVELOPMENT SAMPLE DATA

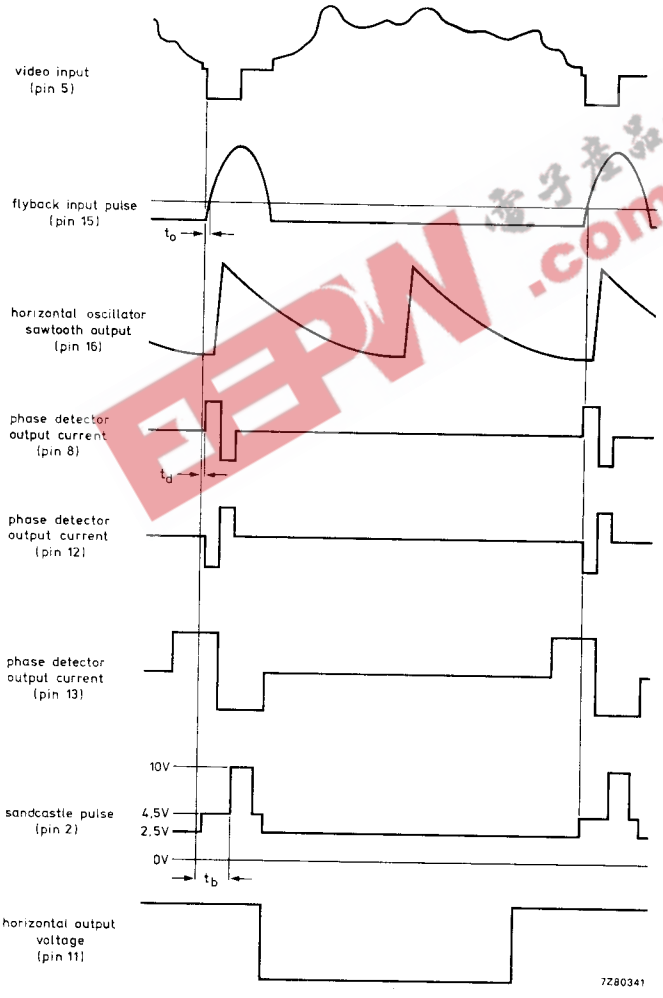

Fig. 2 Phase relationship between the input and output signals of the TDA3576B.

APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

1. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of < 1 V when no sync pulse is detected.

2. Sandcastle output pulse

This output has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level, for the horizontal blanking, is typically 4,5 V with a pulse duration equal to the horizontal flyback pulse. For the third level an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by an internal clamping circuit. The input current is typically 2 mA.

3. Vertical output pulse

This pulse is obtained from the 625 divider circuit when standard input signals are received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected. Both pulses have good stability and accuracy and are used to trigger the vertical oscillator.

4. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor of 10 μF is required for biasing the vertical sync separator, this provides the vertical sync output pulse with a delay of 37 μs. This value can be changed by an external resistor. A resistor of 470 kΩ between pin 3 and +12 V gives a delay of 45 μs.

5. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,1 to 1 V which provides good sync separation down to pulses with an amplitude of 100 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level < 1 V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V.

6. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 7.

7. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 22 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 4,7 kΩ resistor connected between pins 6 and 7 results in a slicing level of 50%.

8. Horizontal phase detector output and control oscillator input

The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 8 and 13 to limit the free running frequency drift.

The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out-of-sync. The result is a large catching range, and the phase detector not gated. The output current is low when the oscillator is synchronized and the phase detector is gated; this provides good noise immunity.

APPLICATION INFORMATION (continued)

9. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. The following output voltages can occur:

- when in-sync 1,3 V
- when out-of-sync 2,7 V
- during noise at the input 2,1 V

There are two switching levels at pin 9. At the first switching level when the output voltage is $< 2{,}1$ V, the phase detector output is low and the gating of the phase detector is switched on. When the output voltage is $> 2{,}7$ V, the output current of the phase detector is high and the gating of the phase detector is switched off. The result is a large catching range and a high dynamic steepness of the PLL. At the second switching level when the output voltage is $> 9{,}2$ V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

10. Negative supply (ground)

11. Horizontal sync pulse output

This is an open collector output. The collector resistor mus be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback.

12. Control voltage second loop

This voltage controls the output pulse at pin 11 (positive-going edge). The capacitor connected to this pin must have a minimum value of 6,8 nF. A higher value decreases the dynamic-loop gain in the second control loop. When a high dynamic-loop gain is not required a capacitor value of 100 nF is recommended. Horizontal shift is possible by applying an external current to pin 12.

13. Reference voltage control loops

The reference voltage must be decoupled by a capacitor of 10 μF.

14. Decoupling internal power supply

The IC has two power terminals. The main terminal (pin 17) supplies the output stages, the sync separator and the divider circuit. The specially decoupled terminal (pin 14) supplies the horizontal oscillator. The decoupling capacitor should be 22 μF.

15. Flyback input pulse

This pulse is required for the second phase control loop and for generating the horizontal blanking pulse in the sandcastle output. The input current must be at least 0,2 mA and not exceed 3 mA.

16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors. The oscillator can be adjusted when pins 8 and 13 are short circuited (see Fig. 3).

17. Positive supply

The supply voltage may vary between 10,5 and 13,2 V. The current-draw is typ. 70 mA and the range is 50 to 85 mA.

18. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 1 is > 4 V (video transmitter detected). The output will be active high when the level at pin 1 is $< 1{,}7$ V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

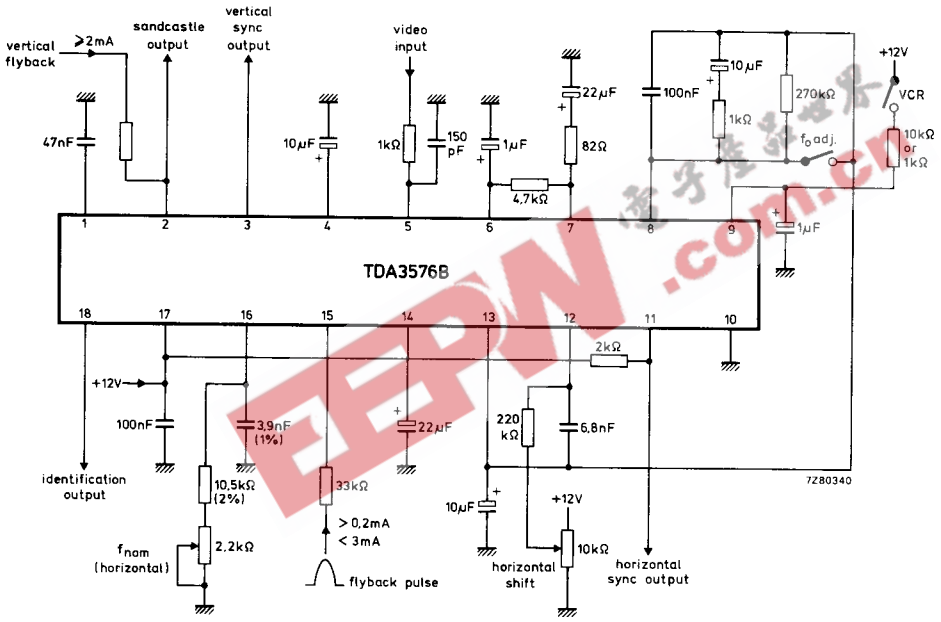

Fig. 3 Application circuit diagram.