

Multistandard VIF Amplifier and PLL Demodulator

Application

Monolithic integrated circuit for vision IF signal processing in multistandard TV and VTR sets.

Description

This multistandard video IF processing circuit with PLL picture carrier regeneration gives a high performance of linear video demodulation.

The IF signal is internally fed via a 3-stage controlled wideband amplifier to the video demodulator and the phase detector. The phase detector compares the phase of IF signal (0°) with the output signal of the VCO (90°) and sets the VCO frequency accordingly. A lock detector switches the PLL loop filter according to the state of the PLL (locked-PLL slow, unlocked-PLL fast).

A second output of the VCO (0°) provides the reference carrier for the video demodulator. The polarity of the demodulator can be inverted by the standard switch (Pin 10), so that negative or positive modulated IF signals are always available with the same polarity at the demodulator output. The demodulated video signal is filtered,

amplified and fed via an interference limiter to the video output (Pin 6).

The standard switch also determines the clamp level of the video amplifier and the required IF-AGC mode. In the standard B/G mode the sync peak value is the criterion for a fast charge and discharge. In the standard L mode on the other hand, fast AGC action is achieved by charging at peak white level and discharging by the averaged video signal (time constant on Pin 7). The response level for discharge has a hysteresis. In the D2MAC mode a similar function is applied to achieve the AGC, but with different threshold levels.

An overload detector prevents the PLL becoming unlocked by large IF input signals.

To achieve a delayed tuner-AGC action, the current output (Pin 3) can be adjusted with a resistor at Pin 2.

Features

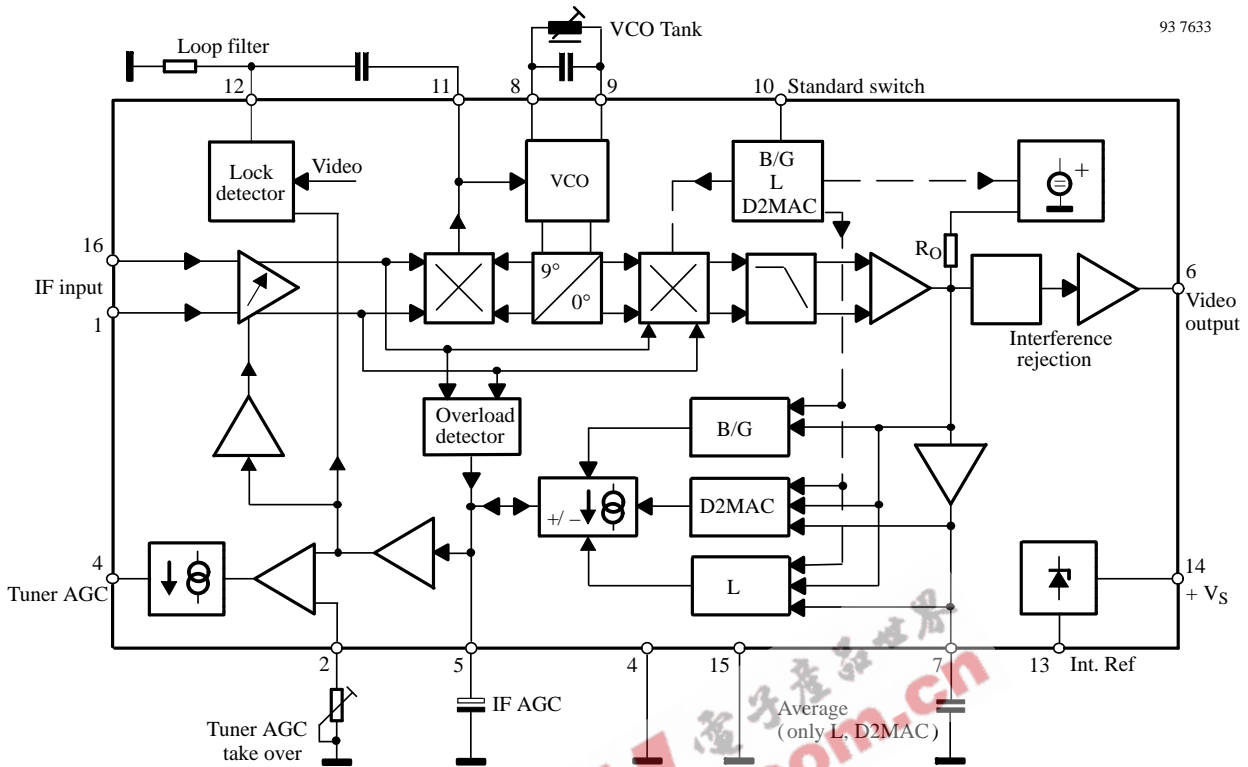
- Suitable for standard B/G, L and D2MAC, processes negative and positive modulated IF-signals with equal polarity of the output signal
- High performance video demodulator with PLL picture carrier regeneration
- Extended video bandwidth (12 MHz) for the demodulation of amplitude modulated MAC-signals
- Standard B/G: AGC acting on the sync peak pulse
- Standard L: fast AGC acting on peak white level with average value controlled capacitor discharge and reference hysteresis
- D2MAC: fast AGC acting on peak level with controlled capacitor discharge
- Output for delayed tuner-AGC, take over point adjustable
- High input sensitivity
- Ultra white and ultra black limiting
- Supply voltage range 6.8 to 13 V
- Low power consumption
- ESD protection

Package Options

Case: 16-pin DIL plastic

Block Diagram

93 7633



Pin Description

| Pin | Symbol | Function |
|-------|--------|--|
| 1, 16 | | IF input |
| 2 | | Tuner AGC adjustment (turn over point) |
| 3 | | Delayed tuner AGC current |
| 4, 15 | | Ground |
| 5 | | IF AGC time constant |
| 6 | | Video output |
| 7 | | Video averaging for standard L and D2MAC |

| Pin | Symbol | Function |
|------|--------|--------------------------|
| 8, 9 | | VCO circuit |
| 10 | | Standard switch |
| 11 | | PLL loop filter |
| 12 | | PLL time constant switch |
| 13 | | Reference voltage |
| 14 | | Supply voltage |

Absolute Maximum Ratings

Reference point Pin 4, unless otherwise specified

| Parameters | Symbol | Value | Unit |
|--------------------------------------|-----------|-------------|------|
| Supply voltage Pin 14 | V_s | 6.8 to 13.0 | V |
| Supply current Pin 14 | I_s | 55 | mA |
| Output current Pin 6 | I_{out} | 5.0 | mA |
| Maximum power dissipation | P | 720 | mW |
| Junction temperature | T_j | +125 | °C |
| Ambient temperature during operation | T_{amb} | -25 to +85 | °C |
| Storage temperature | T_{stg} | -25 to +125 | °C |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|------------|-------|------|
| Junction ambient (when soldered to PCB) | R_{thJA} | 60 | K/W |

External Voltage

| Pin | Voltage Range *) |
|------|---|
| 1-16 | $0 \leq V_{pin} \leq \min(V_s, 8\text{ V})$ |
| 2 | $0 \leq V_{pin} \leq V_s$ |
| 3 | $0 \leq V_{pin} \leq \min(V_s, 10\text{ V})$ |
| 5 | $0 \leq V_{pin} \leq \min(V_s, 10\text{ V})$ |
| 6 | $0 \leq V_{pin} \leq 6\text{ V}$ |
| 7 | $0 \leq V_{pin} \leq \min(V_s, 8\text{ V})$ |
| 8-9 | $0 \leq V_{pin} \leq V_s$ |
| 10 | $0 \leq V_{pin} \leq V_s$ |
| 11 | $0 \leq V_{pin} \leq \min(V_s, 7.5\text{ V})$ |
| 12 | $0 \leq V_{pin} \leq V_s$ |
| 13 | $0 \leq V_{pin} \leq V_s$ |
| 14 | $6.8\text{ V} \leq V_{pin} \leq V_s$ |

*) $\min(V_s, xV)$: the lesser of the two values is the lower limit.

Electrical Characteristics

$V_s = 8\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point Pin 4, unless otherwise specified

| Parameters | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|--|-------------------------|------|-----------|------|----------------------------|
| DC-supply Pin 14 | | | | | | |
| Supply voltage | | V_s | 6.8 | 8.0 | 13.0 | V |
| Supply current | | I_s | | 45 | 55 | mA |
| IF-amplifier Pins 1–16 | | | | | | |
| Input sensitivity | Sync peak value, B/G | V_{in} | | 80 | 120 | μV_{eff} |
| Input impedance | | R_{in} | | 1.2 | | k Ω |
| Input capacitance | | C_{in} | | 2 | | pF |
| IF-AGC Pins 5 and 7 | | | | | | |
| IF gain control range | | G_v | 60 | 66 | | dB |
| Response time, standard L | See note 1 | t_{AGC} | | | 10 | μsec |
| AGC capacitor | | C_5 | | 4.7 | | μF |
| Average capacitor | | C_7 | | 68 | | nF |
| Tuner-AGC Pins 2 and 3 | | | | | | |
| Available tuner-AGC current | | I_3 | | 4 | | mA |
| Automatic turn over point | | $G_{v,\text{tun}}$ | | 65 | | dB |
| PLL Pins 8–9, 11, 12 see note 2 | | | | | | |
| PLL capture range | | Δf_{cap} | | ± 1.5 | | MHz |
| VCO-tuning range | | Δf_{vco} | | 3.0 | | MHz |
| VCO-tuning sensitivity | | $\Delta f / \Delta u$ | 3.0 | 4.5 | | kHz/mV |
| Video demodulator output Pin 6 see note 3 | | | | | | |
| Composite video output signal – standard B/G | Note 4 | V_{out} | 1.8 | 2.0 | 2.2 | V_{pp} |
| Video output signal standard L | Note 5 | V_{out} | 1.2 | 1.4 | 1.6 | V_{pp} |
| Difference of the video signals | Standard B/G and L | ΔV_{out} | | | 10 | % |
| Ultra white level, standard B/G | Zero carrier level | V_6 | | 4.2 | | V |
| Ultra black level, stand. L | Zero carrier level | V_6 | | 1.9 | | V |
| Supply voltage influence on the ultra black level (B/G) | | $\Delta V/V$ | | 0.5 | | %/V |
| Supply voltage influence on the ultra black level (L) | | $\Delta V/V$ | | 0.5 | | %/V |
| Video bandwidth (–3 dB) | | B | 12 | | | MHz |
| Video frequency response over the AGC range | | ΔB | | | 2.0 | dB |
| Differential gain error | | ΔG | | 3 | | % |
| Differential phase error | | $\Delta \Phi$ | | 3 | | deg |
| Video demodulator output Pin 6 | | | | | | |
| Sound chroma beat (1.07 MHz intermodulation) related to demodulated auxiliary colour carrier) | Picture carrier = 0 dB Colour carrier = –6 dB Sound carrier = –24 dB | a_{IM} | 52 | | | dB |

| Parameters | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------------|---------------------------------|------|------|-------|------|
| IF residual voltage f = 38.9 MHz f = 77.8 MHz | | V_{res1} | | 2 | | mV |
| | | V_{res2} | | 5 | | mV |
| Upsetting factor of sync pulse in the AGC range | | ΔV_{sync} V_{sync} | | 3 | | % |
| Tilt of half picture between black and white | Standard L | | | 5 | 10 | % |
| Ultra black limiting threshold | Below sync level | ΔV_{lim1} | | 250 | | mV |
| Ultra white limiting threshold | Above ultra white level | ΔV_{lim2} | | 500 | | mV |
| Standard switch Pin 10 | | | | | | |
| Control voltage B/G | Note 6 | V_{sw1} | 2.5 | | 4.0 | V |
| Control voltage L | | V_{sw2} | 0 | | 1.5 | V |
| Control voltage D2MAC | | V_{sw3} | 5.0 | | V_s | V |

Notes

1. A peak white value for at least 10 μ s must be transmitted for each complete frame
2. Loop filter: $R1 = 500 \Omega - 1 k$, $C1 = 0.47 \mu F$
Capacitor VCO circuit: $C_{VCO} = 27 - 47 pF$
3. Pin 6 unloaded
4. Residual carrier: 10% carrier amplitude
5. Blanking level: 30% carrier amplitude
6. Without control voltage at Pin 10 – standard B/G is automatically selected

Alignment of the VCO

1. Apply 4.5 V to Pin 5, to disable the broadband amplifier.
2. Measure the dc-voltage at Pin 11 (phase detector).
3. Apply a 38.9 MHz unmodulated carrier signal to the IF input (Pins 1–16); adjust the input level so that the AGC voltage at Pin 5 is between 2.0 V and 2.5 V.
4. Adjust the VCO circuit until at Pin 11 is the same dc-voltage as measured in step 2.

Pin Related Internal Circuits

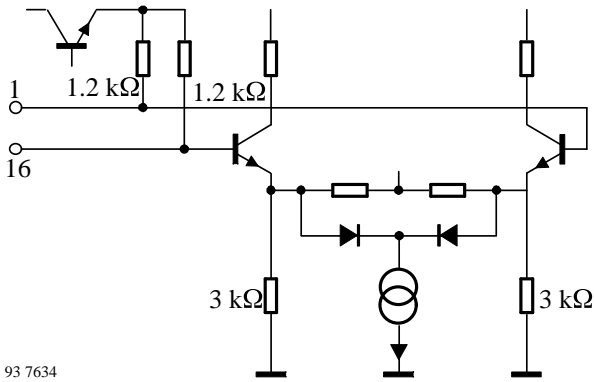


Figure 1. Pin 1 – 16

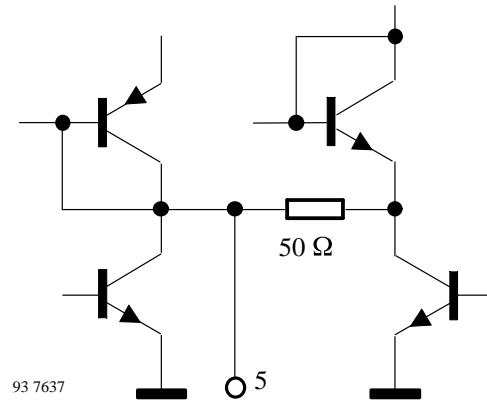


Figure 4. Pin 5

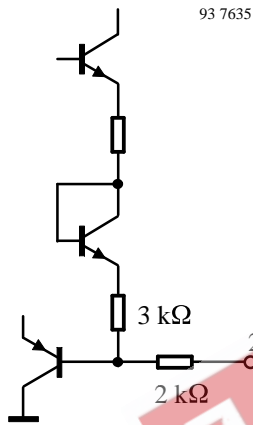


Figure 2. Pin 2

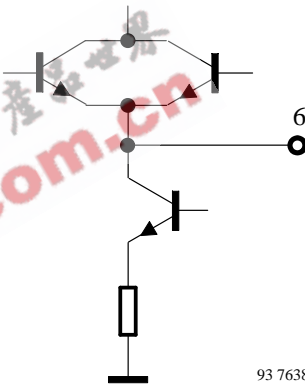


Figure 5. Pin 6

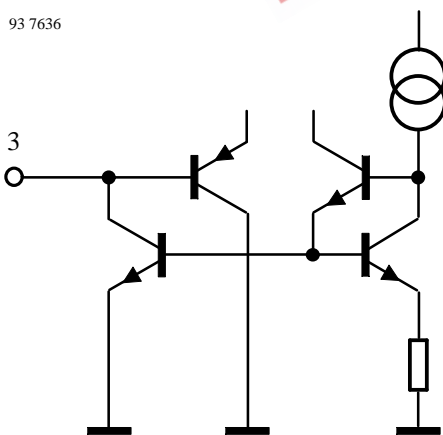


Figure 3. Pin 3

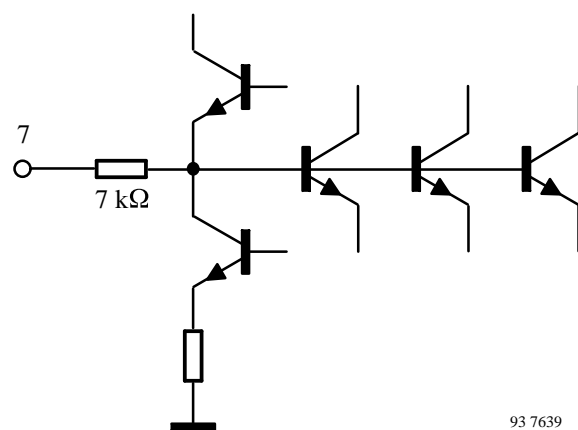


Figure 6. Pin 7

Pin Related Internal Circuits (Continued)

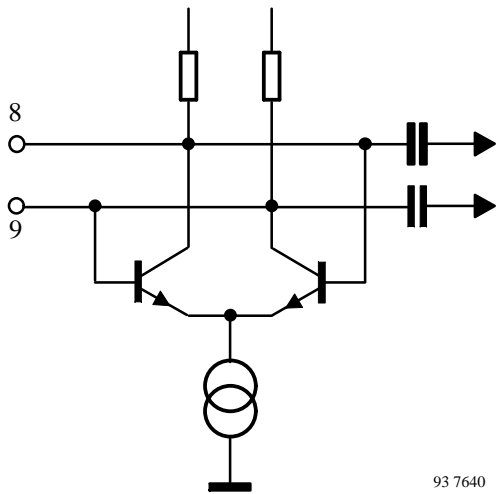


Figure 7. Pin 8 - 9

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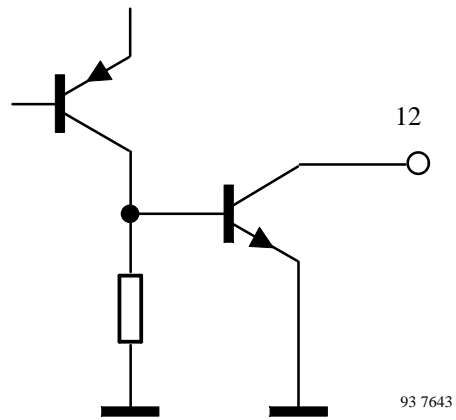


Figure 10. Pin 12

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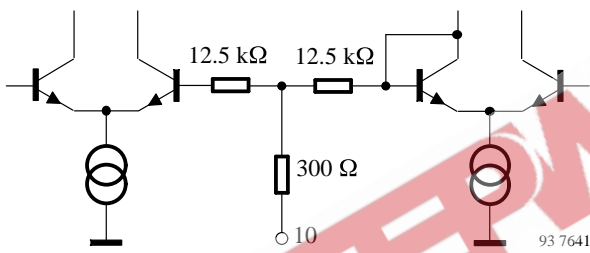


Figure 8. Pin 10

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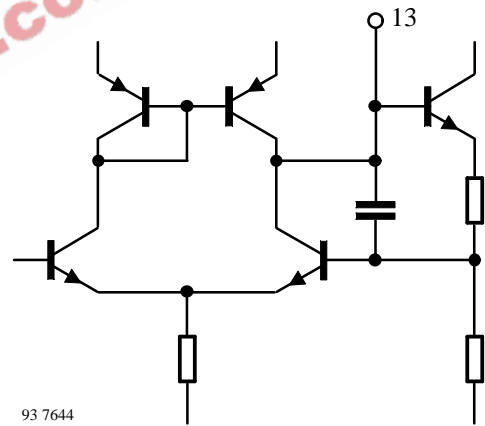


Figure 11. Pin 13

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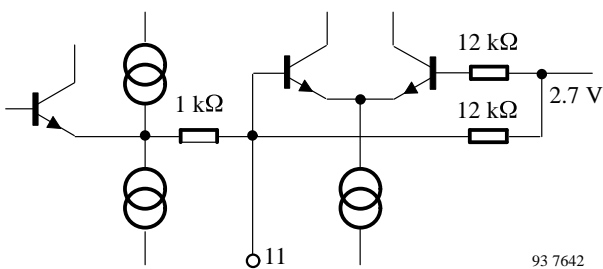


Figure 9. Pin 11

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IF-AGC, Switching Thresholds

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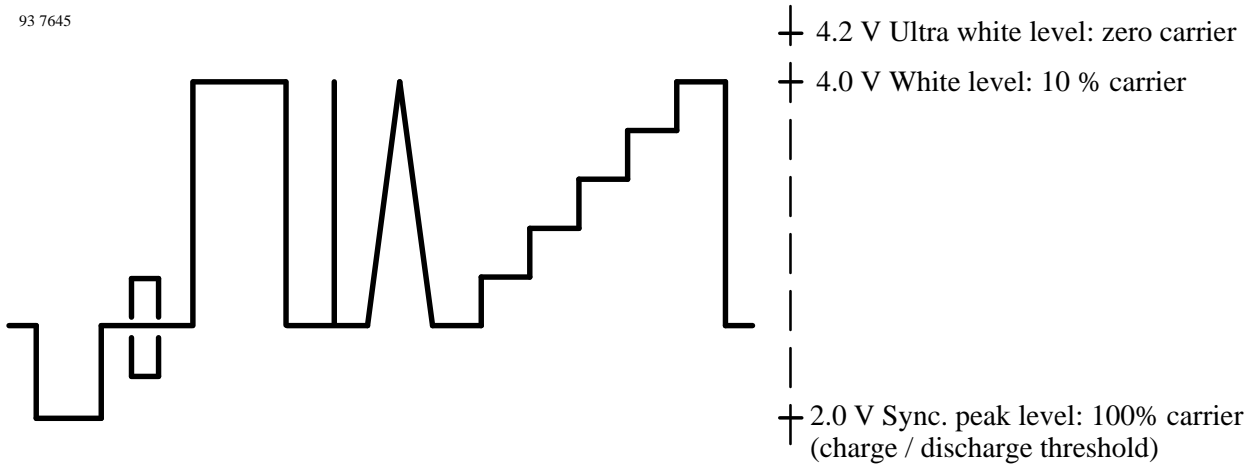


Figure 12. B/G-standard (neg. modulated)

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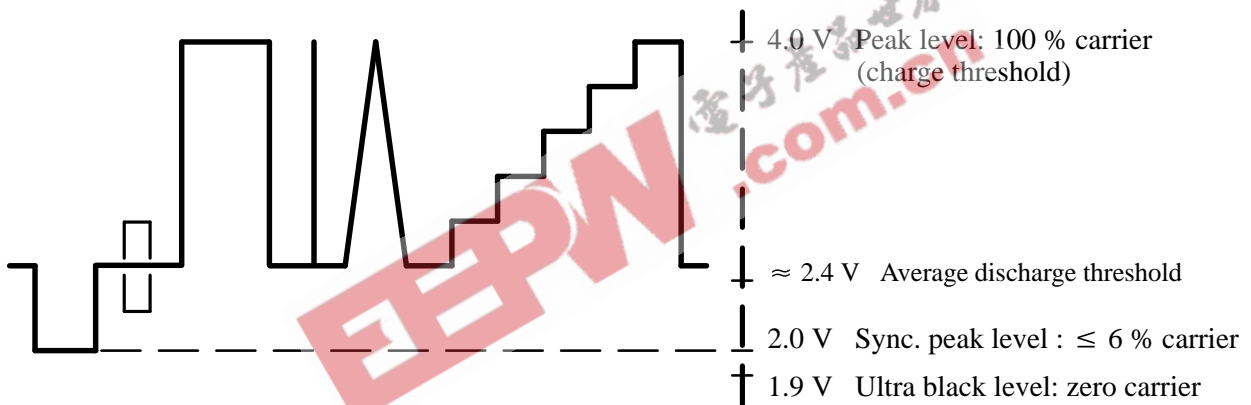


Figure 13. L-standard (pos. modulated)

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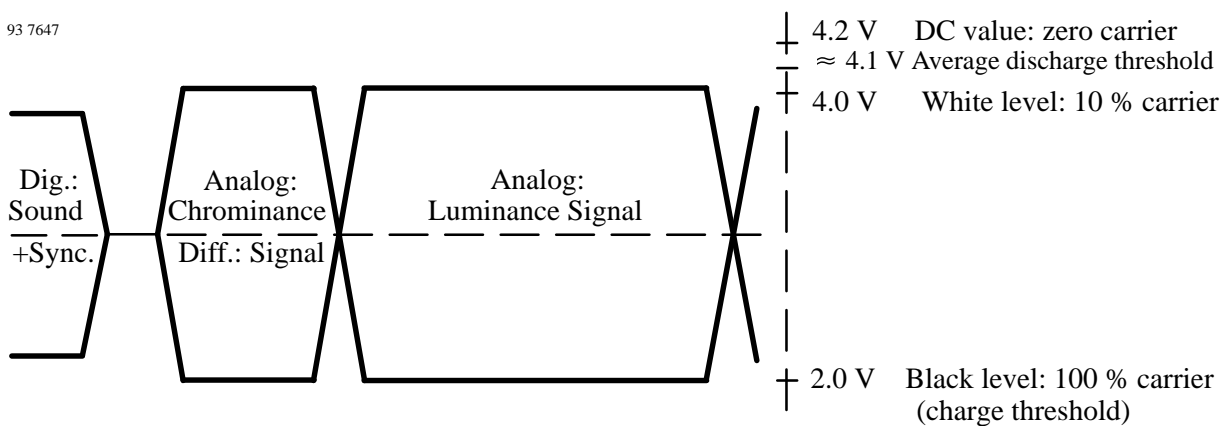
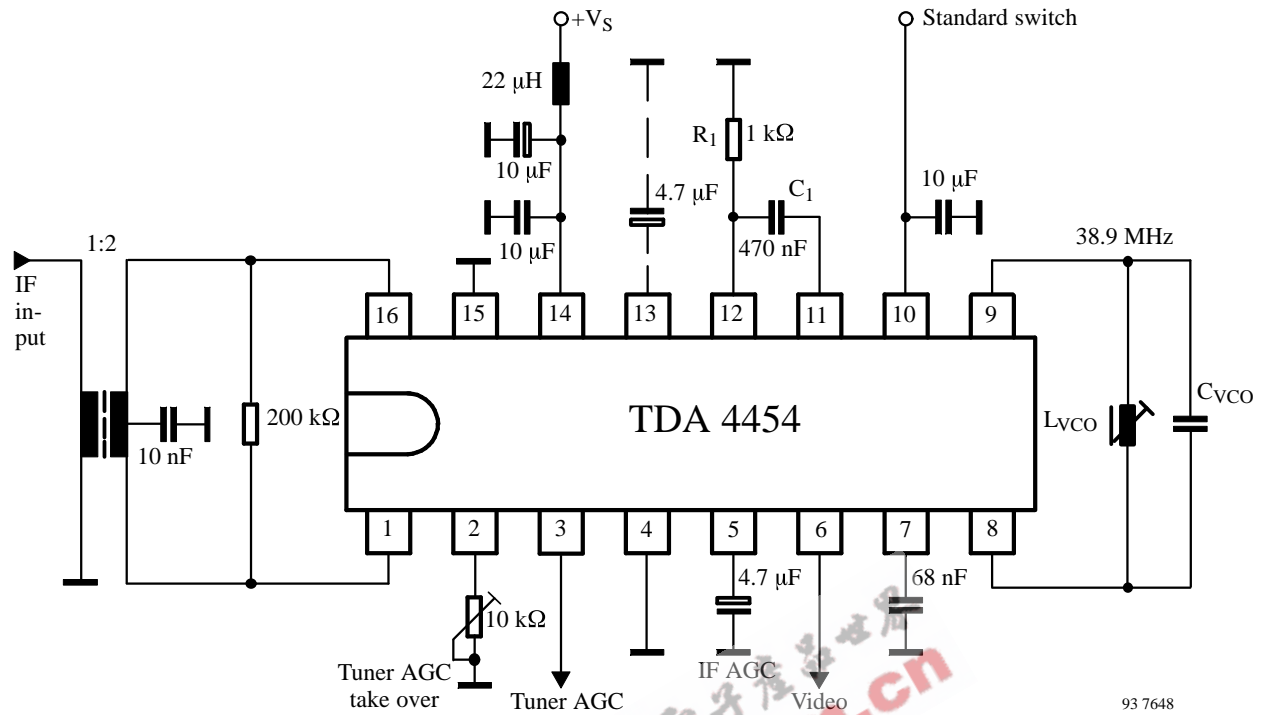
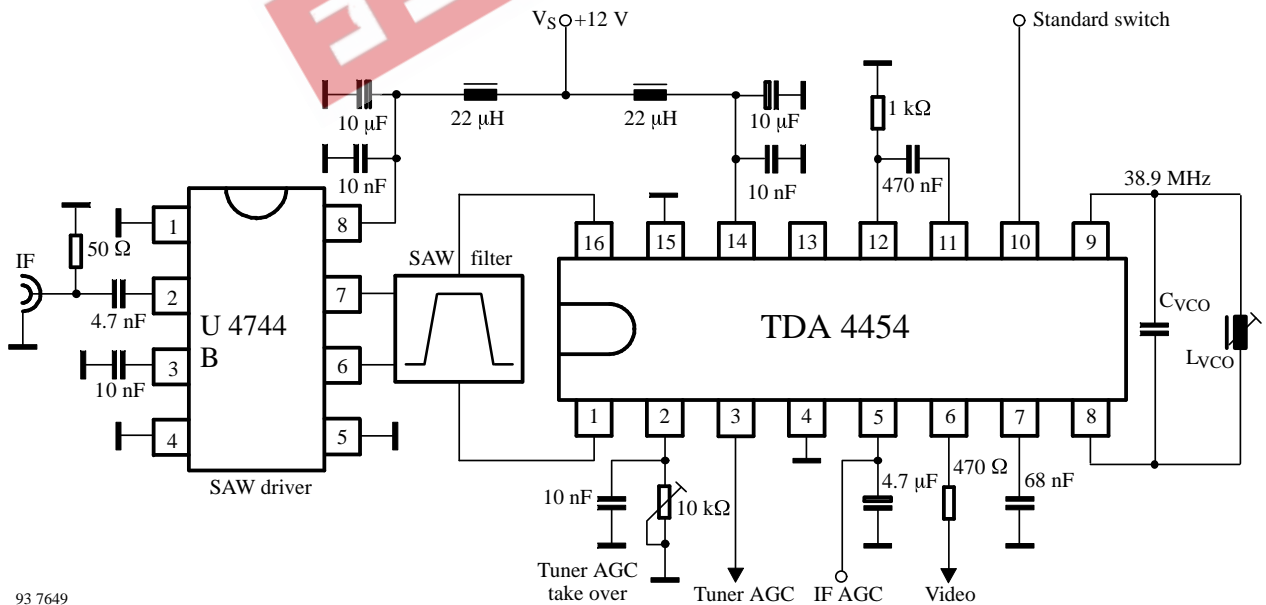


Figure 14. D2MAC-standard (neg. modulated)

Test Circuit



Application Circuit



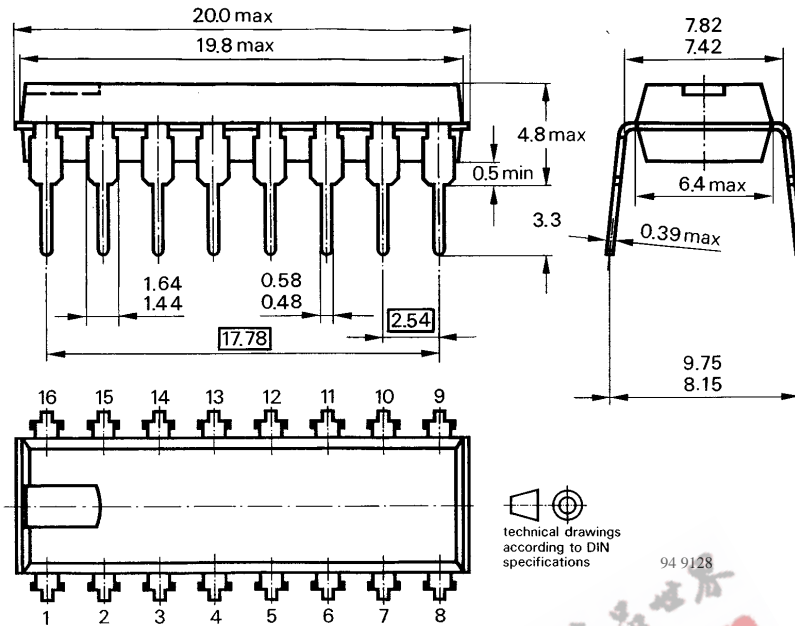
TDA4454

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Dimensions in mm

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