DATA SHEET

TDA3601Q
TDA3601AQ
Multiple output voltage regulators

Product specification
Supersedes data of September 1994
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (low current pin)
- V_{P2} supply pin (high current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 μs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulator 1
- Foldback current limit protection (regulators 2 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
$I1_{tot}$	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_c	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes

1. Load dump, during 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V; V_{P2} = R4-sel = R5-sel = 0; I_{R1} = 0.

BLOCK DIAGRAM

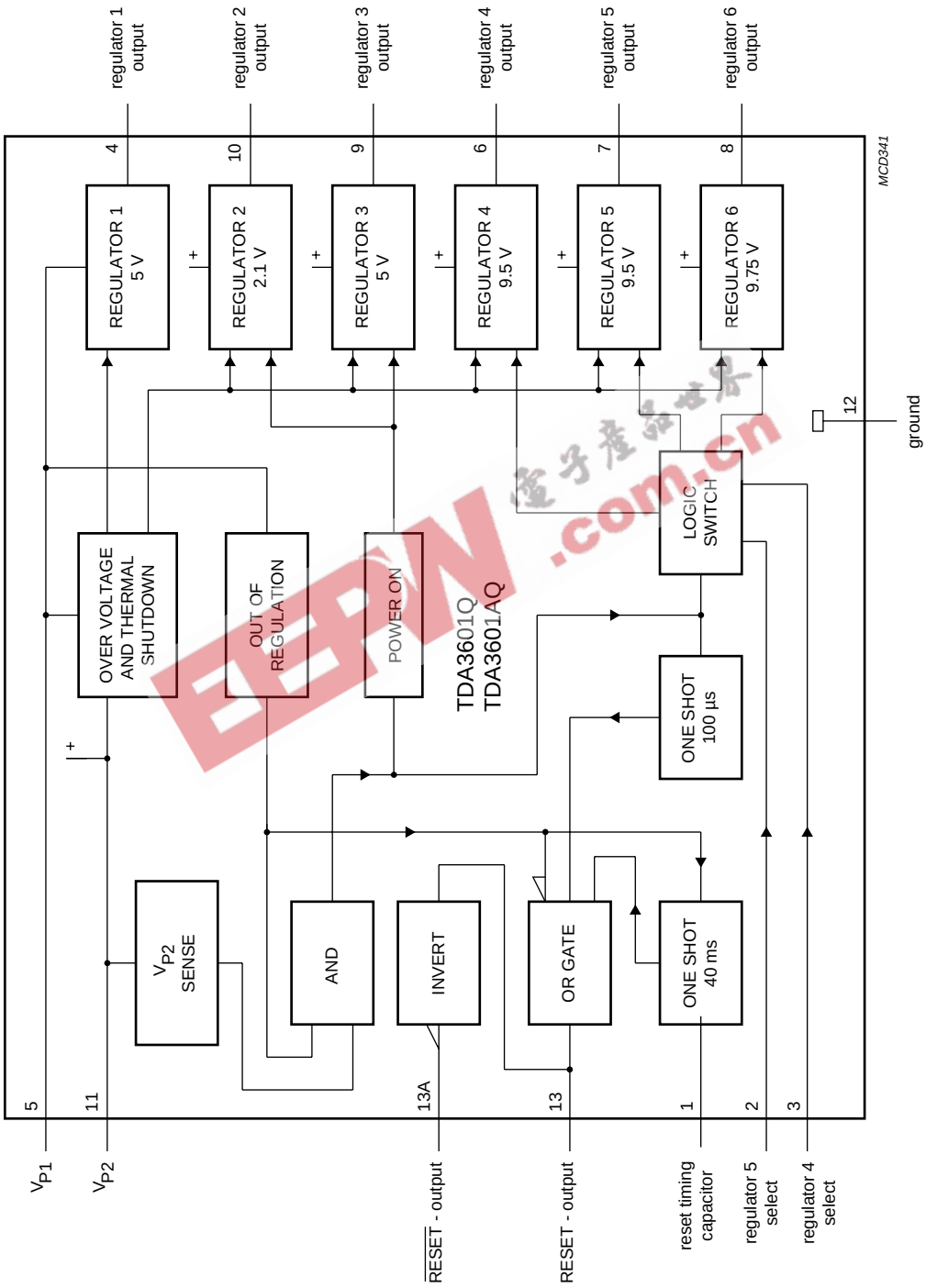


Fig.1 Block diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3601Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6
TDA3601AQ			

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.4 V)
V_{P2}	11	supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

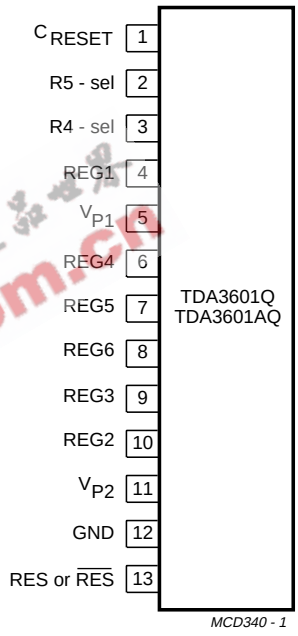


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3601Q is a multiple output voltage regulator with six fixed voltage regulators. Three, logical switch controlled, voltage regulators (numbers 4 to 6) are available, and one non-switchable voltage regulator (number 1). In addition, there are two further regulators (numbers 2 and 3), which are controlled by supply voltages V_{P1} and V_{P2} (Schmitt trigger).

Regulator 1 is not affected by load dump or thermal shutdown. Regulators 2 to 6 are supplied by V_{P2}; they can therefore be switched of by an ignition switch, for example. An internal bandgap voltage reference, which provides a reference voltage for each independent regulator, is supplied by V_{P1}. This supply voltage V_{P1} also supplies regulator 1.

A V_{P2} sense circuit outputs a logical high when the V_{P2} voltage rises through V_{thr}, which remains high until the V_{P2} voltage falls through V_{thf}.

The supply voltage V_{P1} is sensed by an out-of-regulation Schmitt trigger.

When this voltage drops below 5.95 V typical, the reset output is disabled, to prevent a microprocessor being disturbed by a too-low supply voltage. An out-of-regulation condition is indicated by a logical low and an in-regulation condition indicated by a logical high.

The 'Power On' switch low will disable regulator 2 and 3 outputs. In addition, the logic switch will be disabled, so that regulators 4 to 6 are switched off. When both V_{P2}-sense and out-of-regulation are high, the 'Power On' will be high, so that the logic multiplexer and regulators 2 and 3 are enabled. Regulators 4 to 6 can now be selected by the multiplexer.

Re-triggerable one-shot circuits produce a RESET (open collector output) when V_{P1} is available (40 ms delay signal), or when both V_{P1} and V_{P2} are available (100 µs pulse). RESET will be held in a constant high state when the supply voltage V_{P1} is less than 5.5 V (5.95 V typical).

The TDA3601 has a RESET output, but the TDA3601A has an inverted RESET output ($\overline{\text{RESET}}$).

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; $t_r > 2.5$ ms; note 1	–	50	V
P_{tot}	total power dissipation	$T_{case} < 30$ °C	–	15	W
T_{stg}	storage temperature range	non-operating	–55	150	°C
T_{vj}	virtual junction temperature	operating	–40	150	°C
V_{pr}	reverse polarity	non-operating	–	6	V

Note

1. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	8	K/W
$R_{th\ j\text{-}amb}$	thermal resistance from junction to ambient in free air	40	K/W

QUALITY SPECIFICATION

Quality according to UZW-BO/FQ-0601.

CHARACTERISTICS

V_{P1} = V_{P2} = 13.2 V, T_{amb} = 25 °C, C_{out} = 10 µF; unless otherwise specified (see Fig.5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	supply voltage range	operating	11	13.2	18	V
V_{P1}	supply voltage range	load dump; notes 1and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
V_{P2}	supply voltage range	load dump; note 1	–	–	50	V
I_{P1}	quiescent current	V_{P2} = 0; note 3	–	1.1	1.4	mA
Schmitt triggers						
V_{P2}-SENSE THRESHOLD						
V_{thr}	rising threshold voltage		7.6	8	8.4	V
V_{thf}	falling threshold voltage		6.2	6.5	6.8	V
V_{hy}	hysteresis		1.35	1.5	1.65	V
OUT-OF-REGULATION THRESHOLD						
V_{thr}	rising threshold voltage		6.8	7.35	7.9	V
V_{thf}	falling threshold voltage		5.5	5.95	6.4	V
V_{hy}	hysteresis		1.2	1.4	1.6	V
Reset circuits (for timing, see Fig.3)						
t_{rst1}	reset delay time	C_{rst} = 100 nF	20	40	100	ms
t_{rst}	reset hold time		50	100	150	µs
V_{rl}	reset low	I_{sync} = 1 mA	–	0.15	0.8	V
I_{cr}	delay current (pin 1 to C_{rst})		–	–5	–	µA
t_r	reset rise time	note 4	–	–	1	µs
t_f	reset fall time	note 4	–	–	1	µs
V_{CAP}	voltage pin 1	C_{rst} = 0	5.5	6.0	–	V
R_{sp}	spike-on reset	on-state; note 5	–	0	100	mV
Regulators						
SELECTOR CONTROL INPUTS R4-SEL AND R5-SEL						
V_{sl}	input low voltage		–0.5	–	0.8	V
V_{sh}	input high voltage		2	–	–	V
I_{hs}	input high current	V_{RXsel} > 2 V	–	–	1	µA
I_{ls}	input low current	V_{RXsel} < 0.8 V	–1	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 1 (I_{R1} = 1 mA UNLESS OTHERWISE SPECIFIED)						
V_{R1}	output voltage	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
		6.25 V ≤ V_{P1} ≤ 18 V	4.75	5	5.25	V
V_{R1L}	output voltage	18 V ≤ V_P ≤ 50 V	4.75	5	5.25	V
ΔV_{R1}	line regulation	6.25 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL1}	load regulation	0.5 mA ≤ I_{R1} ≤ 20 mA	–	–	60	mV
RR1	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd1}	drop-out voltage	I_{R1} = 20 mA	–	–	1	V
I_{Rm1}	current limit		30	–	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 2 (I_{R2} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R2}	output voltage	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
		7 V ≤ V_P ≤ 18 V	1.9	2.1	2.3	V
ΔV_{R2}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL2}	load regulation	5 mA ≤ I_{R2} ≤ 200 mA	–	–	70	mV
RR2	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm2}	current limit	V_{R2} > 1.75 V; note 7	250	–	–	mA
I_{Rsc2}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 3 (I_{R3} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R3}	output voltage	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5	5.25	V
ΔV_{R3}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL3}	load regulation	5 mA ≤ I_{R3} ≤ 150 mA	–	–	70	mV
RR3	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
I_{Rm3}	current limit	V_{R3} > 4.5 V; note 7	200	–	–	mA
I_{Rsc3}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 4 (I_{R4} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R4}	output voltage	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R4}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL4}	load regulation	5 mA ≤ I_{R4} ≤ 150 mA	–	–	70	mV
RR4	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd4}	drop-out voltage	I_{R4} = 150 mA	–	–	1	V
I_{Rm4}	current limit	V_{R4} > 8.5 V; note 7	200	–	–	mA
I_{Rsc4}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 5 (I_{R5} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R5}	output voltage	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R5}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL5}	load regulation	5 mA ≤ I_{R5} ≤ 200 mA	–	–	70	mV
RR5	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd5}	dropout voltage	I_{R5} = 200 mA	–	–	1	V
I_{Rm5}	current limit	V_{R5} > 8.5 V; note 7	250	–	–	mA
I_{Rsc5}	short-circuit current	R_L ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 6 (I_{R6} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R6}	output voltage	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.25	V
		11 V ≤ V_P ≤ 18 V	9.3	9.75	10.25	V
ΔV_{R6}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL6}	load regulation	5 mA ≤ I_{R6} ≤ 200 mA	–	–	70	mV
RR6	ripple rejection	f_o = 120 Hz; V_{P1} = V_{P2}; note 6	60	–	–	dB
V_{Rd6}	dropout voltage	I_{R6} = 200 mA	–	–	0.5	V
I_{Rm6}	current limit	V_{R6} > 8.5 V; note 7	300	–	–	mA
I_{Rsc6}	short-circuit current	R_{bel} ≤ 0.5 Ω; note 7	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

Notes

1. During 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V, V_{P2} = R4-sel = R5-sel = 0, I_{R1} = 0.
4. External pull-up resistor of 10 kΩ to 5 V required, and C_{load} ≤ 10 pF.
5. Spike-on reset measured within a time frame of 75 msec.
6. V_{P1} = V_{P2} = 13.2 V, ripple on V_{P1} = V_{P2} of: 1 $V_{(p-p)}$, f_o = 120 Hz.
7. Foldback current protection behaviour: see Fig.4.

Reset circuits

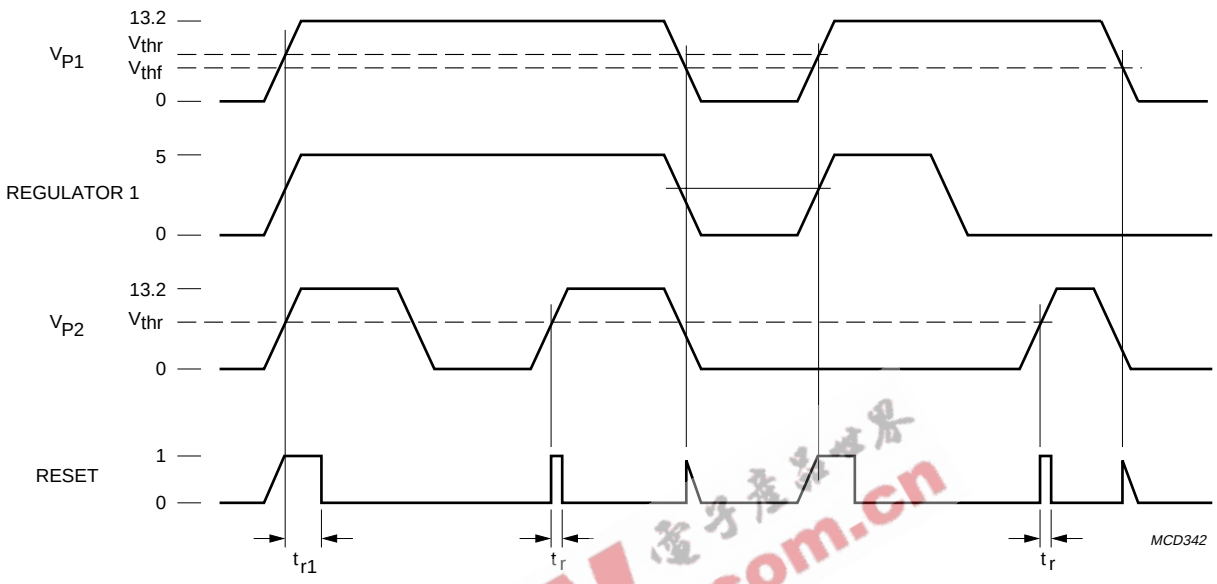


Fig.3 Timing reset.

Regulators truth table (see note 1)

INPUTS				OUTPUTS				
V_{P1}	V_{P2}	R4-SEL	R5-SEL	REG.1	REGS 2 & 3	REG.4	REG.5	REG.6
0	X	X	X	0	0	0	0	0
1	0	X	X	1	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	0	1	1
1	1	1	1	1	1	0	0	1

Note

1. 0 = LOW/OFF;
   1 = HIGH/ON;
   X = don't care.

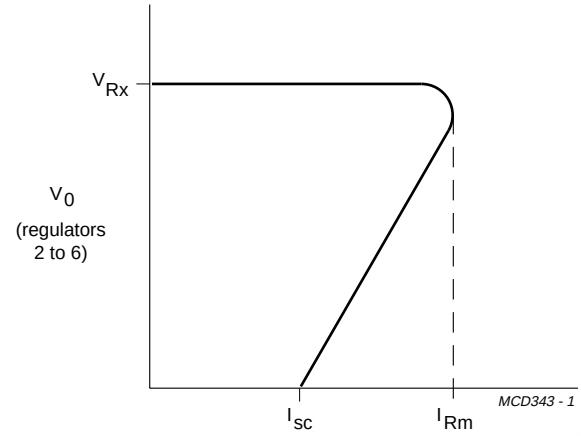
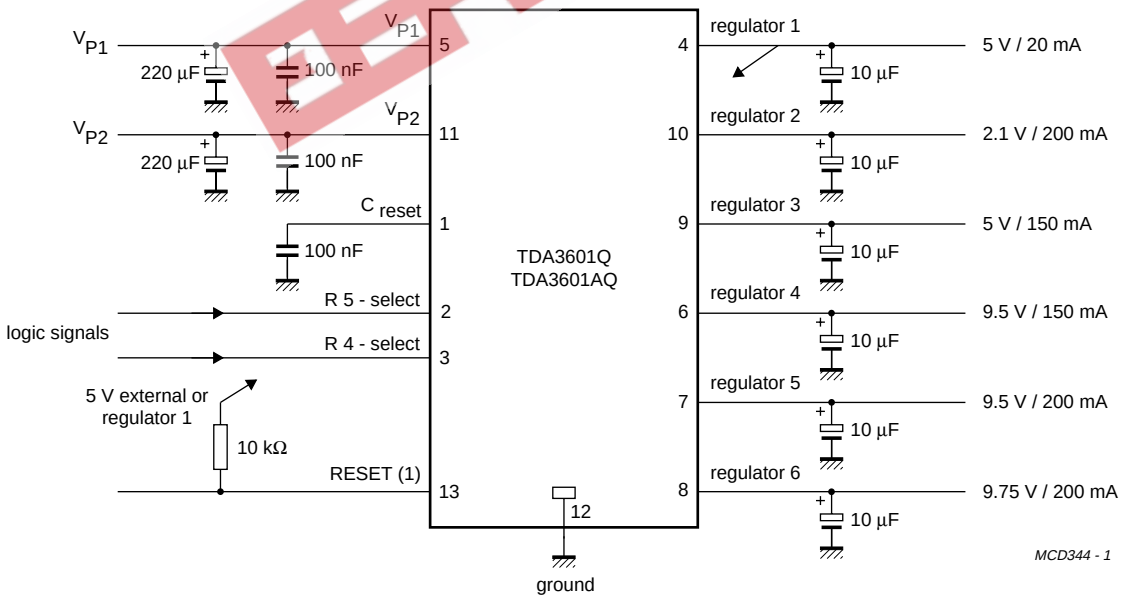


Fig.4 Foldback current protection behaviour.

TEST AND APPLICATION INFORMATION

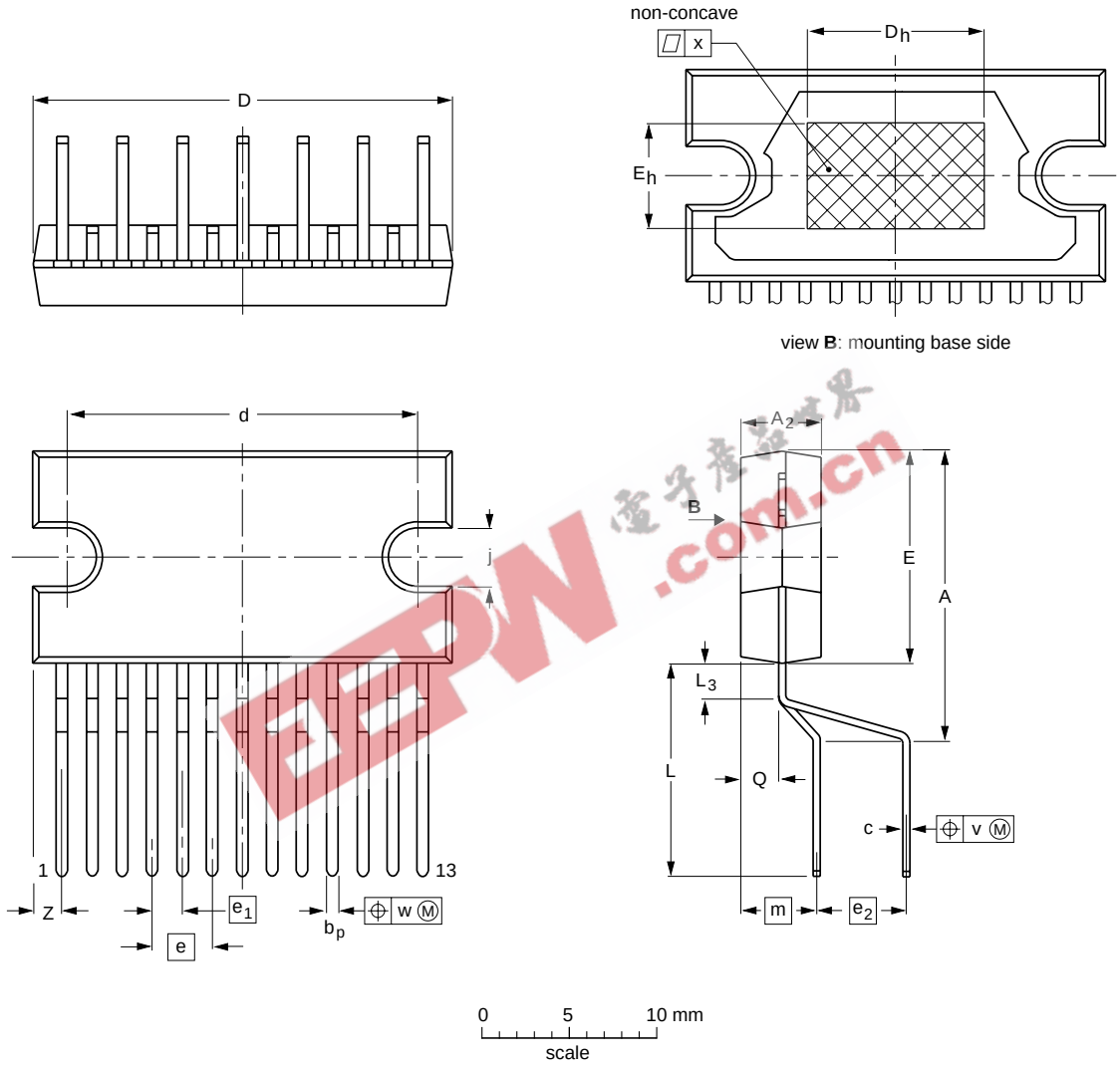


(1) RESET output for TDA3601Q; $\overline{\text{RESET}}$ output for TDA3601AQ.

Fig.5 Application circuit.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~95-03-11~~ 97-12-16

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.