

Complementary Silicon Power Transistors

... designed for general-purpose switching and amplifier applications.

- DC Current Gain — $h_{FE} = 20-70 @ I_C = 4.0 \text{ A dc}$
- Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.1 \text{ Vdc (Max) @ } I_C = 4.0 \text{ A dc}$
- Excellent Safe Operating Area

MAXIMUM RATINGS

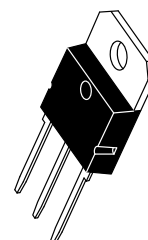
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	1.5	A dc
Base Current	I_B	7.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	90 0.72	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

NPN
TIP3055
PNP
TIP2955

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
90 WATTS



CASE 340D-02

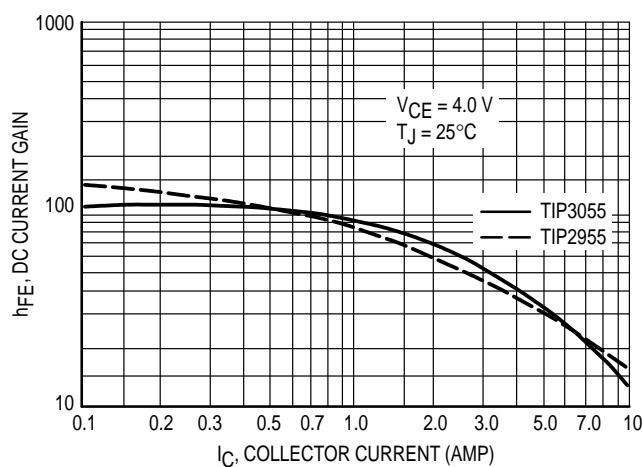


Figure 1. DC Current Gain



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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) ($I_C = 30\text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current ($V_{CE} = 70\text{ Vdc}$, $R_{BE} = 100\text{ Ohms}$)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current ($V_{CE} = 100\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 4.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	20 5.0	70 —	—
Collector–Emitter Saturation Voltage ($I_C = 4.0\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 3.3\text{ Adc}$)	$V_{CE(sat)}$	— —	1.1 3.0	Vdc
Base–Emitter On Voltage ($I_C = 4.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 30\text{ Vdc}$, $t = 1.0\text{ s}$; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
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DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)	f_T	2.5	—	MHz
Small–Signal Current Gain ($V_{CE} = 4.0\text{ Vdc}$, $I_C = 1.0\text{ Adc}$, $f = 1.0\text{ kHz}$)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

NOTE: For additional design curves, refer to electrical characteristics curves of 2N3055.

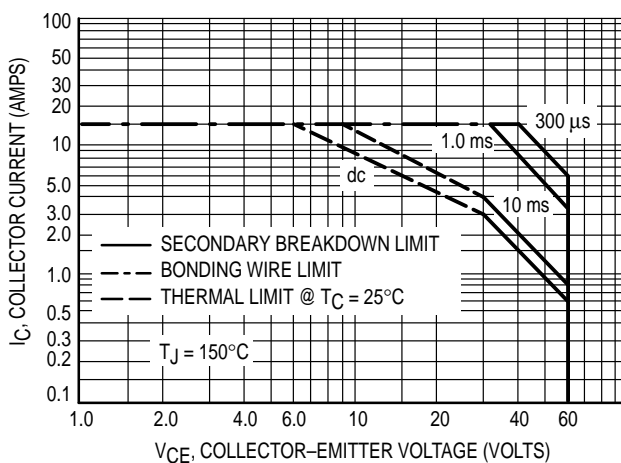
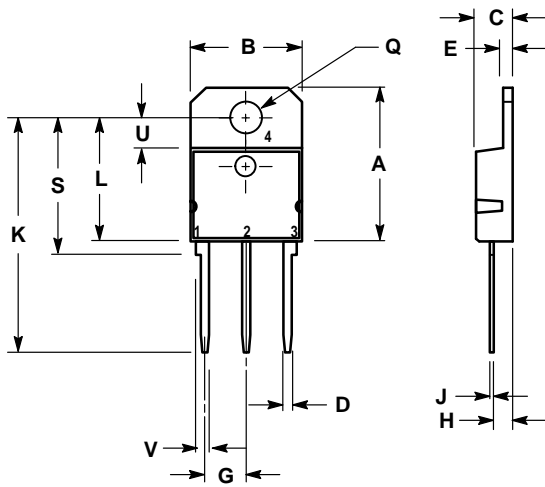


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

PACKAGE DIMENSIONS

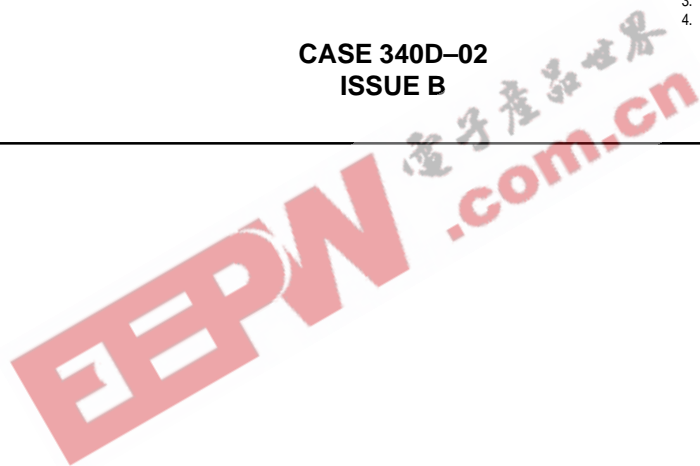


NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	20.35	—	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	—	16.20	—	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	


STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 340D-02
 ISSUE B



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