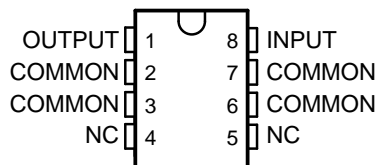


## FEATURES

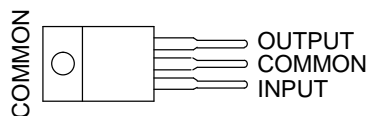
- Very Low Dropout Voltage, Less Than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection Down to –50 V
- Internal Thermal-Overload Protection
- Overvoltage Protection
- Internal Overcurrent-Limiting Circuitry
- Less Than 500- $\mu$ A Disable (TL751L Series)

TL750L... D PACKAGE  
(TOP VIEW)

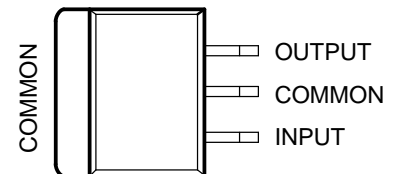


NC – No internal connection

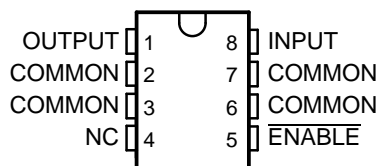
TL750L... KC PACKAGE  
(TOP VIEW)



TL750L... KTE PACKAGE  
(TOP VIEW)

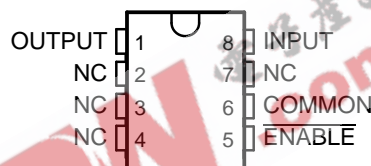


TL751L... D PACKAGE  
(TOP VIEW)



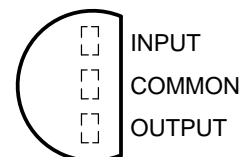
NC – No internal connection

TL751L... P PACKAGE  
(TOP VIEW)



NC – No internal connection

TL750L... LP PACKAGE  
(TO-92, TO-226AA)  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable (ENABLE) input. When ENABLE is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX is a trademark of Texas Instruments.

# TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

SLVS017S – SEPTEMBER 1987 – REVISED AUGUST 2005

## ORDERING INFORMATION

T <sub>J</sub>	V <sub>O</sub> TYP AT 25°C	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER <sup>(2)</sup>	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KTE	Reel of 2000	TL750L05CKTER	TL750L05C
		SOIC – D	Tube of 75	TL750L05CD	50L05C
			Reel of 2500	TL750L05CDR	
			Tube of 75	TL751L05CD	51L05C
			Reel of 2500	TL751L05CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L05CLP	750L05C
	Reel of 2000		TL750L05CLPR		
	TO-220 – KC	Tube of 50	TL750L05CKC	TL750L05C	
	8 V	SOIC – D	Tube of 75	TL750L08CD	50L08C
			Reel of 2500	TL750L08CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L08CLP	750L08C
	10 V	PDIP – P	Tube of 50	TL751L10CP	TL751L10C
		SOIC – D	Tube of 75	TL750L10CD	50L10C
			Reel of 2500	TL750L10CDR	
			Tube of 75	TL751L10CD	51L10C
			Reel of 2500	TL751L10CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L10CLP	750L10C
	Reel of 2000		TL750L10CLPR		
	12 V	SOIC – D	Tube of 75	TL750L12CD	50L12C
			Reel of 2500	TL750L12CDR	
Tube of 75			TL751L12CD	51L12C	
Reel of 2500			TL751L12CDR		
TO-226/TO-92 – LP		Bulk of 1000	TL750L12CLP	750L12C	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) For the most current ordering information, see the Package Option Addendum at the end of this data sheet.

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

### Absolute Maximum Ratings<sup>(1)</sup>

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
	Continuous input voltage		26	V	
	Transient input voltage <sup>(2)</sup>	$T_A = 25^\circ\text{C}$	60	V	
	Continuous reverse input voltage		-15	V	
	Transient reverse input voltage	$t \leq 100 \text{ ms}$	-50	V	
$T_J$	Operating virtual junction temperature		150	$^\circ\text{C}$	
	Lead temperature	1,6 mm (1/16 in) for 10 s	260	$^\circ\text{C}$	
$T_{\text{stg}}$	Storage temperature range		-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The transient input voltage rating applies to the waveform shown in Figure 1.

### Package Thermal Data<sup>(1)</sup>

PACKAGE	BOARD	$\theta_{\text{JC}}$	$\theta_{\text{JA}}$
PDIP (P)	High K, JESD 51-7	57 $^\circ\text{C}/\text{W}$	85 $^\circ\text{C}/\text{W}$
PowerFLEX™ (KTE)	High K, JESD 51-5	3 $^\circ\text{C}/\text{W}$	23 $^\circ\text{C}/\text{W}$
SOIC (D)	High K, JESD 51-7	39 $^\circ\text{C}/\text{W}$	97 $^\circ\text{C}/\text{W}$
TO-226/TO-92 (LP)	High K, JESD 51-7	55 $^\circ\text{C}/\text{W}$	140 $^\circ\text{C}/\text{W}$
TO-220 (KC)	High K, JESD 51-5	3 $^\circ\text{C}/\text{W}$	19 $^\circ\text{C}/\text{W}$

- (1) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{\text{JA}}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{\text{JA}}$ . Operating at the absolute maximum  $T_J$  of 150 $^\circ\text{C}$  can affect reliability.

### Recommended Operating Conditions

over recommended operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_I$	Input voltage	TL75xL05	6	26	V
		TL75xL08	9	26	
		TL75xL10	11	26	
		TL75xL12	13	26	
$V_{\text{IH}}$	High-level $\overline{\text{ENABLE}}$ input voltage	TL75xLxx	2	15	V
$V_{\text{IL}}^{(1)}$	Low-level $\overline{\text{ENABLE}}$ input voltage	$T_J = 25^\circ\text{C}$	-0.3	0.8	V
		$T_J = 0^\circ\text{C}$ to 125 $^\circ\text{C}$	-0.15	0.8	
$I_O$	Output current	TL75xLxx	0	150	mA
$T_J$	Operating virtual junction temperature	TL75xLxxC	0	125	$^\circ\text{C}$

- (1) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for  $\overline{\text{ENABLE}}$  voltage levels and temperature only.

# TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

SLVS017S – SEPTEMBER 1987 – REVISED AUGUST 2005

## TL75xL05 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L05 TL751L05			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V to }26\text{ V}$ , $I_O = 0\text{ to }150\text{ mA}$	$T_J = 25^\circ\text{C}$	4.8	5	5.2	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	4.75		5.25	
Input regulation voltage	$V_I = 9\text{ V to }16\text{ V}$			5	10	mV
	$V_I = 6\text{ V to }26\text{ V}$			6	30	
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$ , $f = 120\text{ Hz}$		60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to }150\text{ mA}$			20	50	mV
Dropout voltage	$I_O = 10\text{ mA}$				0.2	V
	$I_O = 150\text{ mA}$				0.6	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$			500		$\mu\text{V}$
Input bias current	$I_O = 150\text{ mA}$			10	12	mA
	$V_I = 6\text{ V to }26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to }125^\circ\text{C}$			1	2	
	$\text{ENABLE} \geq 2\text{ V}$				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

## TL75xL08 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L08 TL751L08			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 9\text{ V to }26\text{ V}$ , $I_O = 0\text{ to }150\text{ mA}$	$T_J = 25^\circ\text{C}$	7.68	8	8.32	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	7.6		8.4	
Input regulation voltage	$V_I = 10\text{ V to }17\text{ V}$			10	20	mV
	$V_I = 9\text{ V to }26\text{ V}$			25	50	
Ripple rejection	$V_I = 11\text{ V to }21\text{ V}$ , $f = 120\text{ Hz}$		60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to }150\text{ mA}$			40	80	mV
Dropout voltage	$I_O = 10\text{ mA}$				0.2	V
	$I_O = 150\text{ mA}$				0.6	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$			500		$\mu\text{V}$
Input bias current	$I_O = 150\text{ mA}$			10	12	mA
	$V_I = 9\text{ V to }26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to }125^\circ\text{C}$			1	2	
	$\text{ENABLE} \geq 2\text{ V}$				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

### TL75xL10 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L10 TL751L10			UNIT	
		MIN	TYP	MAX		
Output voltage	$V_I = 11\text{ V to }26\text{ V}$ , $I_O = 0\text{ to }150\text{ mA}$	$T_J = 25^\circ\text{C}$	9.6	10	10.4	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	9.5		10.5	
Input regulation voltage	$V_I = 12\text{ V to }19\text{ V}$		10	25	mV	
	$V_I = 11\text{ V to }26\text{ V}$		30	60		
Ripple rejection	$V_I = 12\text{ V to }22\text{ V}$ , $f = 120\text{ Hz}$	60	65		dB	
Output regulation voltage	$I_O = 5\text{ mA to }150\text{ mA}$		50	100	mV	
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V	
	$I_O = 150\text{ mA}$			0.6		
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		700		$\mu\text{V}$	
Input bias current	$I_O = 150\text{ mA}$		10	12	mA	
	$V_I = 11\text{ V to }26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to }125^\circ\text{C}$		1	2		
	$\text{ENABLE} \geq 2\text{ V}$			0.5		

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

### TL75xL12 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L12 TL751L12			UNIT	
		MIN	TYP	MAX		
Output voltage	$V_I = 13\text{ V to }26\text{ V}$ , $I_O = 0\text{ to }150\text{ mA}$	$T_J = 25^\circ\text{C}$	11.52	12	12.48	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	11.4		12.6	
Input regulation voltage	$V_I = 14\text{ V to }19\text{ V}$		15	30	mV	
	$V_I = 13\text{ V to }26\text{ V}$		20	40		
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$ , $f = 120\text{ Hz}$	50	55		dB	
Output regulation voltage	$I_O = 5\text{ mA to }150\text{ mA}$		50	120	mV	
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V	
	$I_O = 150\text{ mA}$			0.6		
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		700		$\mu\text{V}$	
Input bias current	$I_O = 150\text{ mA}$		10	12	mA	
	$V_I = 13\text{ V to }26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to }125^\circ\text{C}$		1	2		
	$\text{ENABLE} \geq 2\text{ V}$			0.5		

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

## PARAMETER MEASUREMENT INFORMATION

The TL750L, TL751L series are low-dropout regulators. This means that capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and its equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and temperature range. Figure 1 shows the recommended range of ESR for a given load with a  $10\text{-}\mu\text{F}$  capacitor on the output.

TYPICAL CHARACTERISTICS

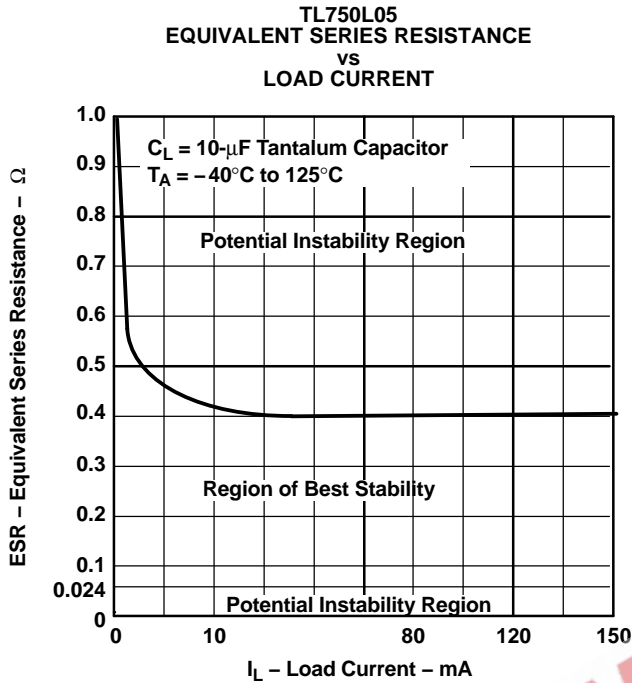


Figure 1.

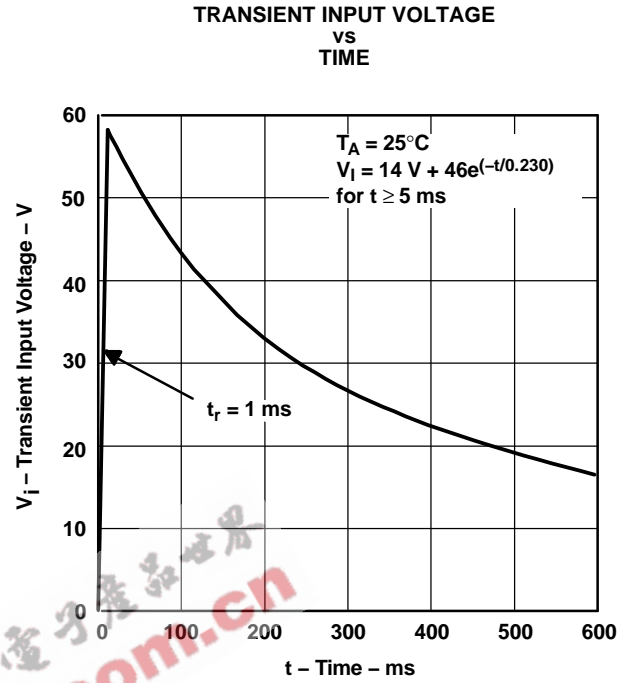


Figure 2.

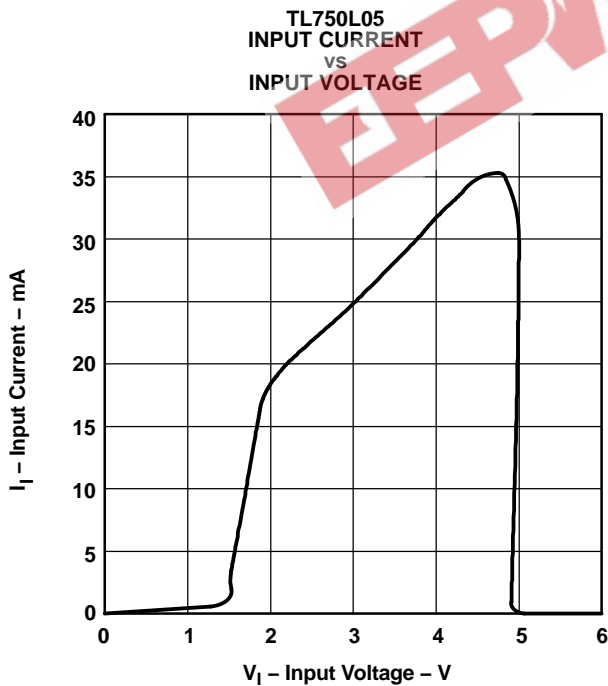


Figure 3.

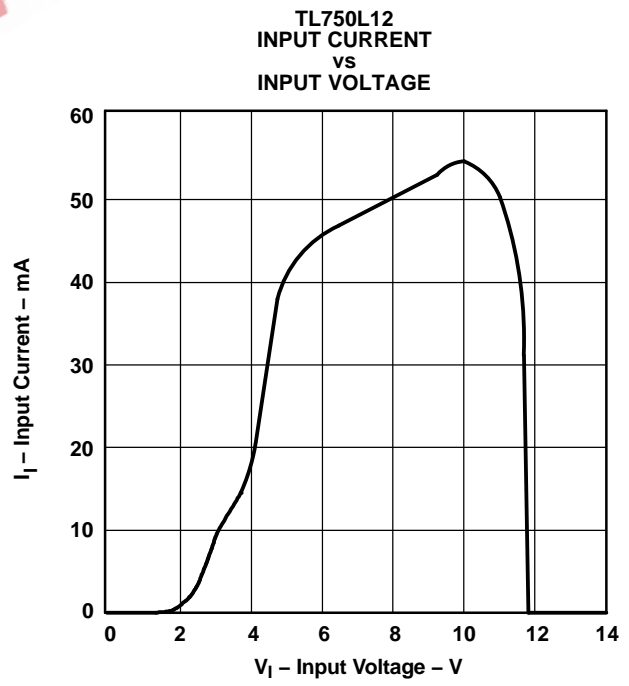


Figure 4.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9166901Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
5962-9166901QPA	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL750L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L05CKC	ACTIVE	TO-220	KC	3	50	TBD	CU SNPB	Level-NC-NC-NC
TL750L05CKTER	ACTIVE	PFM	KTE	3	2000	TBD	CU SNPB	Level-1-220C-UNLIM
TL750L05CLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
TL750L05CLPM	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL750L05CLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
TL750L05CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L05QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L05QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L05QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L05QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL750L05QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L08CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L08CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L08CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L08CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L08CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L08CLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
TL750L08CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L08QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L08QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L08QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L08QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL750L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L10CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L10CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L10CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L10CLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL750L10CLPR	ACTIVE	TO-92	LP	3	2000	TBD	CU SNPB	Level-NC-NC-NC
TL750L10CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L10QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L10QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L10QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L10QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL750L10QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L12CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L12CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL750L12CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L12CLP	ACTIVE	TO-92	LP	3	1000	TBD	CU SNPB	Level-NC-NC-NC
TL750L12CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL750L12QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L12QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL750L12QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TL750L12QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL750L12QP	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL751L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL751L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL751L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL751L05CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL751L05MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL751L05MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL751L05QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L05QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L05QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL751L08CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L08CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL751L08QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L08QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L10CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL751L10CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L10CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL751L10CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL751L10QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L10QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL751L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L12CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L12CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL751L12CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL751L12MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL751L12MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL751L12QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L12QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL751L12QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

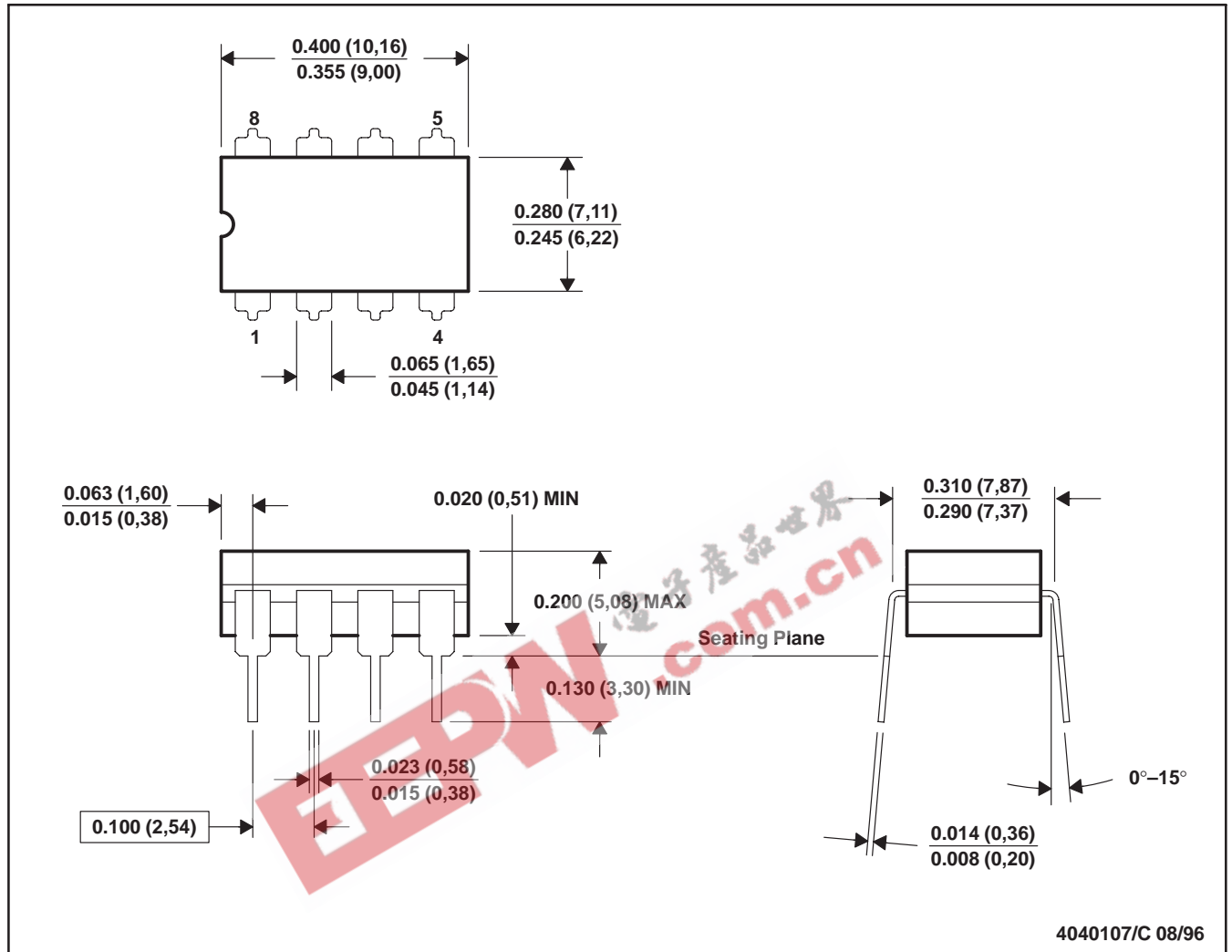
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# MECHANICAL DATA

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification.
  - Falls within MIL STD 1835 GDIP1-T8

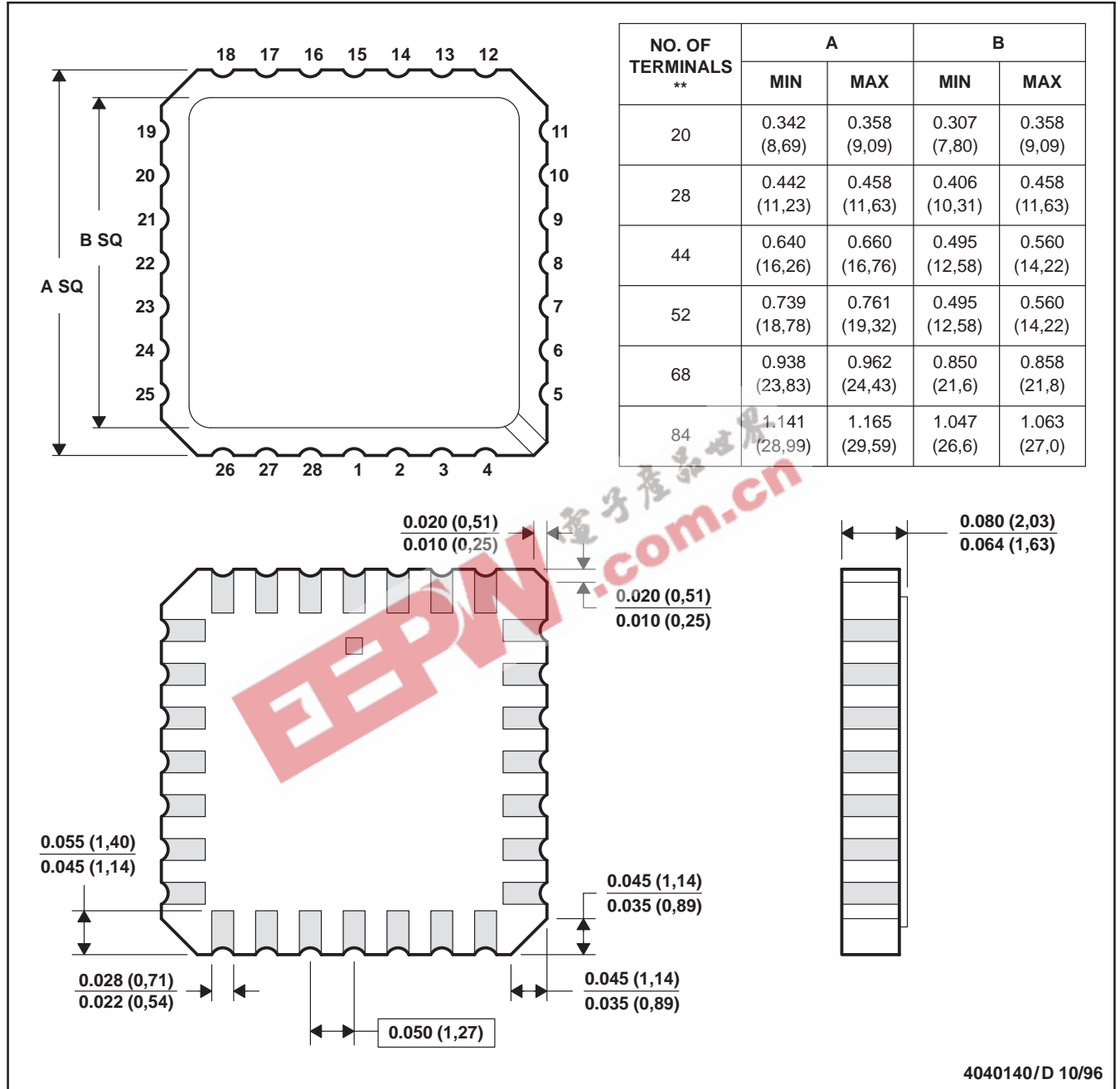
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



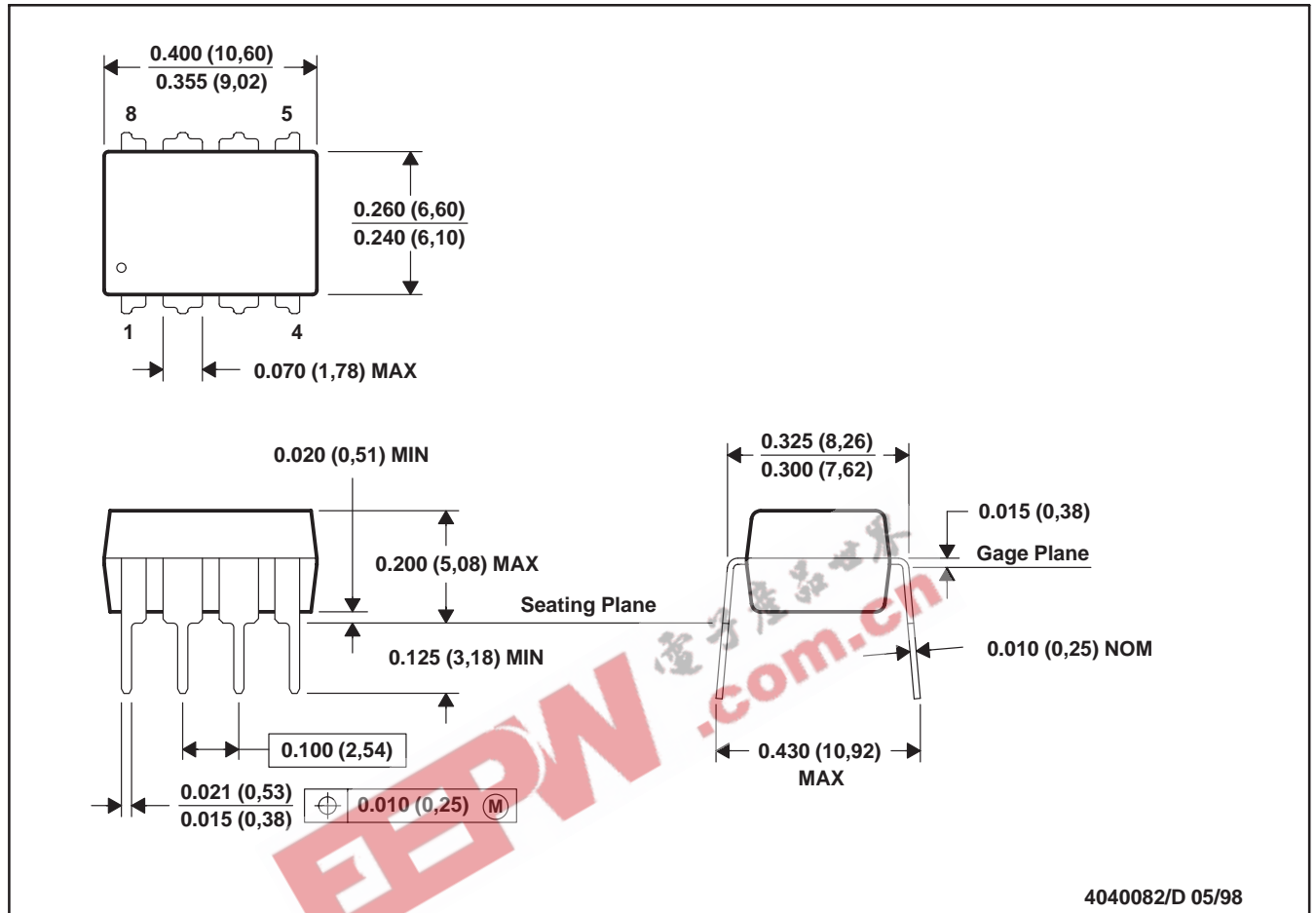
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

# MECHANICAL DATA

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)



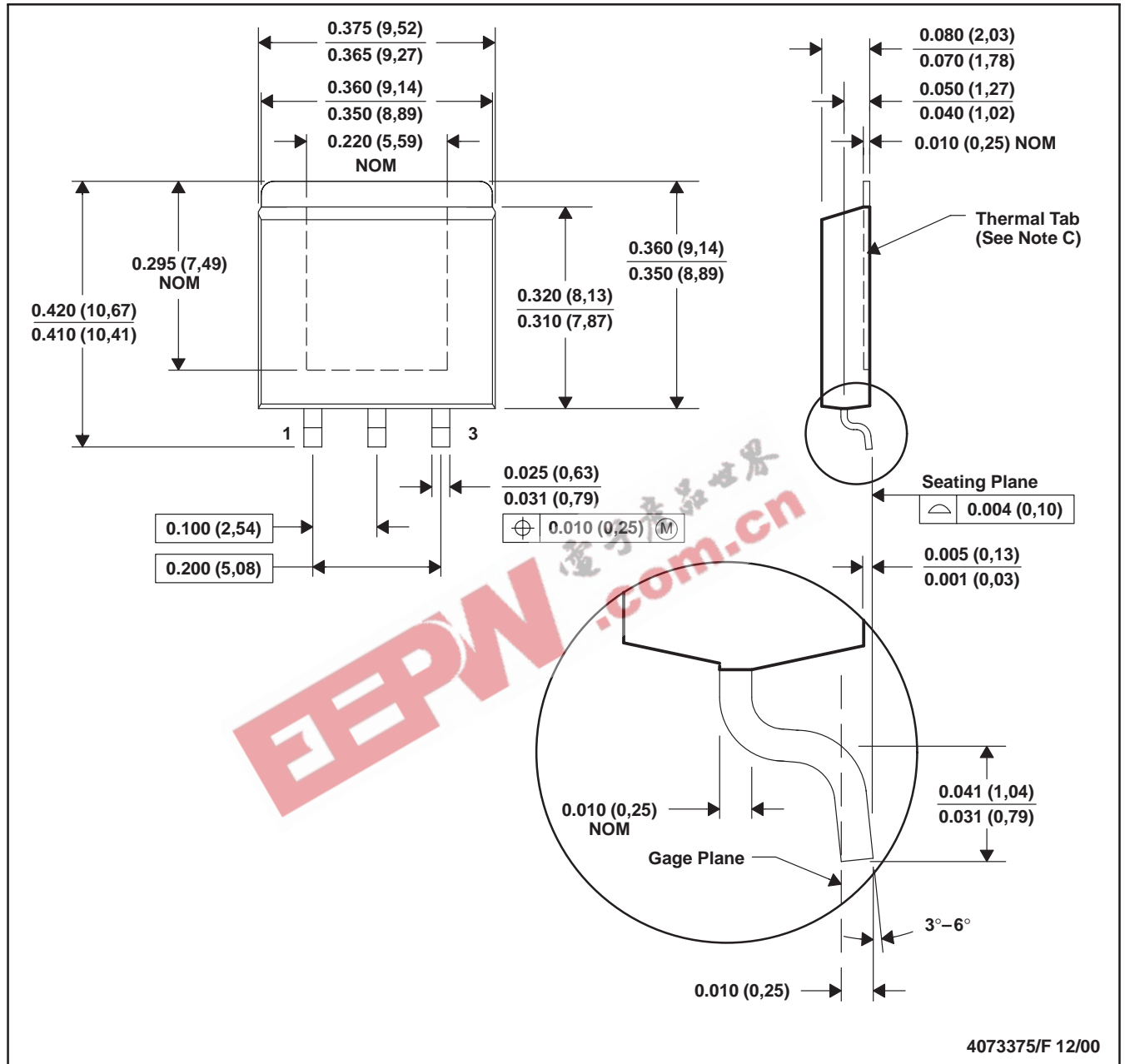
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# MECHANICAL DATA

MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

KTE (R-PSFM-G3)

PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. The center lead is in electrical contact with the thermal tab.  
 D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).  
 E. Falls within JEDEC MO-169

PowerFLEX is a trademark of Texas Instruments.

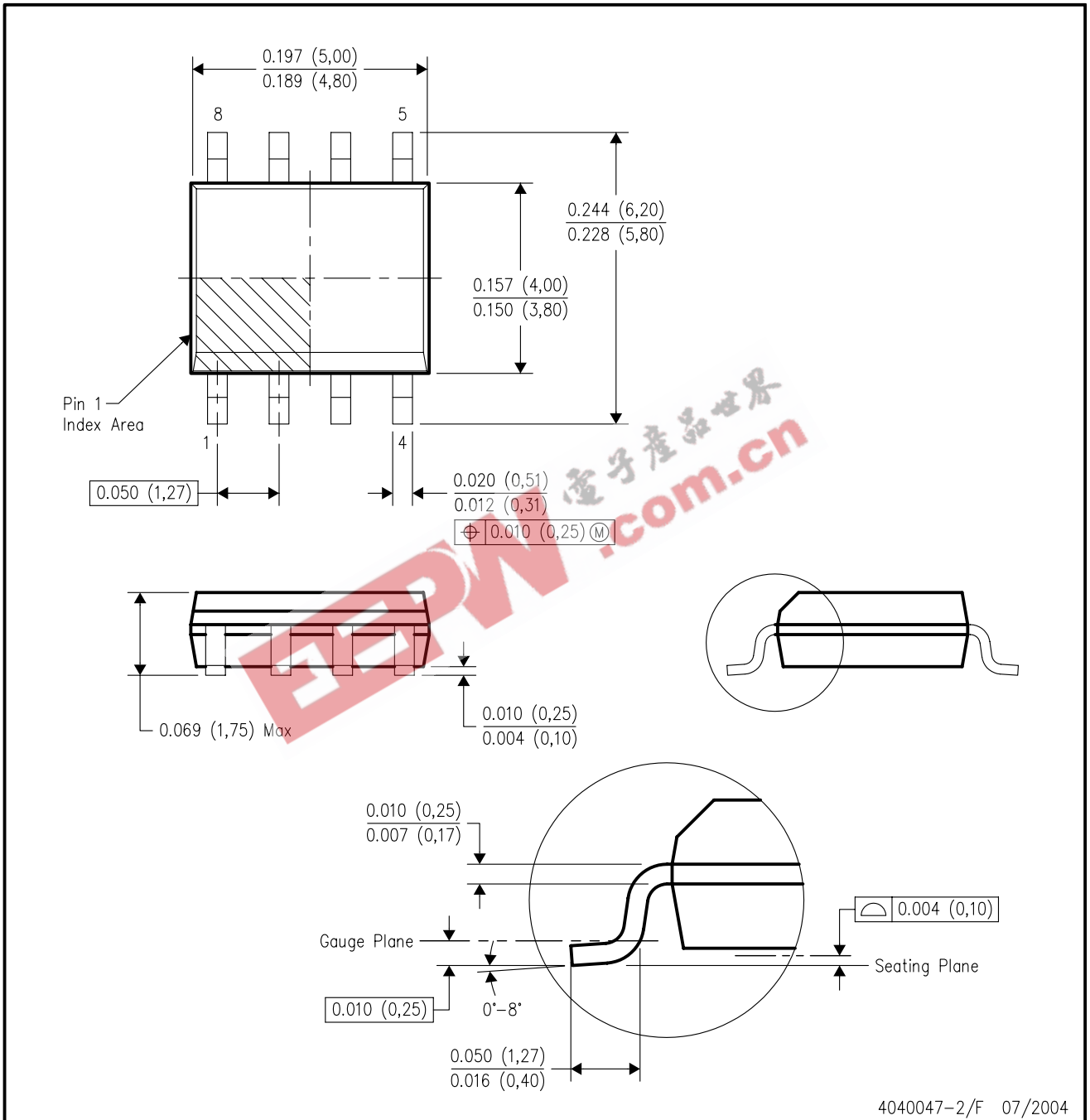
 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# MECHANICAL DATA

## D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



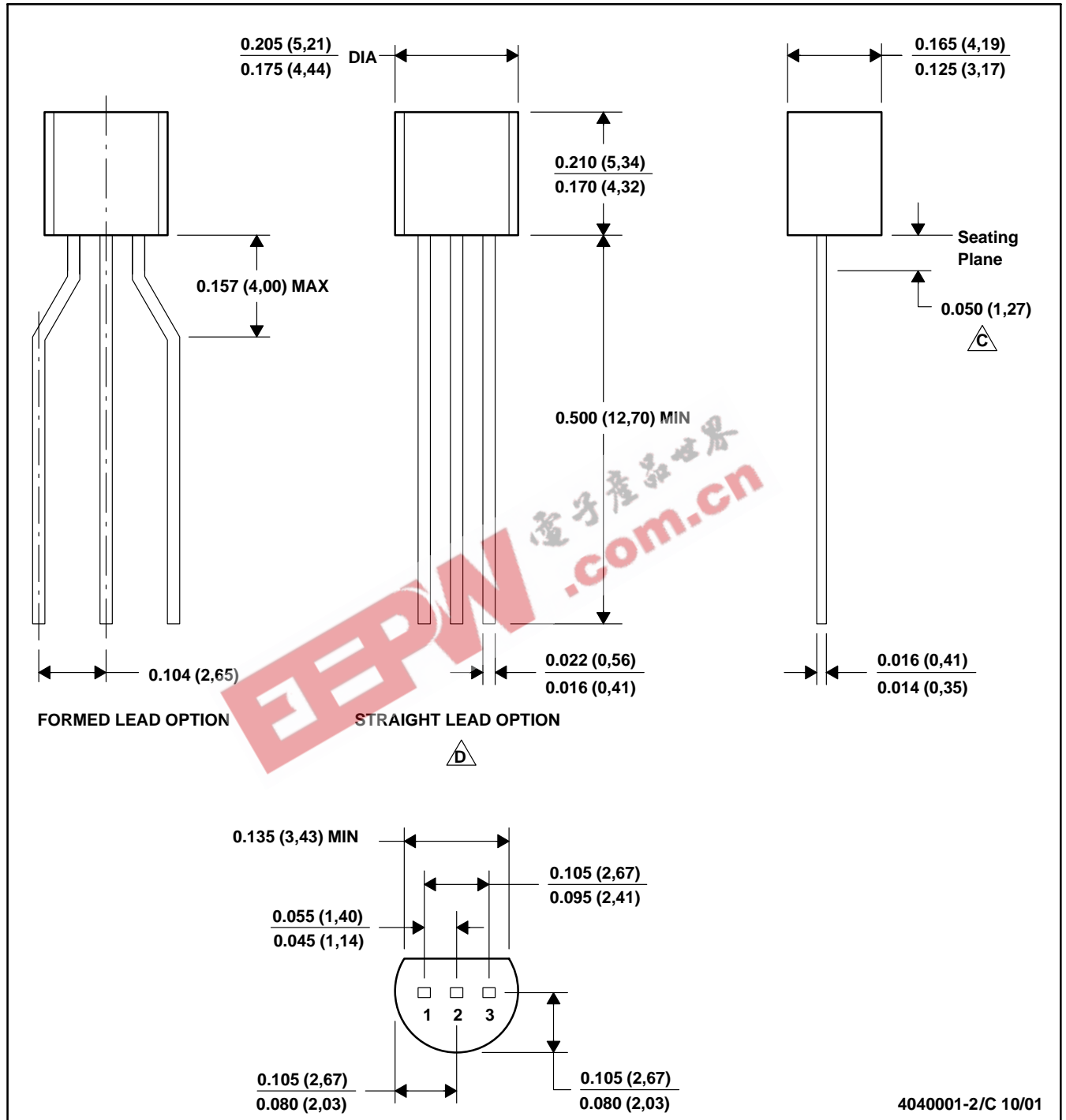
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AA.



# MECHANICAL DATA

MSOT002A – OCTOBER 1994 – REVISED NOVEMBER 2001

## LP (O-PBCY-W3)

## PLASTIC CYLINDRICAL PACKAGE



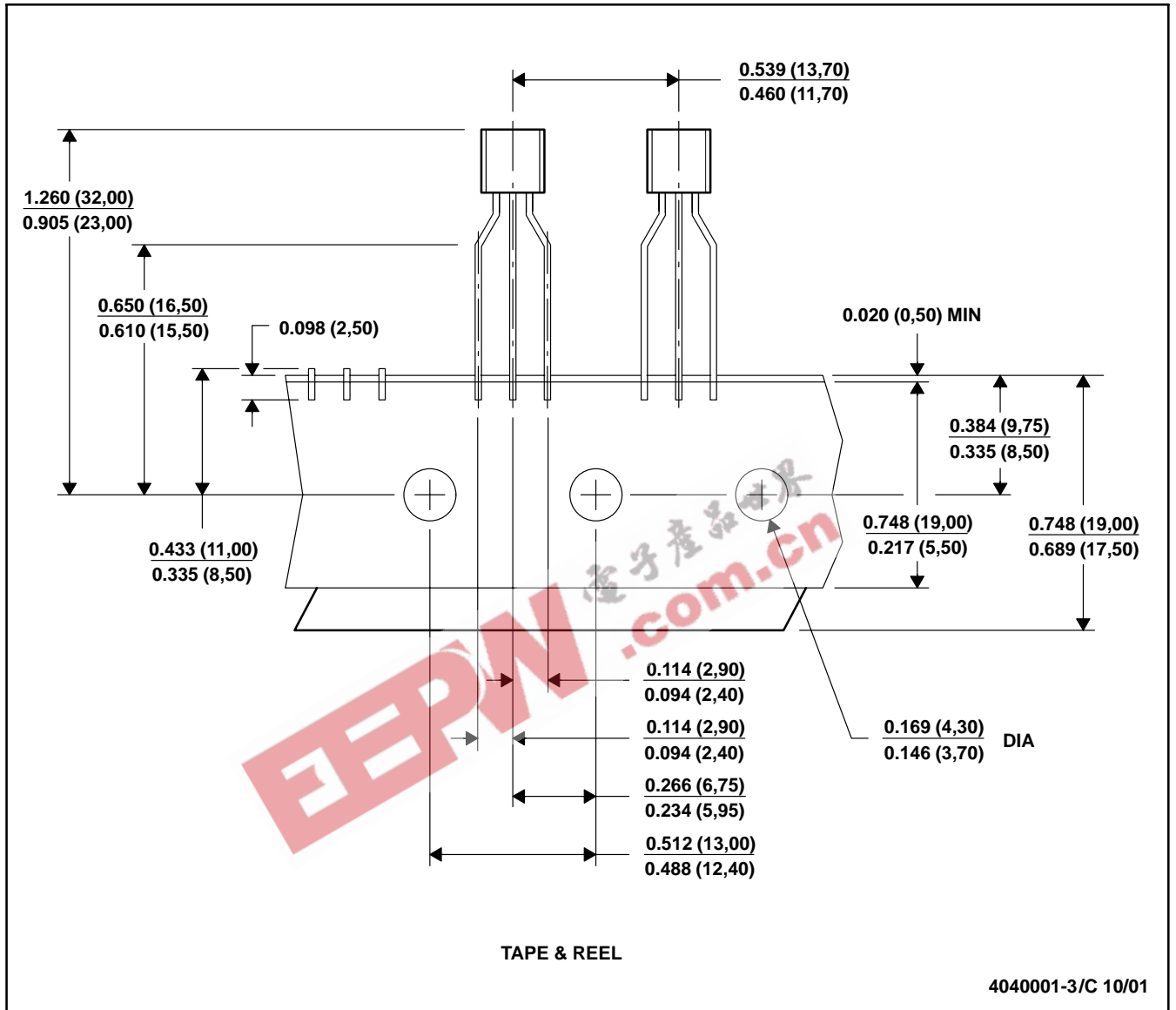
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Lead dimensions are not controlled within this area
  -  Falls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
  - E. Shipping Method:
    - Straight lead option available in bulk pack only.
    - Formed lead option available in tape & reel or ammo pack.

# MECHANICAL DATA

MSOT002A – OCTOBER 1994 – REVISED NOVEMBER 2001

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



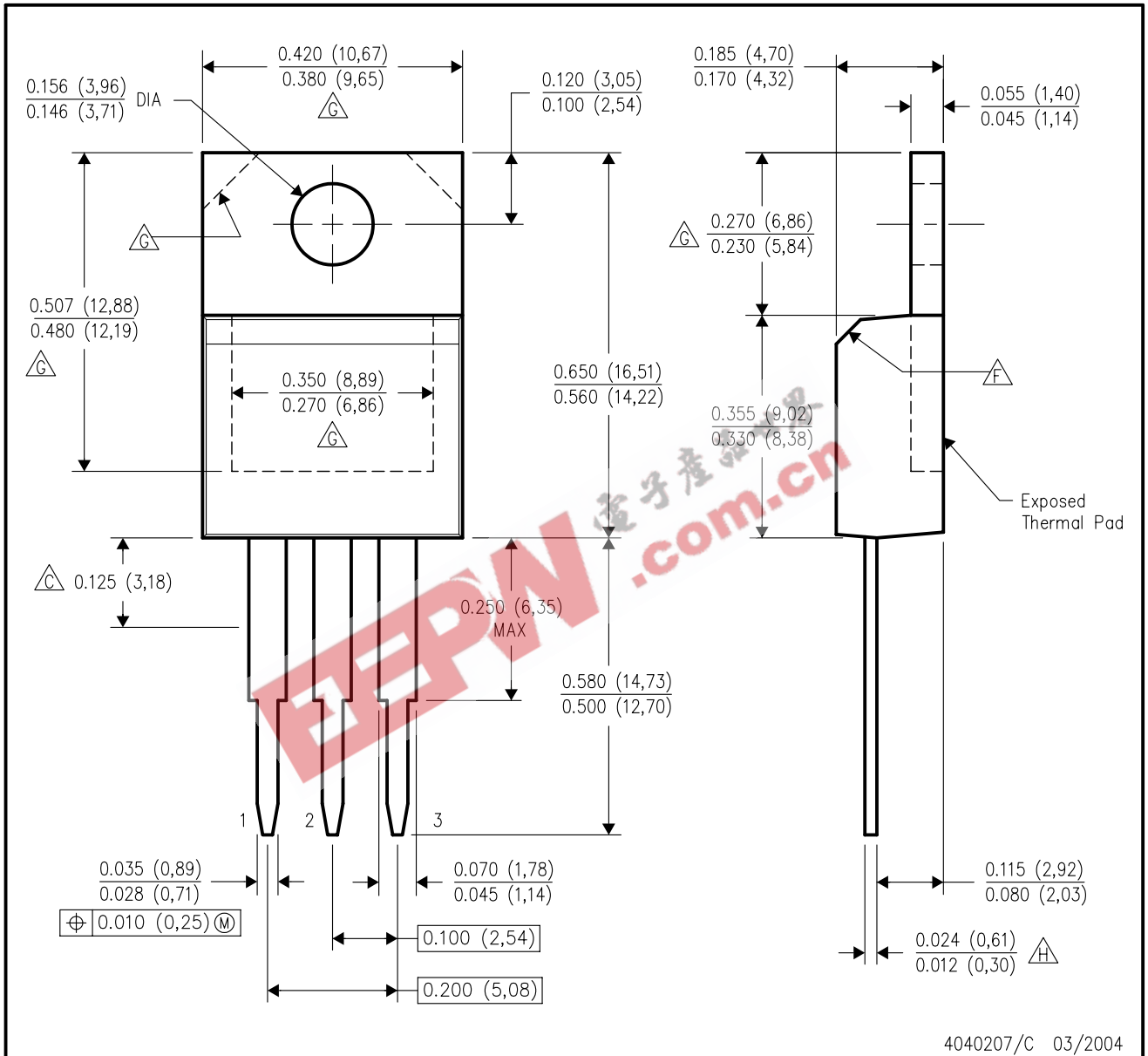
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Tape and Reel information for the Format Lead Option package.



# MECHANICAL DATA

## KC (R-PSFM-T3)

## PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Lead dimensions are not controlled within this area.
  - D. All lead dimensions apply before solder dip.
  - E. The center lead is in electrical contact with the mounting tab.
  - $\triangle F$  The chamfer is optional.
  - $\triangle G$  Thermal pad contour optional within these dimensions.
  - $\triangle H$  Falls within JEDEC TO-220 variation AB, except minimum lead thickness.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265