

TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- $\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1 \text{ V}$
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Duration

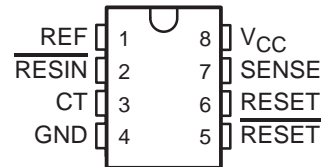
description

The TL7702B and TL7705B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

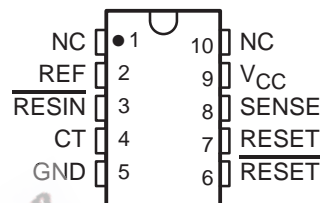
An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC and TL7705BC are characterized for operation from 0°C to 70°C. The TL7702BI and TL7705BI are characterized for operation from -40°C to 85°C. The TL7705BQ is characterized for operation from -40°C to 125°C. The TL7705BM is characterized for operation from -55°C to 125°C.

TL77xxBC . . . D OR P PACKAGE
TL7705BM . . . JG PACKAGE
TL7705BQ . . . D PACKAGE
(TOP VIEW)

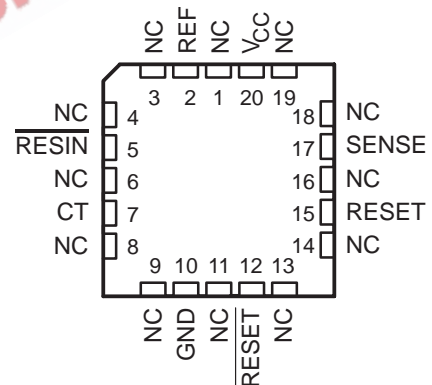


TL7705BM . . . U PACKAGE
(TOP VIEW)



NC – No internal connection

TL7705BM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES					CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLATPACK (U)	
0°C to 70°C	TL7702BCD	—	—	TL7702BCP	—	TL7702BY, TL7705BY
	TL7705BCD	—	—	TL7705BCP	—	
–40°C to 85°C	TL7702BID	—	—	TL7702BIP	—	
	TL7705BID	—	—	TL7705BIP	—	
–40°C to 125°C	TL7705BQD	—	—	—	—	
–55°C to 125°C	—	TL7702BMFK	TL7702BMJG	—	TL7702BMU	
	—	TL7705BMFK	TL7705BMJG	—	TL7705BMU	

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL7702BCDR). Chip forms are tested at 25°C.

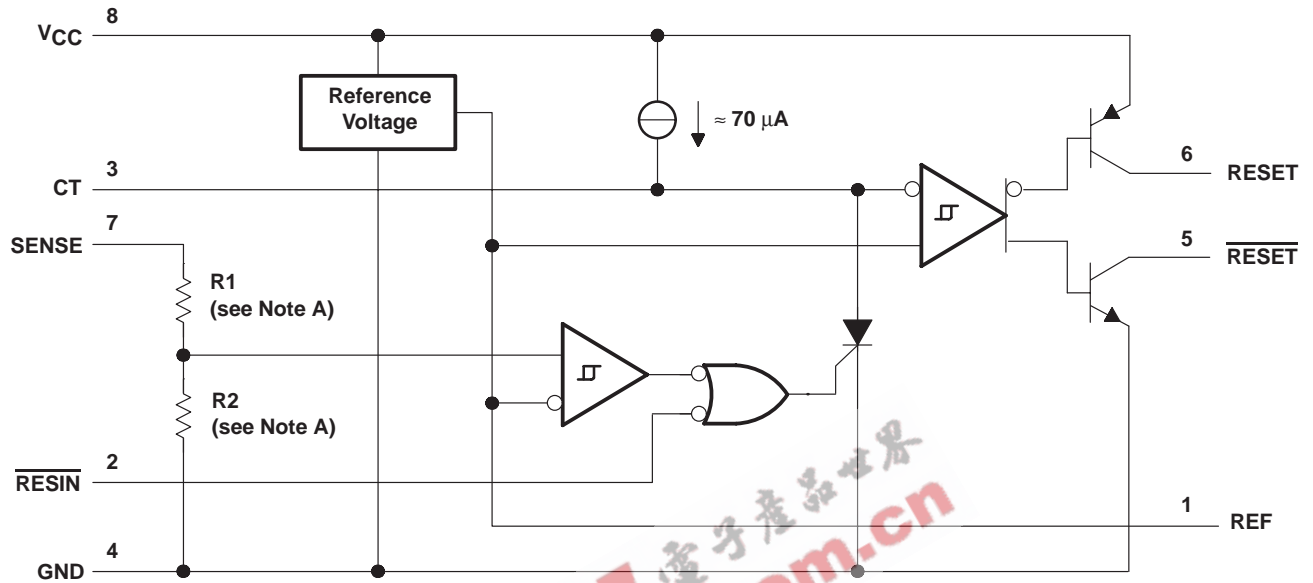
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TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

functional block diagram

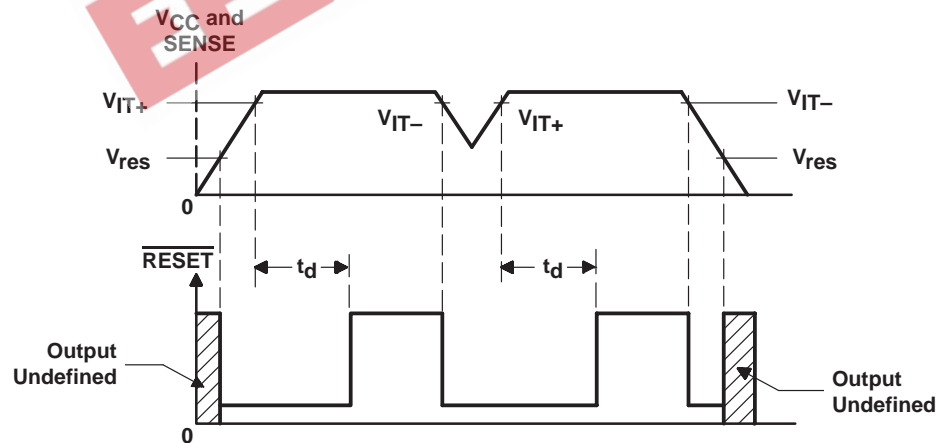
The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



Pin numbers shown are for the D, JG, and P packages.

NOTE A: TL7702B: R1 = 0 Ω, R2 = open
TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal

typical timing diagram



TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I : $\overline{\text{RESIN}}$	-0.3 V to 20 V
SENSE	-0.3 V to 20 V
High-level output current, I_{OH} (RESET)	-30 mA
Low-level output current, I_{OL} (RESET)	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
P package	127°C/W
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or U packages	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values are with respect to the network ground terminal.
 - Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 - The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	18	V
High-level input voltage, V_{IH}	$\overline{\text{RESIN}}$	2	18	V
Low-level input voltage, V_{IL}	$\overline{\text{RESIN}}$	0	0.8	V
Input voltage, V_I	SENSE	0	18	V
High-level output current, I_{OH}	RESET		-16	mA
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		16	mA
Operating free-air temperature range, T_A	TL770xBC	0	70	°C
	TL770xBI	-40	85	
	TL7705BQ	-40	125	
	TL7705BM	-55	125	

TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION [†]		TL77xxBC TL77xxBI TL7705BQ			UNIT
				MIN	TYP	MAX	
V _{OH}	High-level output voltage, RESET	I _{OH} = -16 mA		V _{CC} -1.5			V
V _{OL}	Low-level output voltage, RESET	I _{OL} = 16 mA		0.4			V
V _{ref}	Reference voltage	I _{ref} = 500 μA, T _A = 25°C		2.48	2.53	2.58	V
V _{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	T _A = 25°C	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7702B	T _A = full range [‡]	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
V _{hys}	Hysteresis, SENSE (V _{IT+} - V _{IT-})	TL7702B	V _{CC} = 3.6 V to 18 V, T _A = 25°C	10			mV
		TL7705B		30			
V _{res} [§]	Power-up reset voltage	I _{OL} at RESET = 2 mA, T _A = 25°C		1			V
I _I	Input current	RESIN	V _I = 0.4 V to V _{CC}	-10			μA
		SENSE	TL7702B V _I = V _{ref} to 18 V	-0.1 -2			
I _{OH}	High-level output current, RESET	V _O = 18 V, See Figure 1		50			μA
I _{OL}	Low-level output current, RESET	V _O = 0 V, See Figure 1		-50			μA
I _{CC}	Supply current	V _{SENSE} = 15 V, RESIN ≥ 2 V		1.8	3		mA
		V _{CC} = 18 V, T _A = full range [‡]		3.5			mA

[†] All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V_{CC} to GND.

[‡] Full range is 0°C to 70°C for the C-suffix devices, -40°C to 85°C for the I-suffix devices, and -40°C to 125°C for the Q-suffix device.

[§] This is the lowest voltage at which RESET becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC TL77xxBI TL7705BQ			UNIT
				MIN	TYP	MAX	
t _{PLH}	RESIN	RESET	See Figures 1, 2, and 3	270	500	ns	
t _{PHL}	RESIN	RESET		270	500	ns	
t _w	RESIN		See Figure 2	150		ns	
	SENSE			100			
t _r		RESET	See Figures 1 and 3	75		ns	
t _f				150 200			
t _r		RESET		75 150		ns	
t _f				50			

TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL7705BM			UNIT
				MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage, $\overline{\text{RESET}}$	I _{OH} = -16 mA		V _{CC} -1.5			V
V _{OL}	Low-level output voltage, $\overline{\text{RESET}}$	I _{OL} = 16 mA		0.4			V
V _{ref}	Reference voltage	I _{ref} = 500 μ A, T _A = 25°C		2.48	2.53	2.58	V
V _{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	T _A = 25°C	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7702B	T _A = -55°C to 125°C	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
V _{hys}	Hysteresis, SENSE (V _{IT+} - V _{IT-})	TL7702B	V _{CC} = 3.6 V to 18 V, T _A = 25°C	10			mV
TL7705B	30						
V _{res} ‡	Power-up reset voltage	I _{OL} at $\overline{\text{RESET}}$ = 2 mA, T _A = 25°C		1			V
I _I	Input current	$\overline{\text{RESIN}}$		V _I = 0.4 V to V _{CC}			μ A
		SENSE	TL7702B	V _I = V _{ref} to V _{CC} - 1.5 V			
I _{OH}	High-level output current, $\overline{\text{RESET}}$	V _O = 18 V		50			μ A
I _{OL}	Low-level output current, $\overline{\text{RESET}}$	V _O = 0		-50			μ A
I _{CC}	Supply current	V _{SENSE} = 15 V, $\overline{\text{RESIN}} \geq 2$ V		1.8			mA
		V _{CC} = 18 V, T _A = -55°C to 125°C		4			

† All electrical characteristics are measured with 0.1- μ F capacitors connected at REF, CT, and V_{CC} to GND.

‡ This is the lowest value at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7705BM			UNIT
				MIN	TYP	MAX	
t _{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3	270	500*	ns
t _{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$		270	500*	
t _w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2	150		ns
		SENSE			100		
t _r	Rise time		RESET	See Figures 1 and 3	75*		ns
t _f	Fall time				150 200*		
t _r	Rise time		$\overline{\text{RESET}}$		75 150*		ns
t _f	Fall time				50*		

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITION [†]		TL7702BY TL7705BY			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, $\overline{\text{RESET}}$	$I_{OH} = -16\text{ mA}$		$V_{CC} - 1.5$			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$	$I_{OL} = 16\text{ mA}$		0.4			V
V_{ref}	Reference voltage	$I_{ref} = 500\ \mu\text{A}$		2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input	TL7702BY		2.505	2.53	2.555	V
		TL7705BY		4.5	4.55	4.6	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702BY	$V_{CC} = 3.6\text{ V to }18\text{ V}$	10			mV
		TL7705BY		30			
V_{res}^\ddagger	Power-up reset voltage	I_{OL} at $\overline{\text{RESET}} = 2\text{ mA}$		1			V
I_I	Input current	RESIN	$V_I = 0.4\text{ V to }V_{CC}$	-10			μA
		SENSE	TL7702BY $V_I = V_{ref}$ to 18 V	-0.1 -2			
I_{OH}	High-level output current, $\overline{\text{RESET}}$	$V_O = 18\text{ V}$, See Figure 1		50			μA
I_{OL}	Low-level output current, $\overline{\text{RESET}}$	$V_O = 0\text{ V}$, See Figure 1		-50			μA
I_{CC}	Supply current	$V_{SENSE} = 15\text{ V}$, $\text{RESIN} \geq 2\text{ V}$		1.8	3		mA

[†] All electrical characteristics are measured with 0.1- μF capacitors connected at REF, CT, and V_{CC} to GND.

[‡] This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

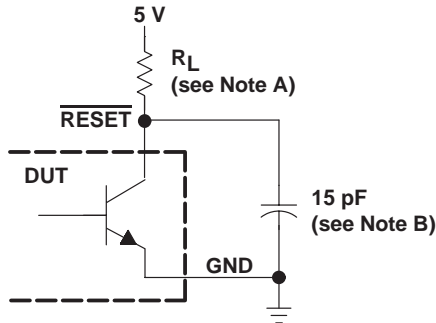
switching characteristics, $V_{CC} = 5\text{ V}$, CT open, $T_A = 25^\circ\text{C}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7702BY TL7705BY			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3	270	500	ns	
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$		270	500		
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2	150		ns	
		SENSE			100			
t_r	Rise time		RESET	See Figures 1 and 3	75		ns	
t_f	Fall time				150 200			
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3	75 150		ns	
t_f	Fall time				50			

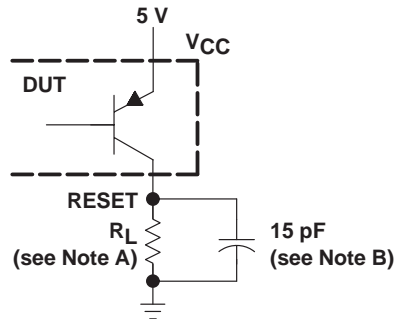
TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION



RESET OUTPUT CONFIGURATION

NOTES: A. For I_{OL} and I_{OH} , $R_L = 10 \text{ k}\Omega$. For all switching characteristics, $R_L = 511 \Omega$.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations



Figure 2. Input Pulse Definition

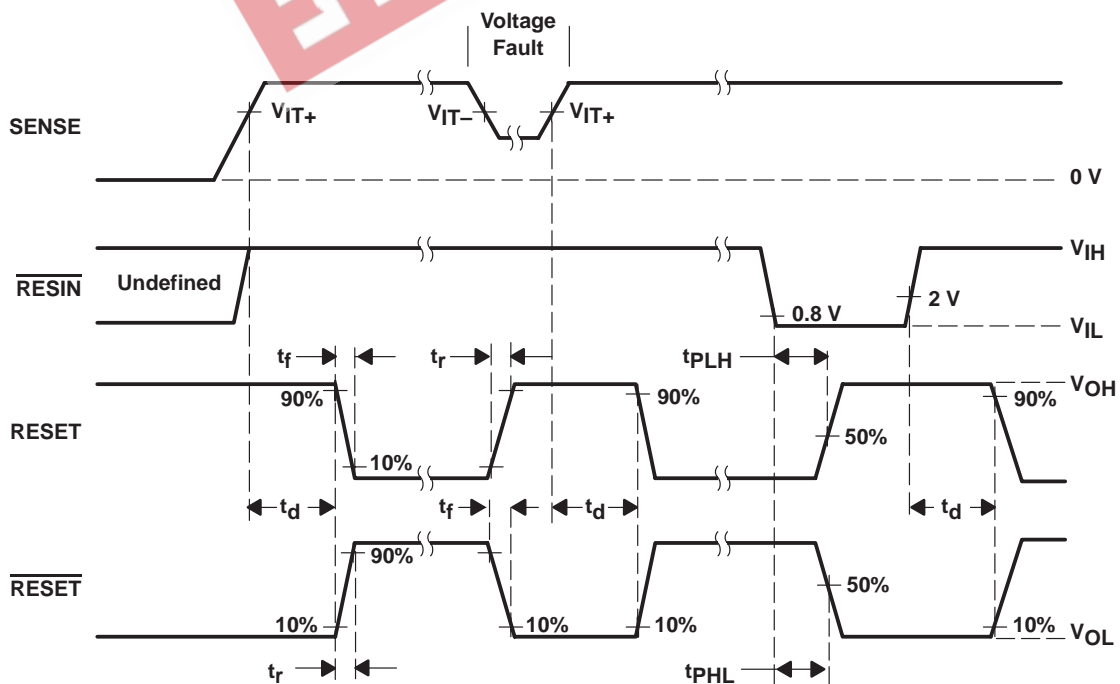
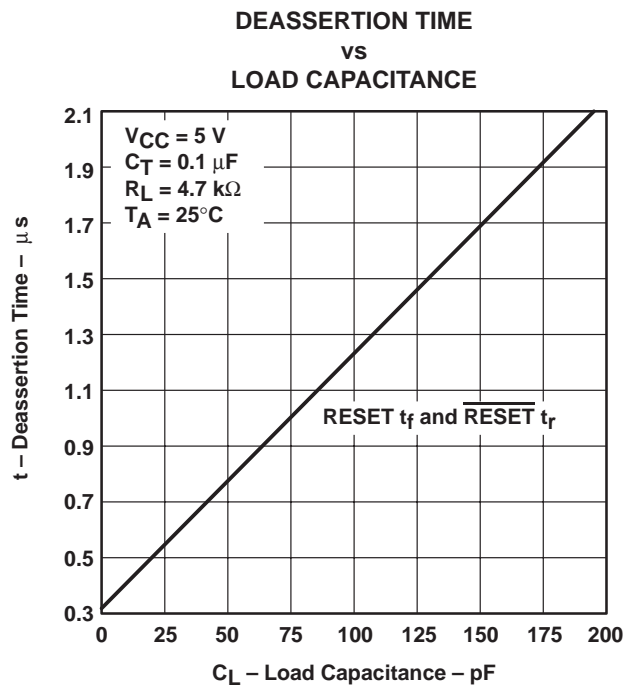
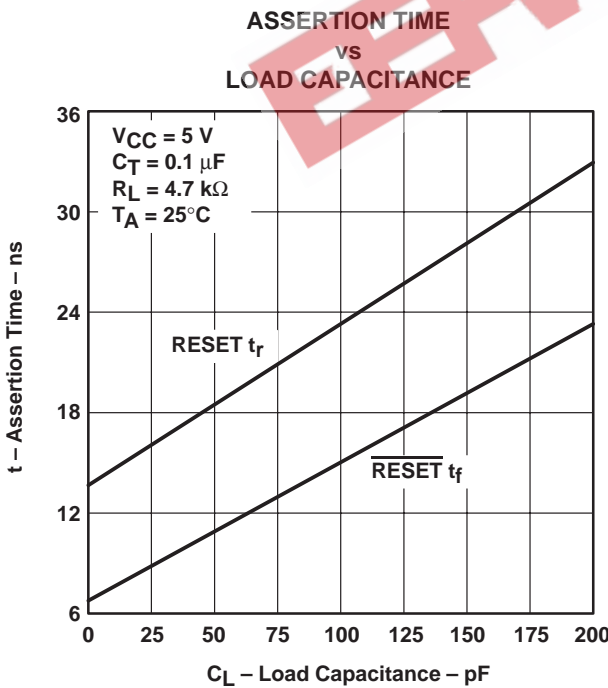
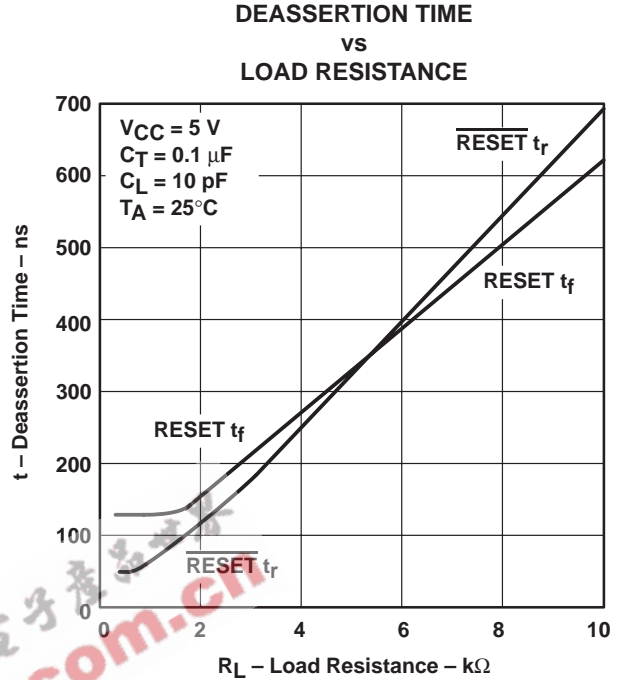
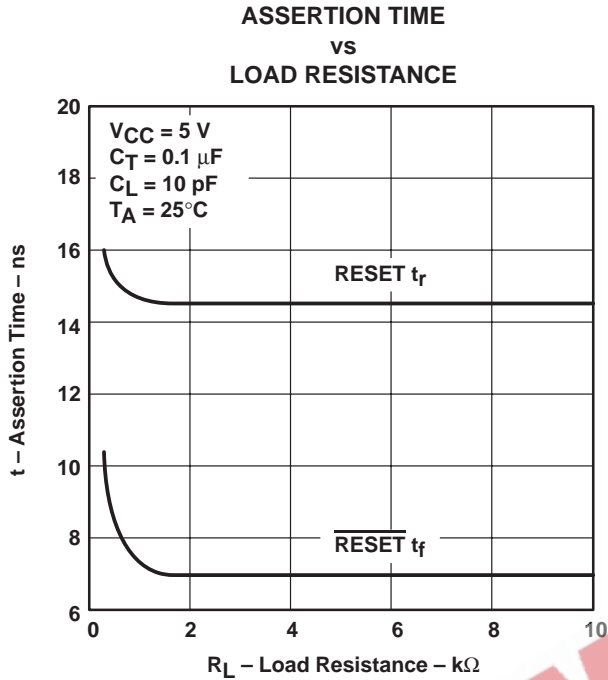


Figure 3. Voltage Waveforms

TYPICAL CHARACTERISTICS†



† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

TL7702B, TL7705B SUPPLY-VOLTAGE SUPERVISORS

SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

APPLICATION INFORMATION

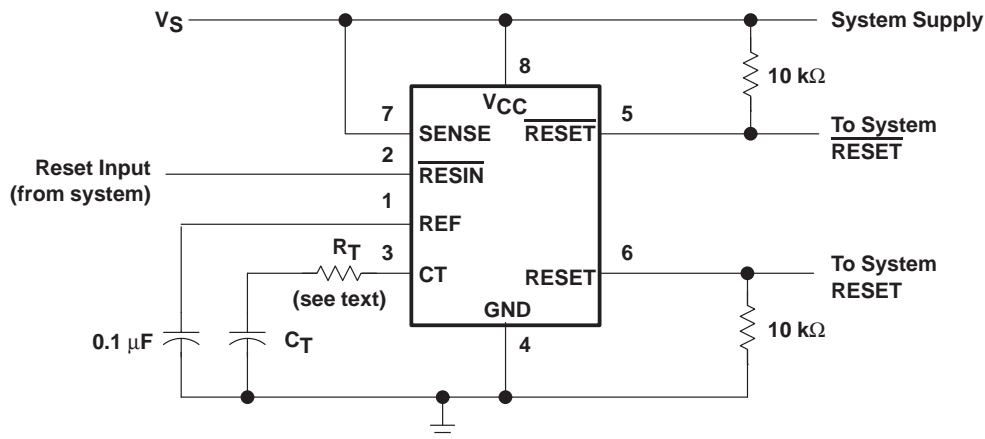


Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC} , a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈ 7.1 -V zener), whichever is less. When the circuit is then subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on C_T exceeds that on V_{CC} . This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-} .

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T , prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T}$$

Where:

$$\begin{aligned} V_{(CT)} &= V_{CC} \text{ or } 7.1 \text{ V, whichever is less} \\ V_{T-} &= 4.55 \text{ V (nom)} \\ R_T &= \text{value of series resistor required} \end{aligned}$$

For $V_{CC} = 5 \text{ V}$:

$$\frac{5 - 4.55}{R_T} < 1 \text{ mA}$$

Therefore,

$$R_T > 450 \ \Omega$$

Using a 20% tolerance resistor, R_T should be greater than 560 Ω .

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T , but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

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