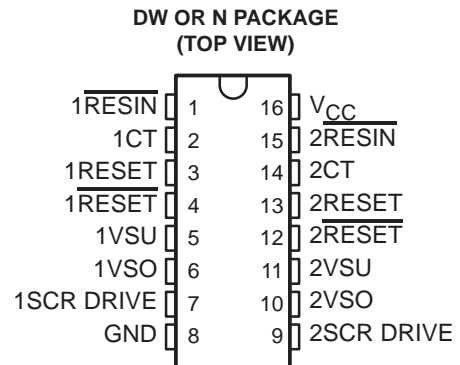


TL7770-5, TL7770-12 DUAL POWER-SUPPLY SUPERVISORS

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- RESET Defined When V_{CC} Exceeds 1 V
- Wide Supply-Voltage Range . . . 3.5 V to 18 V
- Precision Overvoltage and Undervoltage Sensing
- 250-mA Peak Output Current for Driving SCR Gates
- 2-mA Active-Low SCR Gate Drive for False-Trigger Protection
- Temperature-Compensated Voltage Reference
- True and Complementary Reset Outputs
- Externally Adjustable Output Pulse Duration



description

The TL7770 is an integrated-circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power-supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU terminals, respectively. When V_{CC} attains the minimum voltage of 1 V during power up, the RESET output becomes active (low). As V_{CC} approaches 3.5 V, the time-delay function activates, latching RESET and RESET active (high and low, respectively) for a time delay (t_d) after system voltages have achieved normal levels. Above $V_{CC} = 3.5$ V, taking RESIN low activates the time-delay function during normal system-voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value, V_{IT+} , for a time delay, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

The overvoltage-detection circuit is programmable for a wide range of designs. During an overvoltage condition, an internal silicon-controlled rectifier (SCR) is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive terminal, which can drive an external high-current SCR gate or an overvoltage-warning circuit.

The TL7770C series is characterized for operation from 0°C to 70°C. The TL7770I series is characterized for operation from -40°C to 85°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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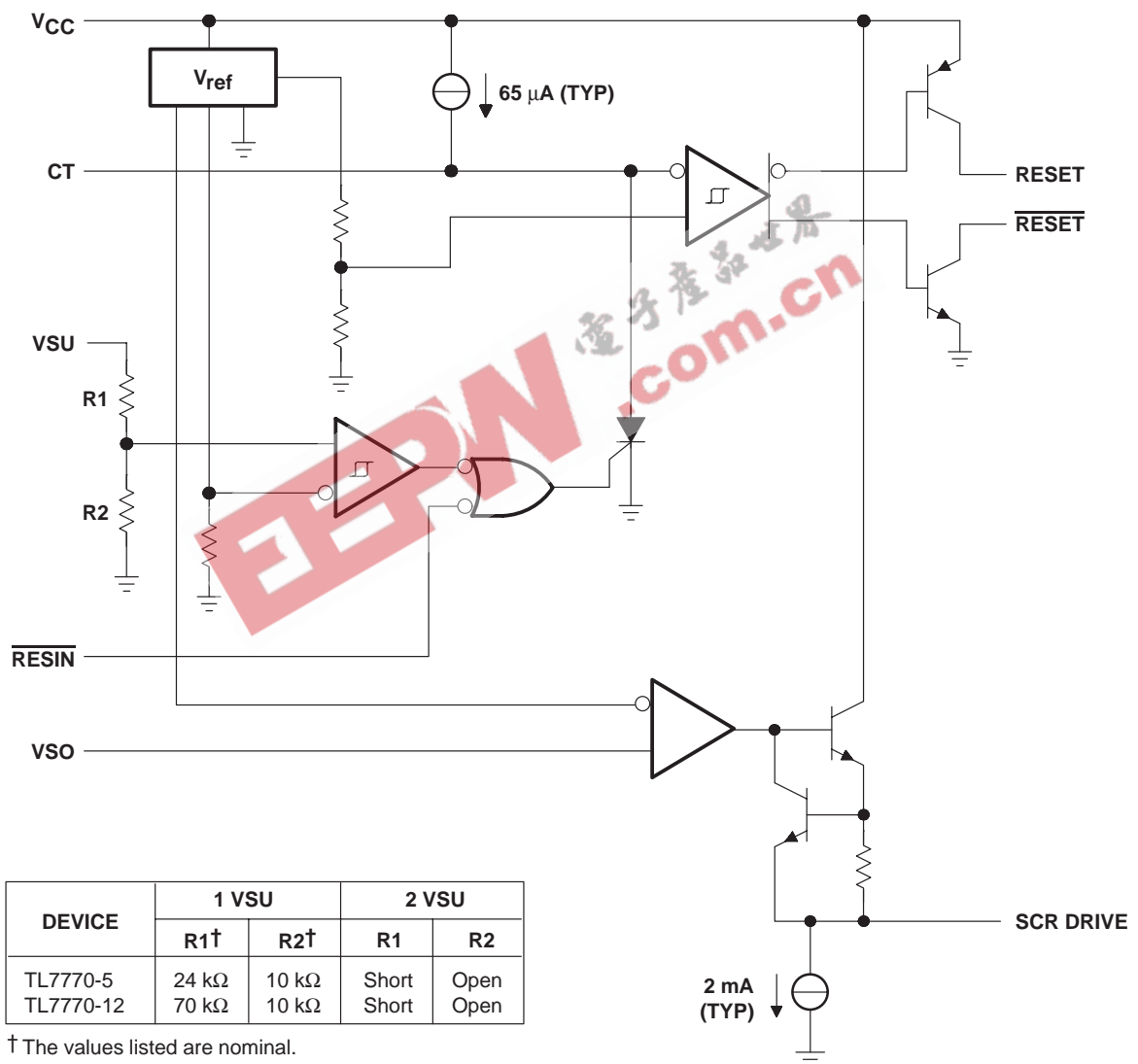
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AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	
0°C to 70°C	TL7770-5CDW TL7770-12CDW	TL7770-5CN TL7770-12CN	TL7770-5Y TL7770-12Y
-40°C to 85°C	TL7770-5IDW	TL7770-5IN	—

DW package is available taped and reeled. Add the suffix R to the device type (e.g., TL7770-5CDWR). Chip forms are tested at 25°C.

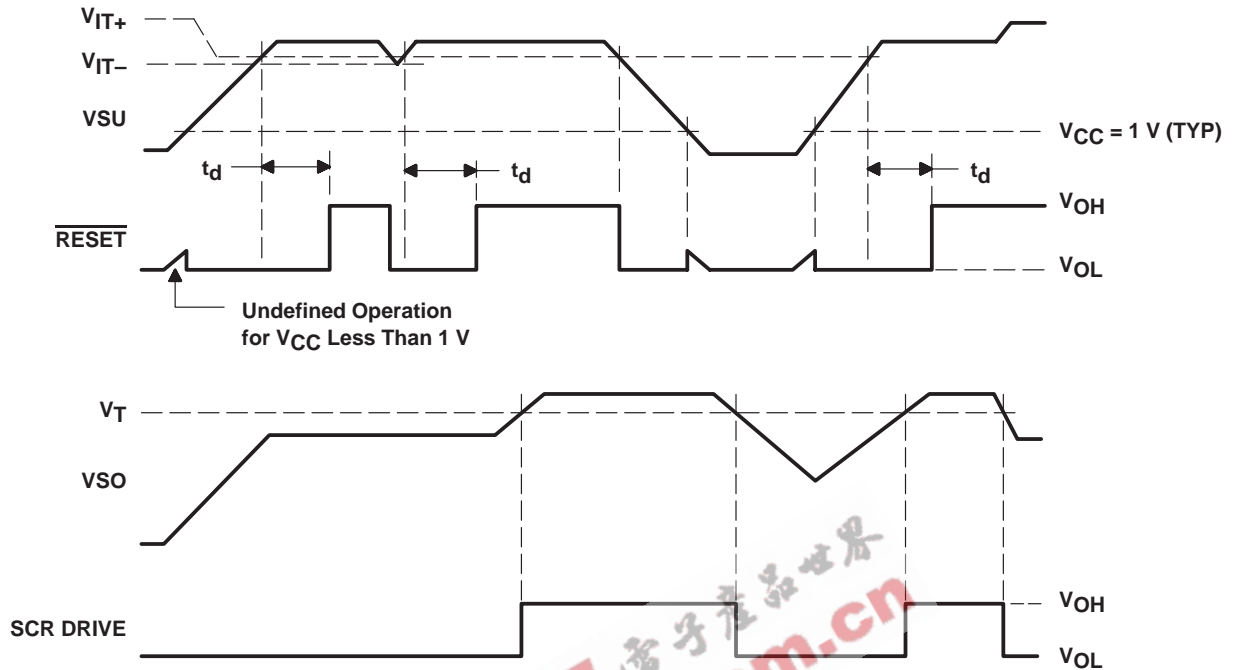
functional block diagram (each channel)



TL7770-5, TL7770-12 DUAL POWER-SUPPLY SUPERVISORS

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

timing requirements



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} (see Note 1)	20 V
Input voltage range, V _I : 1V _{SU} , 2V _{SU} , 1V _{SO} , and 2V _{SO} (see Note 1)	-0.3 V to 18 V
Low-level output current (1RESET and 2RESET), I _{OL}	20 mA
High-level output current (1RESET and 2RESET), I _{OH}	-20 mA
Package thermal impedance, θ _{JA} (see Notes 2 and 3): DW package	57°C/W
N package	88°C/W
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package	260°C
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values are with respect to the network ground terminal.
 - Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can impact reliability.
 - The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

TL7770-5, TL7770-12

DUAL POWER-SUPPLY SUPERVISORS

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 4)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage, V_O (1CT, 2CT)			5	V
High-level input voltage range, V_{IH} (1RESIN, 2RESIN)		2	18	V
Low-level input voltage range, V_{IL} (1RESIN, 2RESIN)		0	0.8	V
Output sink current, I_O (1CT, 2CT)			50	μ A
High-level output current, I_{OH} (1RESET, 2RESET)			-16	mA
Low-level output current, I_{OL} (1RESET, 2RESET)			16	mA
Continuous output current, I_O (1SCR DRIVE, 2SCR DRIVE)			25	mA
Timing capacitor, C_T			10	μ F
Operating free-air temperature, T_A	TL7770C series	0	70	$^{\circ}$ C
	TL7770I series	-40	85	$^{\circ}$ C

NOTE 4: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

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TL7770-5, TL7770-12 DUAL POWER-SUPPLY SUPERVISORS

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER		TEST CONDITIONS†	TL7770-5C TL7770-12C TL7770-5I			UNIT	
			MIN	TYP‡	MAX		
V _{OH}	High-level output voltage	RESET	I _{OH} = -15 mA			V	
		SCR DRIVE	I _{OH} = -20 mA				
V _{OL}	Low-level output voltage	RESET	I _{OL} = 15 mA			V	
V _{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	4.46		4.64	V	
		TL7770-12 (12-V sense, 1VSU)	10.68		11.12		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)	1.47		1.53		
V _{hys}	Hysteresis at VSU (V _{IT+} - V _{IT-})	TL7770-5 (5-V sense, 1VSU)	15			mV	
		TL7770-12 (12-V sense, 1VSU)	36				
		TL7770-5, TL7770-12 (programmable sense, 2VSU)	5				
V _T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T _A = MIN to MAX		2.48	2.68	V
I _I	Input current	RESIN	V _I = 5.5 V or 0.4 V			-10	μA
		VSO	V _I = 2.4 V			0.5	
I _{OH}	High-level output current	RESET	V _O = 18 V			50	μA
I _{OL}	Low-level output current	RESET	V _O = 0			-50	μA
I _{OH}	Peak output current	SCR DRIVE	Duration = 1 ms			250	mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS†	TL7770-5C TL7770-12C TL7770-5I			UNIT	
			MIN	TYP‡	MAX		
V _{res} §	Power-up reset voltage	V _{CC} = VSU	0.8		1	V	
I _{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1RESIN and 2RESIN at V _{CC} , 1VSO and 2VSO at 0 V	T _A = 25°C			5	mA
			T _A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the lowest voltage at which RESET becomes active.

TL7770-5, TL7770-12 DUAL POWER-SUPPLY SUPERVISORS

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER		TEST CONDITIONS	TL7770-5Y TL7770-12Y			UNIT
			MIN	TYP†	MAX	
V _{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T _A = MIN to MAX	4.46	4.64	V
		TL7770-12 (12-V sense, 1VSU)		10.68	11.12	
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		1.47	1.53	
V _{hys}	Hysteresis at VSU (V _{IT+} - V _{IT-})	TL7770-5 (5-V sense, 1VSU)	T _A = MIN to MAX	15		mV
		TL7770-12 (12-V sense, 1VSU)		36		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		5		
V _T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T _A = MIN to MAX	2.48	2.68	V
I _I	Input current	VSO	V _I = 2.4 V	0.5		μA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER	TEST CONDITIONS	TL7770-5Y TL7770-12Y			UNIT
		MIN	TYP†	MAX	
V _{res} ‡	Power-up reset voltage	V _{CC} = VSU, V _{OL} = 0.4 V, I _{OL} = 1 mA		0.8	V
I _{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1RESIN and 2RESIN at V _{CC} , 1VSO and 2VSO at 0 V		5	mA

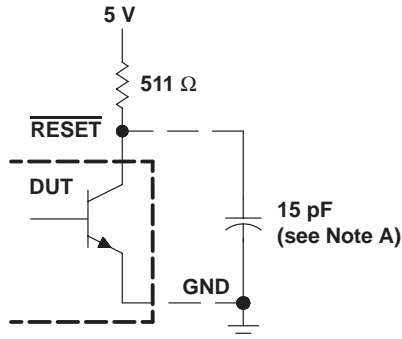
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the lowest voltage at which RESET becomes active.

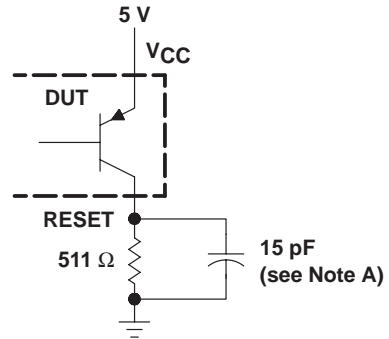
switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1 and 3	270	500		ns
t _{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$		270	500		ns
t _r	Rise time		RESET				75	ns
t _f	Fall time		RESET			150		
t _r	Rise time		$\overline{\text{RESET}}$				75	ns
t _f	Fall time		$\overline{\text{RESET}}$				50	
t _{w(min)}	Minimum effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2a	150		ns	
		VSU		See Figure 2b	100			

PARAMETER MEASUREMENT INFORMATION



RESET OUTPUT CONFIGURATION



RESET OUTPUT CONFIGURATION

NOTE A: This includes jig and probe capacitance.

Figure 1. RESET and RESET Output Configurations

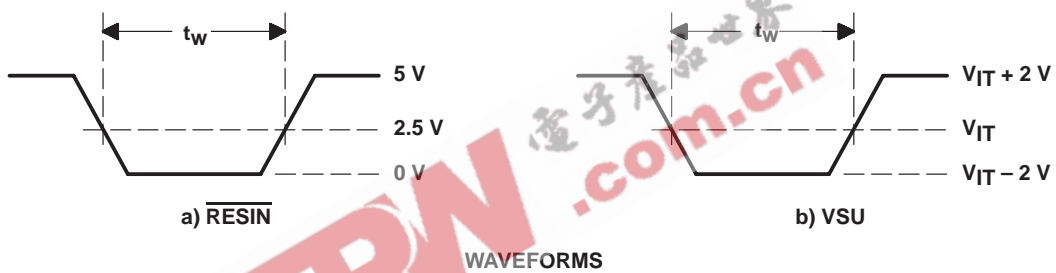


Figure 2. Input Pulse Definition

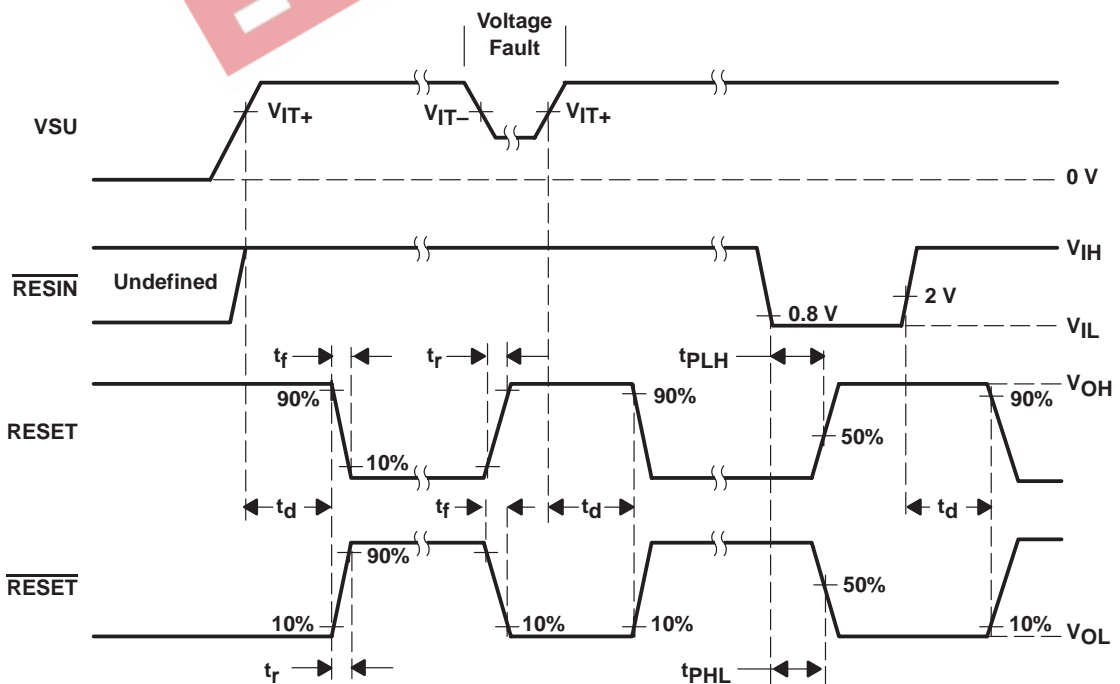
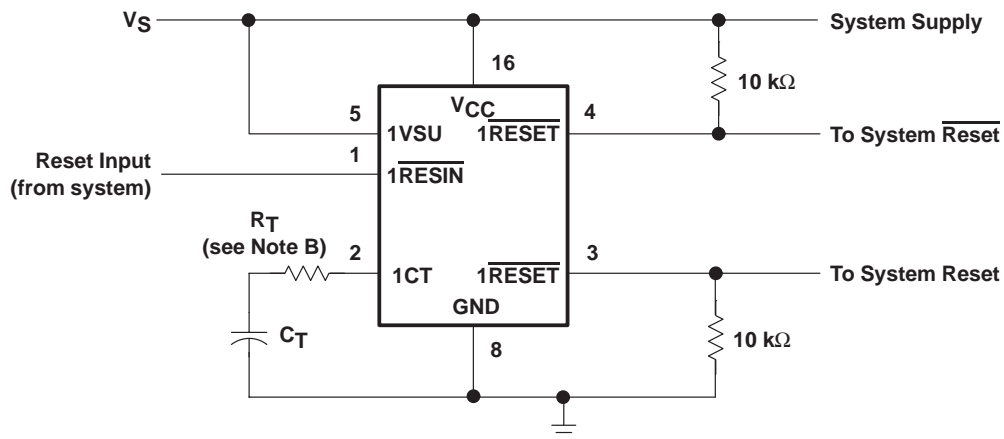


Figure 3. Voltage Waveforms

TL7770-5, TL7770-12 DUAL POWER-SUPPLY SUPERVISORS

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APPLICATION INFORMATION



NOTE B: When V_{CC} and $1VSU$ are connected to the same point, it is recommended that series resistance (R_T) be added between the time-delay programming capacitor (C_T) and the voltage-supervisor device terminal ($1CT$). The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{IT-}}{1 \times 10^{-3}}, \text{ where } V_I = (\text{the lesser of } 7.1 \text{ V or } V_S)$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - [(6.5E - 5) \times 10^{-5}] \times R_T}{6.5 \times 10^{-5}} \times C_T$$

Figure 4. System Reset Controller With Undervoltage Sensing

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