

TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

SLOS437G – APRIL 2004 – REVISED DECEMBER 2004

OPERATIONAL AMPLIFIER

- **Low Offset Voltage Max of:**
 - TL103WA . . . 3 mV (25°C) and 5 mV (Full Temperature)
 - TL103W . . . 4 mV (25°C) and 5 mV (Full Temperature)
- **Low Supply Current . . . 350 μ A/Channel (Typ)**
- **Unity Gain Bandwidth . . . 0.9 MHz (Typ)**
- **Input Common-Mode Range Includes GND**
- **Large Output-Voltage Swing . . . 0 V to $V_{CC} - 1.5$ V**
- **Wide Supply-Voltage Range . . . 3 V to 32 V**
- **2-kV ESD Protection (HBM)**

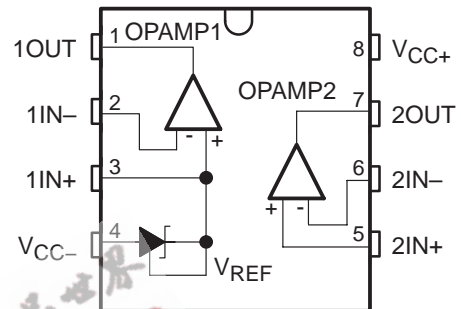
VOLTAGE REFERENCE

- **Fixed 2.5-V Reference**
- **Tight Tolerance Max of:**
 - TL103WA . . . 0.4% (25°C) and 0.8% (Full Temperature)
 - TL103W . . . 0.7% (25°C) and 1.4% (Full Temperature)
- **Low Temperature Drift . . . 7 mV (Typ) Over Operating Temperature Range**
- **Wide Sink-Current Range . . . 0.5 mA (Typ) to 100 mA**
- **Output Impedance . . . 0.2 Ω (Typ)**

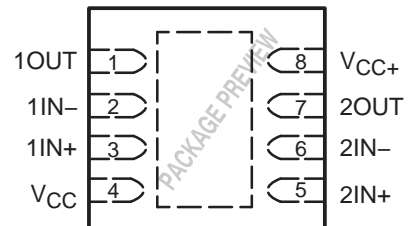
TYPICAL APPLICATIONS

- **Battery Charger**
- **Switch-Mode Power Supply**
- **Linear Voltage Regulation**
- **Data-Acquisition Systems**

D (SOIC) PACKAGE
(TOP VIEW)



DRJ (QFN) PACKAGE
(TOP VIEW)



description/ordering information

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference — both of which often are used in the control circuitry of both switch-mode and linear power supplies. OPAMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OPAMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from -40°C to 105°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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ORDERING INFORMATION

T_A	MAX V_{IO} AND V_{REF} TOLERANCE (25°C)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	A grade 3 mV, 0.4%	QFN (DRJ)	Reel of 1000	TL103WAIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WAID	Z103WA
			Reel of 2500	TL103WAIDR	
	Standard grade 4 mV, 0.7%	QFN (DRJ)	Reel of 1000	TL103WIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WID	Z103W
			Reel of 2500	TL103WIDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	36 V
Operational amplifier input differential voltage, V_{id}	36 V
Operational amplifier input voltage range, V_I	–0.3 V to 36 V
Voltage reference cathode current, I_{KA}	100 mA
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package	97°C/W
(see Notes 1 and 3): DRJ package	TBD°C/W
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions

	MIN	MAX	UNIT
V_{IN} Supply voltage	3	32	V
I_K Cathode current	1	100	mA
T_A Operating free-air temperature	–40	105	°C

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typical application circuit

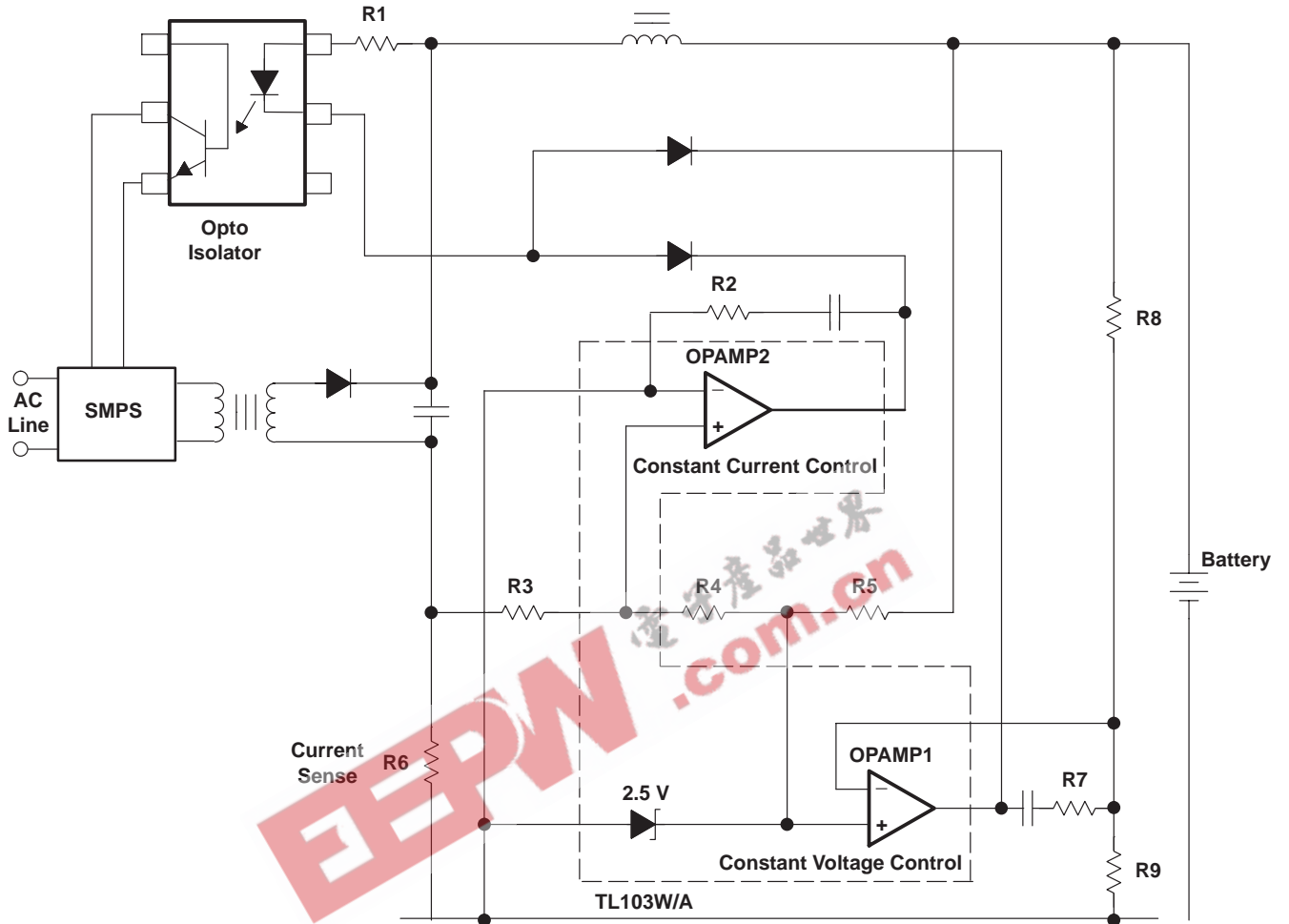


Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger

TL103W, TL103WA

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OPAMP1, operational amplifier with noninverting input connected to the internal V_{REF} electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{icm} = 0\text{ V}$	25°C		1	4	mV
			Full range			5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C		0.5	3	
			Full range			5	
∞V_{IO}	Input offset-voltage drift		25°C		7	$\mu\text{V}/^\circ\text{C}$	
I_{IB}	Input bias current (negative input)		25°C		20	nA	
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{icm} = 0\text{ V}$	25°C		100		V/mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V , $V_{icm} = 0\text{ V}$	25°C	65	100		dB
I_{source}	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$	25°C	20	40		mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
I_{sink}	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$		12	50		μA
V_{OH}	High-level output voltage	$V_{CC+} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range		26		
		$V_{CC+} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	27	28		
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 2 V , unity gain	25°C	0.2	0.4		V/ μs
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_V = 20\text{ dB}$	25°C		0.02		%

TL103W, TL103WA

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OPAMP2, independent operational amplifier
electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $V_O = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TL103W	$V_{icm} = 0\text{ V}$	25°C	1	4	mV
				Full range		5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C	0.5	3		
			Full range		5		
∞V_{IO}	Input offset voltage drift		25°C	7		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current			25°C	2	75	nA
				Full range		150	
I_{IB}	Input bias current			25°C	20	150	nA
				Full range		200	
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1.4\text{ V}$ to 11.4 V		25°C	50	100	V/mV
				Full range		25	
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V		25°C	65	100	dB
V_{ICR}	Input common-mode voltage range	$V_{CC+} = 30\text{ V}$ (see Note 4)		25°C	0	$(V_{CC+}) - 1.5$	V
				Full range	0	$(V_{CC+}) - 2$	
$CMRR$	Common-mode rejection ratio			25°C	70	85	dB
				Full range		60	
I_{source}	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$		25°C	20	40	mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$		25°C	40	60	mA
I_{sink}	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$		25°C	10	12	mA
					$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$	12	
V_{OH}	High-level output voltage	$V_{CC+} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$		25°C	26	27	V
				Full range		26	
				25°C	27	28	
				Full range		27	
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$		25°C	5	20	mV
				Full range		20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 3 V , unity gain		25°C	0.2	0.4	$\text{V}/\mu\text{s}$
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$,		25°C	0.5	0.9	MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_v = 20\text{ dB}$		25°C	0.02		%
V_n	Equivalent input noise voltage	$V_{CC} = 30\text{ V}$, $R_S = 100\ \Omega$, $f = 1\text{ kHz}$			50		$\text{nV}/\sqrt{\text{Hz}}$

NOTE 4: The input common-mode voltage of either input should not be allowed to go below -0.3 V . The upper end of the common-mode voltage range is $(V_{CC+}) - 1.5\text{ V}$, but either input can go to $(V_{CC+}) + 0.3\text{ V}$ (but $\leq 36\text{ V}$) without damage.

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VOLTAGE REFERENCE electrical characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
V _{REF}	Reference voltage	I _K = 10 mA	25°C	2.482	2.5	2.518	V
			Full range	2.465		2.535	
	TL103WA	I _K = 10 mA	25°C	2.49	2.5	2.51	
			Full range	2.48		2.52	
ΔV _{REF}	Reference input voltage deviation over temperature range	V _{KA} = V _{REF} , I _K = 10 mA	Full range		7	30	mV
I _{min}	Minimum cathode current for regulation	V _{KA} = V _{REF}	25°C		0.5	1	mA
z _{ka}	Dynamic impedance (see Note 5)	V _{KA} = V _{REF} , ΔI _K = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω

NOTE 5: The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$.

TOTAL DEVICE electrical characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{CC}	Total supply current, excluding cathode-current reference	V _{CC+} = 5 V, No load	Full range		0.7	1.2	mA
		V _{CC+} = 30 V, No load					

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL103WAID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL103WID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL103WIDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

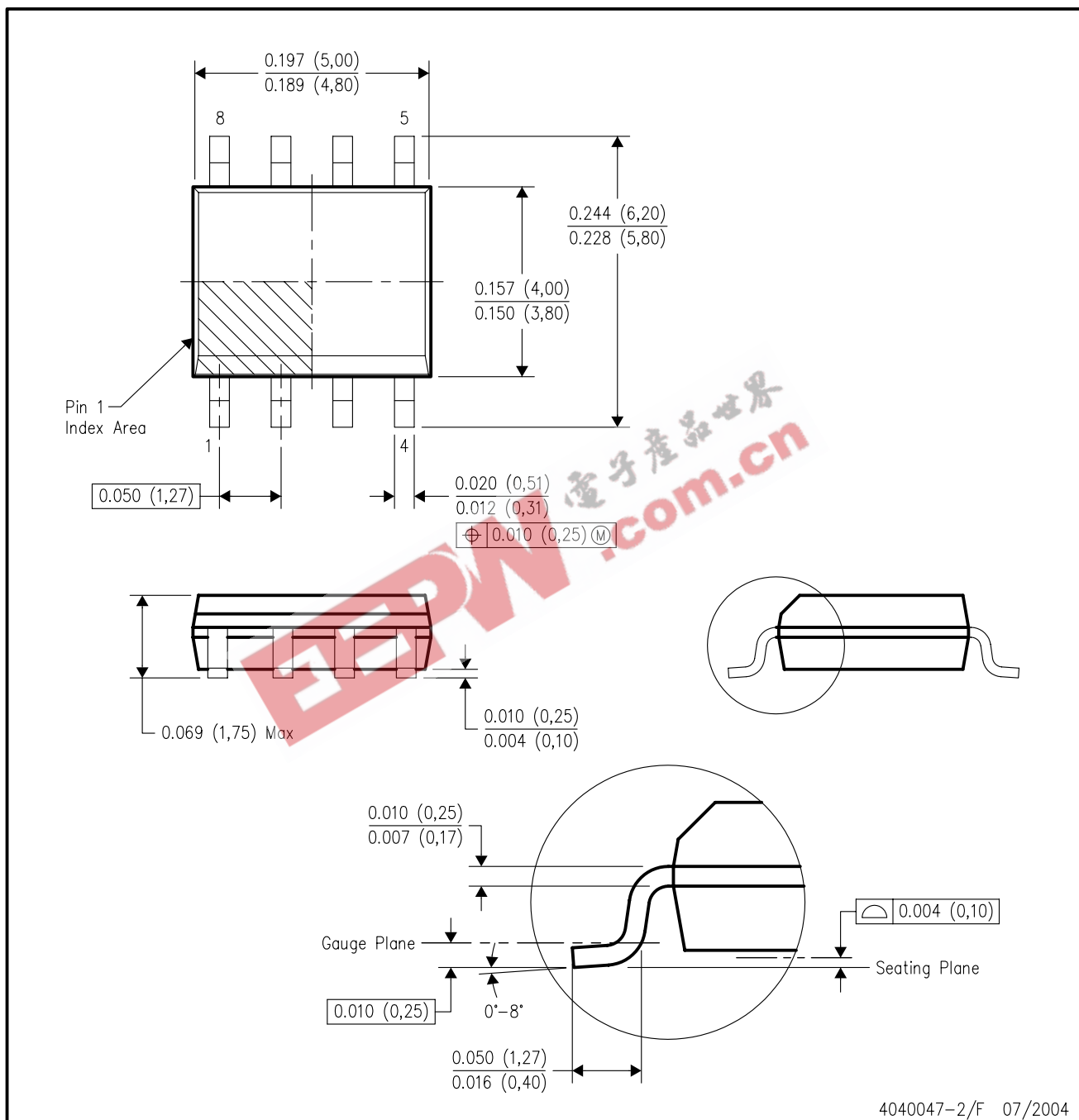
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MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-2/F 07/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

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