

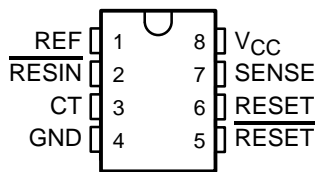
TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

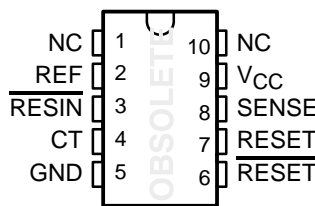
The TL7705BM is obsolete and no longer is supplied.

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- RESET Output Defined From $V_{CC} \geq 1\text{ V}$
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Duration

TL77xxBC . . . D OR P PACKAGE
TL7705BM . . . JG PACKAGE
TL7705BQ . . . D PACKAGE
(TOP VIEW)

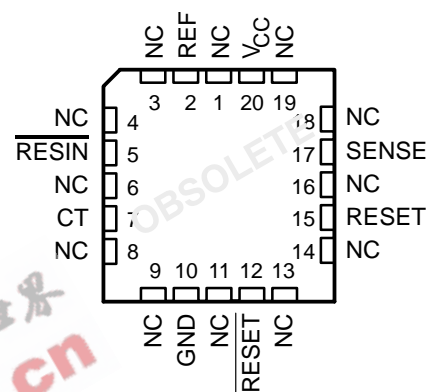


TL7705BM . . . U PACKAGE
(TOP VIEW)



NC – No internal connection

TL7705BM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the RESET output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs RESET and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs RESET and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC, TL7705BC, and TL7733BC are characterized for operation from 0°C to 70°C. The TL7702BI, TL7705BI, and TL7733BI are characterized for operation from –40°C to 85°C. The TL7705BQ is characterized for operation from –40°C to 125°C. The TL7705BM is characterized for operation from –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

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description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL7702BCP	TL7702BCP
	SOIC (D)	Tube of 75	TL7702BCD	7702BC
		Reel of 2500	TL7702BCDR	
	PDIP (P)	Tube of 50	TL7705BCP	TL7705BCP
	SOIC (D)	Tube of 75	TL7705BCD	7705BC
		Reel of 2500	TL7705BCDR	
SOIC (D)	Tube of 75	TL7733BCD	7733BC	
	Reel of 2500	TL7733BCDR		
-40°C to 85°C	PDIP (P)	Tube of 50	TL7702BIP	TL7702BIP
	SOIC (D)	Tube of 75	TL7702BID	7702BI
		Reel of 2500	TL7702BIDR	
	PDIP (P)	Tube of 50	TL7705BIP	TL7705BIP
	SOIC (D)	Tube of 75	TL7705BID	7705BI
		Reel of 2500	TL7705BIDR	
SOIC (D)	Tube of 75	TL7733BID	7733BI	
	Reel of 2500	TL7733BIDR		
-40°C to 125°C	SOIC (D)	Tube of 75	TL7705BQD	TL7705BQD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

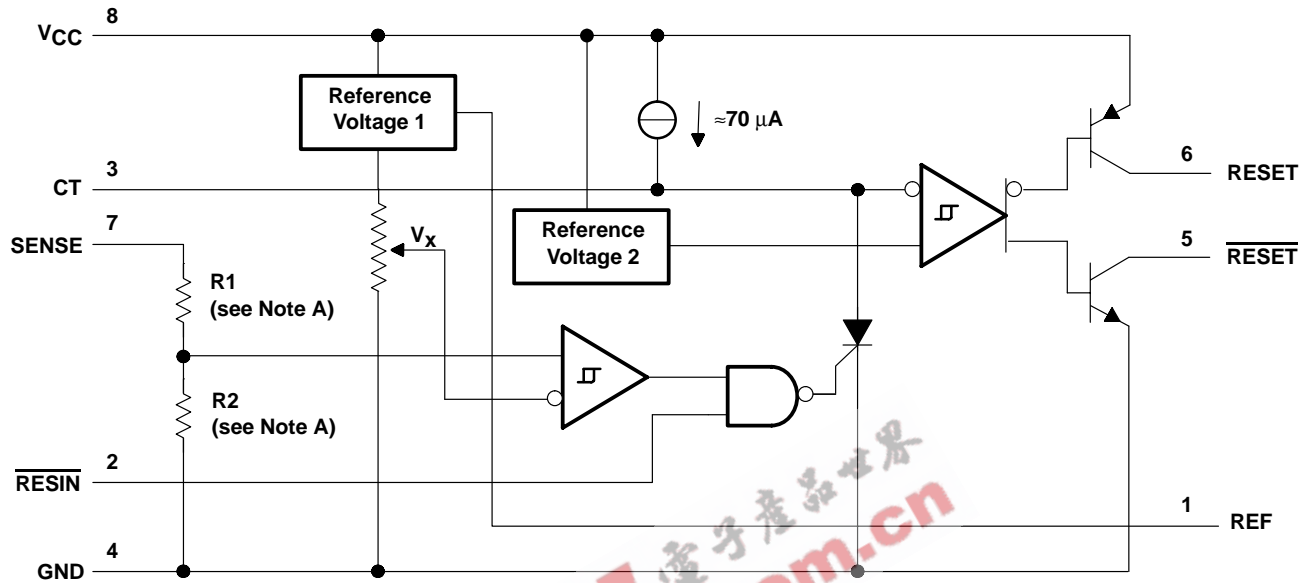
TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

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functional block diagram

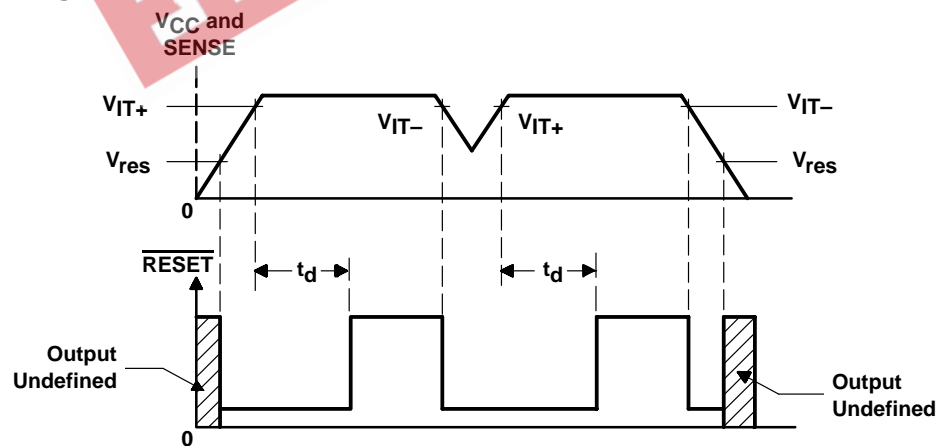
The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



Pin numbers shown are for the D, JG, and P packages.

NOTE A: TL7702B: R1 = 0 Ω, R2 = open, $V_x = V_{REF1}$
 TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal, $V_x \approx 1.43$ V
 TL7733B: R1 = 11.3 kΩ, R2 = 10 kΩ, nominal, $V_x \approx 1.43$ V

typical timing diagram



TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I : $\overline{\text{RESIN}}$	-0.3 V to 20 V
SENSE	-0.3 V to 20 V
High-level output current, I_{OH} (RESET)	-30 mA
Low-level output current, I_{OL} (RESET)	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or U packages	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the network ground terminal.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	3.6	18	V	
V_{IH}	High-level input voltage	$\overline{\text{RESIN}}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{\text{RESIN}}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET	-20	mA	
I_{OL}	Low-level output current	RESET	20	mA	
T_A	Operating free-air temperature range	TL77xxBC	0	70	°C
		TL77xxBI	-40	85	
		TL7705BQ	-40	125	
		TL7705BM	-55	125	

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL77xxBC TL77xxBI TL7705BQ			UNIT	
			MIN	TYP	MAX		
V _{OH}	High-level output voltage, RESET	I _{OH} = -16 mA	V _{CC} -1.5			V	
V _{OL}	Low-level output voltage, RESET	I _{OL} = 16 mA	0.4			V	
V _{ref}	Reference voltage, REF	I _{ref} = -500 µA, T _A = 25°C	2.48	2.53	2.58	V	
V _{IT-}	Negative-going input threshold voltage at SENSE input	T _A = 25°C	TL7702B	2.505	2.53	2.555	V
			TL7705B	4.5	4.55	4.6	
			TL7733B	3.03	3.08	3.13	
		T _A = full range‡	TL7702B	2.48	2.53	2.58	
			TL7705B	4.45	4.55	4.65	
			TL7733B	3	3.08	3.16	
V _{hys}	Hysteresis, SENSE (V _{IT+} - V _{IT-})	V _{CC} = 3.6 V to 18 V, T _A = 25°C	TL7702B	10		mV	
			TL7705B	30			
			TL7733B	10			
V _{res} §	Power-up reset voltage	I _{OL} at RESET = 2 mA, T _A = 25°C	1			V	
I _I	Input current	RESIN	V _I = 0.4 V to V _{CC}			-10	µA
		SENSE TL7702B	V _I = V _{ref} to 18 V			-0.1 -2	
I _{OH}	High-level output current, RESET	V _O = 18 V, See Figure 1	50			µA	
I _{OL}	Low-level output current, RESET	V _O = 0 V, See Figure 1	-50			µA	
I _{CC}	Supply current	V _{SENSE} = 15 V, RESIN ≥ 2 V	1.8		3	mA	
		V _{CC} = 18 V, T _A = full range‡	3.5				

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

‡ Full range is 0°C to 70°C for the C-suffix devices, -40°C to 85°C for the I-suffix devices, and -40°C to 125°C for the Q-suffix device.

§ This is the lowest voltage at which RESET becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC TL77xxBI TL7705BQ			UNIT
				MIN	TYP	MAX	
t _{PLH}	RESIN	RESET	See Figures 1, 2, and 3	270	500	ns	
t _{PHL}	RESIN	RESET	See Figures 1, 2, and 3	270	500	ns	
t _w	RESIN		See Figure 2	150		ns	
	SENSE			100			
t _r		RESET	See Figures 1 and 3	75		ns	
t _f				150 200			
t _r		RESET	See Figures 1 and 3	75 150		ns	
t _f				50			

TL7702B, TL7705B, TL7733B SUPPLY-VOLTAGE SUPERVISORS

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SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL7705BM			UNIT
				MIN	TYP	MAX	
V _{OH}	High-level output voltage, $\overline{\text{RESET}}$	I _{OH} = -16 mA		V _{CC} -1.5			V
V _{OL}	Low-level output voltage, $\overline{\text{RESET}}$	I _{OL} = 16 mA		0.4			V
V _{ref}	Reference voltage, REF	I _{ref} = -500 μ A, T _A = 25°C		2.48	2.53	2.58	V
V _{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	T _A = 25°C	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7702B	T _A = -55°C to 125°C	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
V _{hys}	Hysteresis, SENSE (V _{IT+} - V _{IT-})	TL7702B	V _{CC} = 3.6 V to 18 V, T _A = 25°C	10		mV	
TL7705B	30						
V _{res} ‡	Power-up reset voltage	I _{OL} at $\overline{\text{RESET}}$ = 2 mA, T _A = 25°C		1			V
I _I	Input current	$\overline{\text{RESIN}}$		V _I = 0.4 V to V _{CC}			μ A
		SENSE	TL7702B	V _I = V _{ref} to V _{CC} - 1.5 V			
I _{OH}	High-level output current, $\overline{\text{RESET}}$	V _O = 18 V		50			μ A
I _{OL}	Low-level output current, $\overline{\text{RESET}}$	V _O = 0		-50			μ A
I _{CC}	Supply current	V _{SENSE} = 15 V, $\overline{\text{RESIN}} \geq 2$ V		1.8		3	mA
		V _{CC} = 18 V, T _A = -55°C to 125°C		4			

† All electrical characteristics are measured with 0.1- μ F capacitors connected at REF, CT, and V_{CC} to GND.

‡ This is the lowest value at which $\overline{\text{RESET}}$ becomes active.

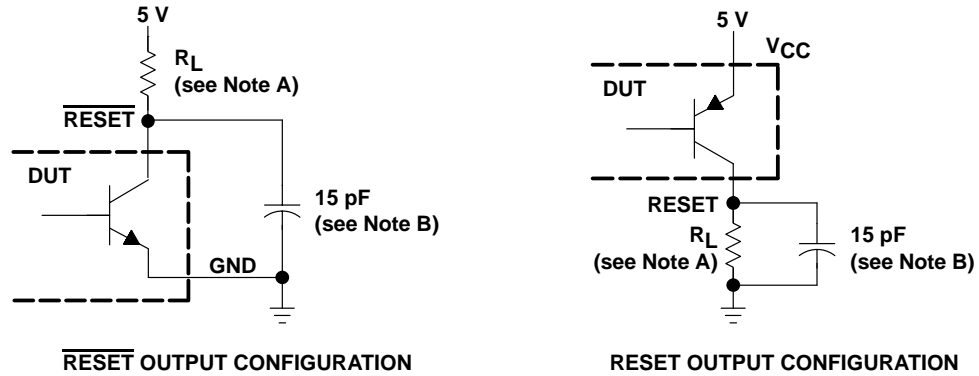
switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7705BM			UNIT
					MIN	TYP	MAX	
t _{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3	270	500*	ns	
t _{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See Figures 1, 2, and 3	270	500*	ns	
t _w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2	150		ns	
		SENSE			100			
t _r	Rise time		RESET	See Figures 1 and 3	75*		ns	
t _f	Fall time				150 200*			
t _r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3	75 150*		ns	
t _f	Fall time				50*			

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

The TL7705BM is obsolete and no longer is supplied.

PARAMETER MEASUREMENT INFORMATION

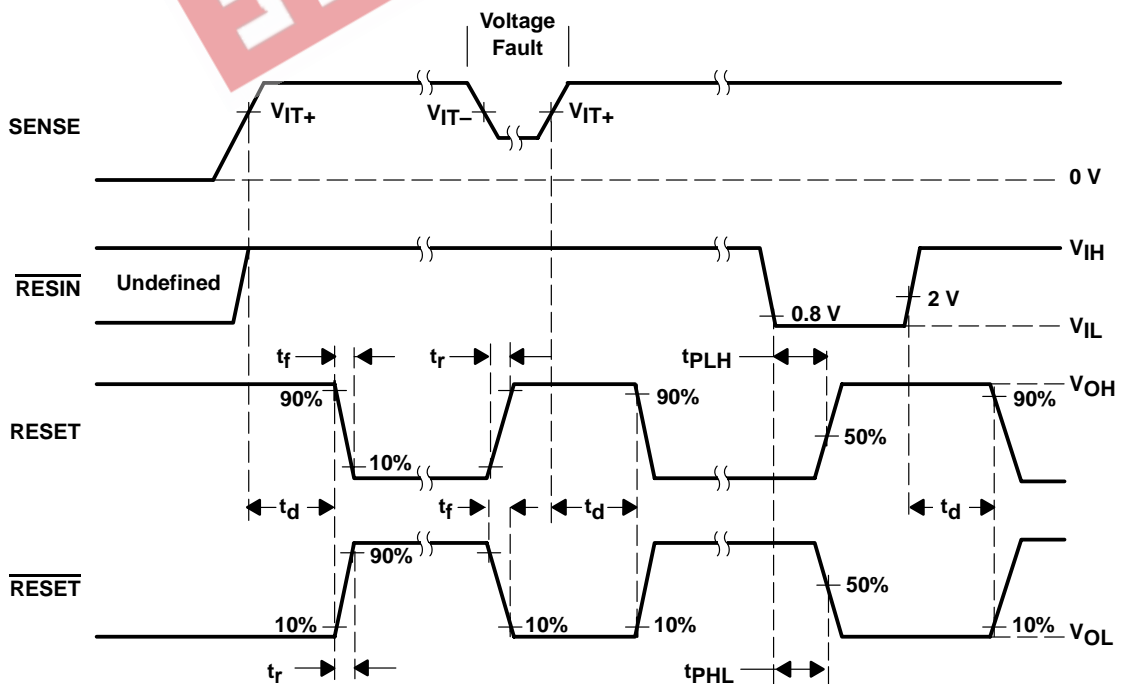


NOTES: A. For I_{OL} and I_{OH} , $R_L = 10\text{ k}\Omega$. For all switching characteristics, $R_L = 511\ \Omega$.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations



Figure 2. Input Pulse Definition

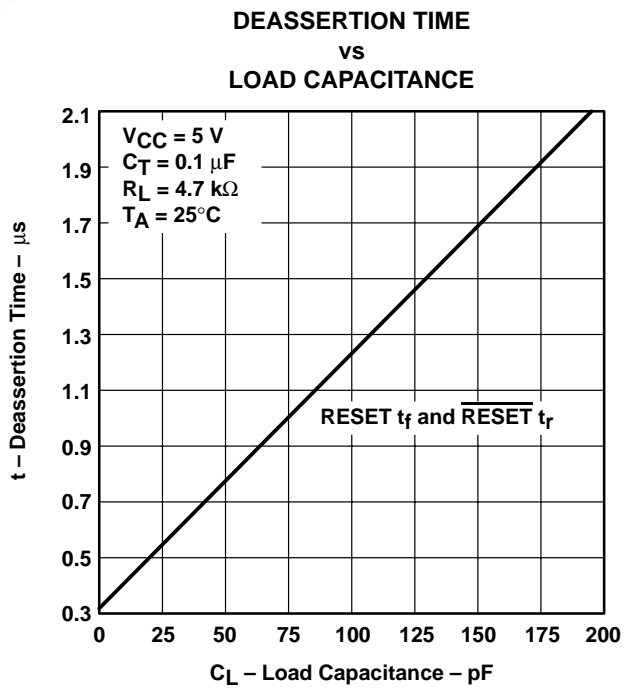
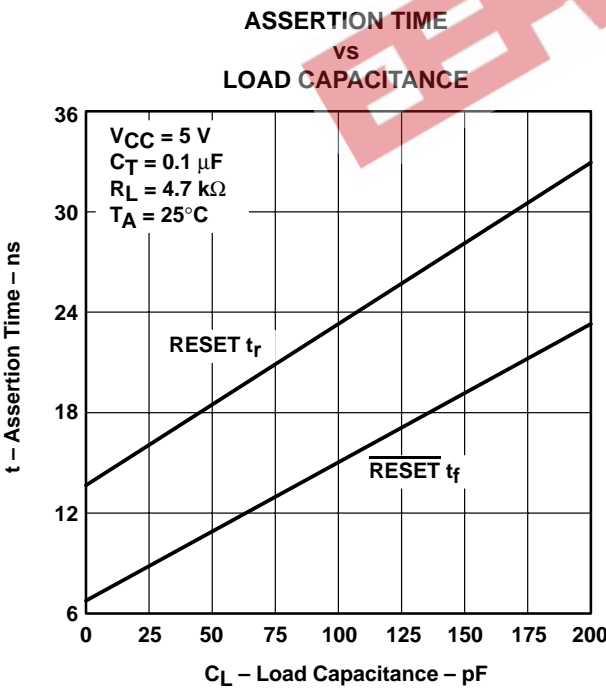
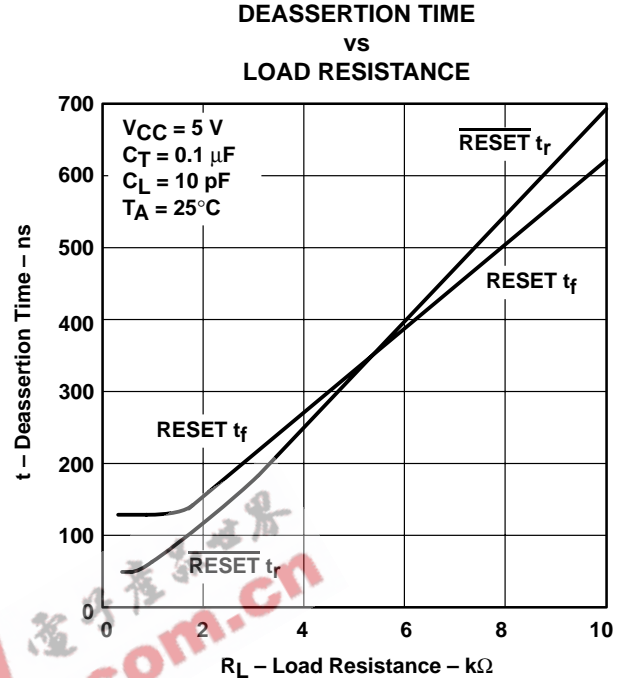
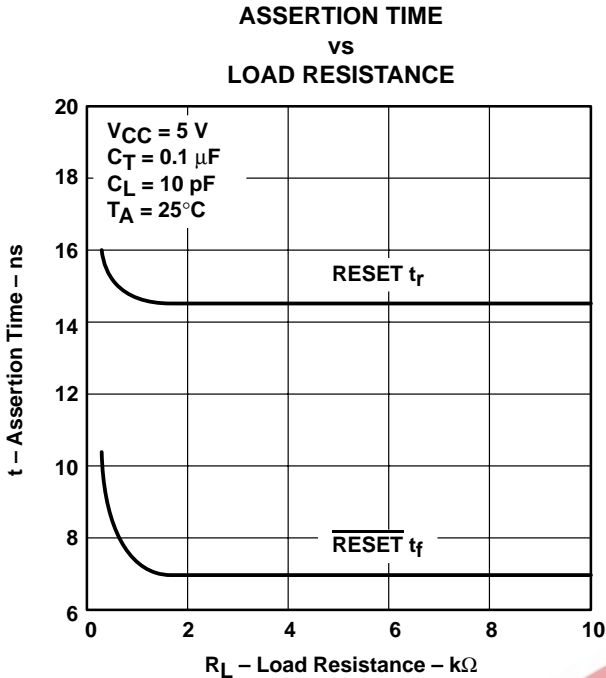


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SLVS037M – SEPTEMBER 1989 – REVISED MAY 2003

TYPICAL CHARACTERISTICS†



† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

The TL7705BM is obsolete
and no longer is supplied.

APPLICATION INFORMATION

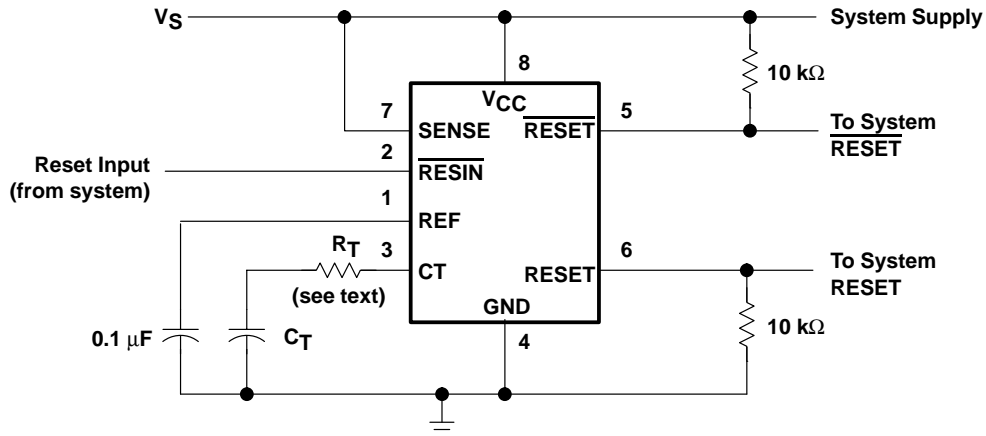


Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC} , a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈ 7.1 -V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC} . This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-} .

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T , prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T}$$

Where:

- $V_{(CT)}$ = V_{CC} or 7.1 V, whichever is less
- V_{T-} = 4.55 V (nom)
- R_T = value of series resistor required

For $V_{CC} = 5$ V:

$$\frac{5 - 4.55}{R_T} < 1 \text{ mA}$$

Therefore,

$$R_T > 450 \ \Omega$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω .

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T , but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

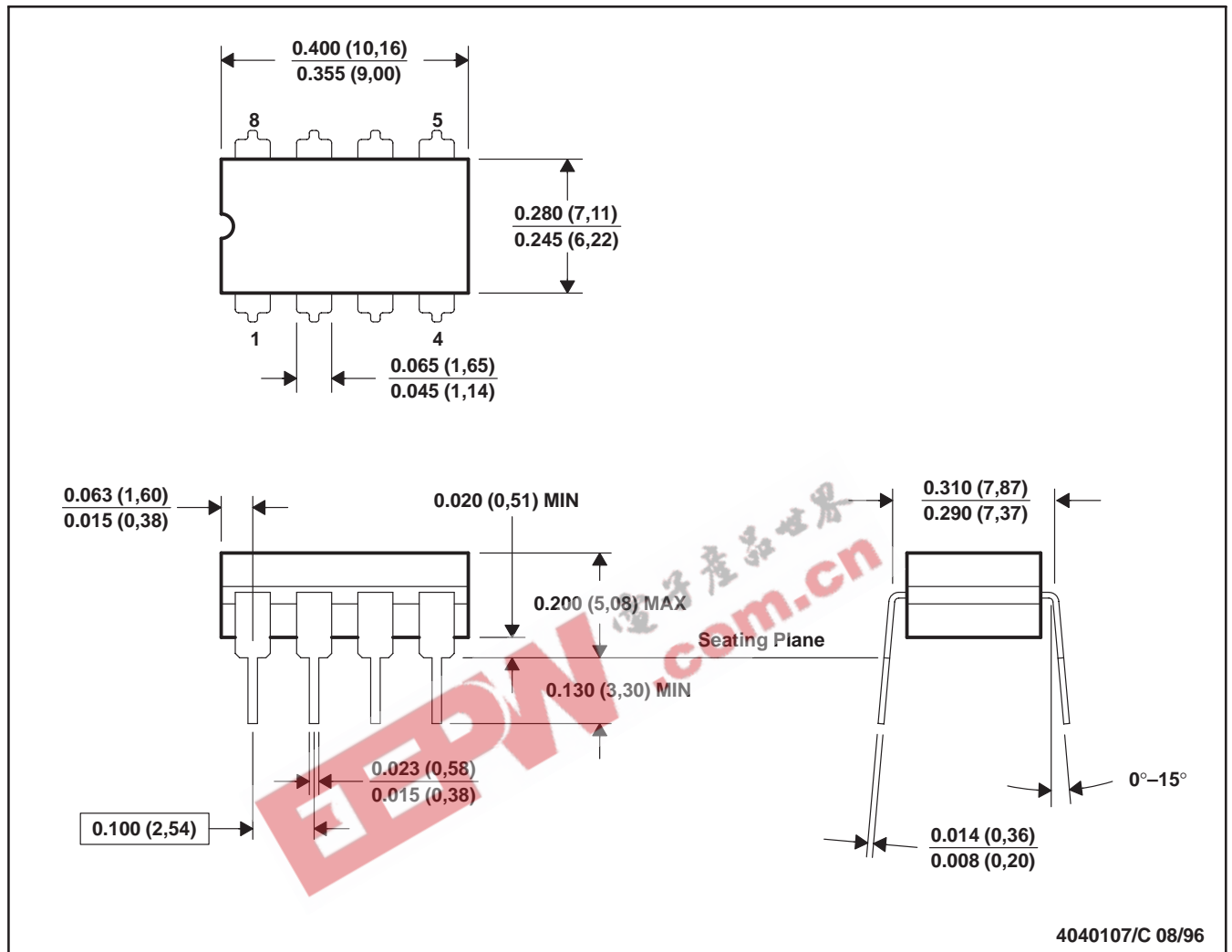
Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

MECHANICAL DATA

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



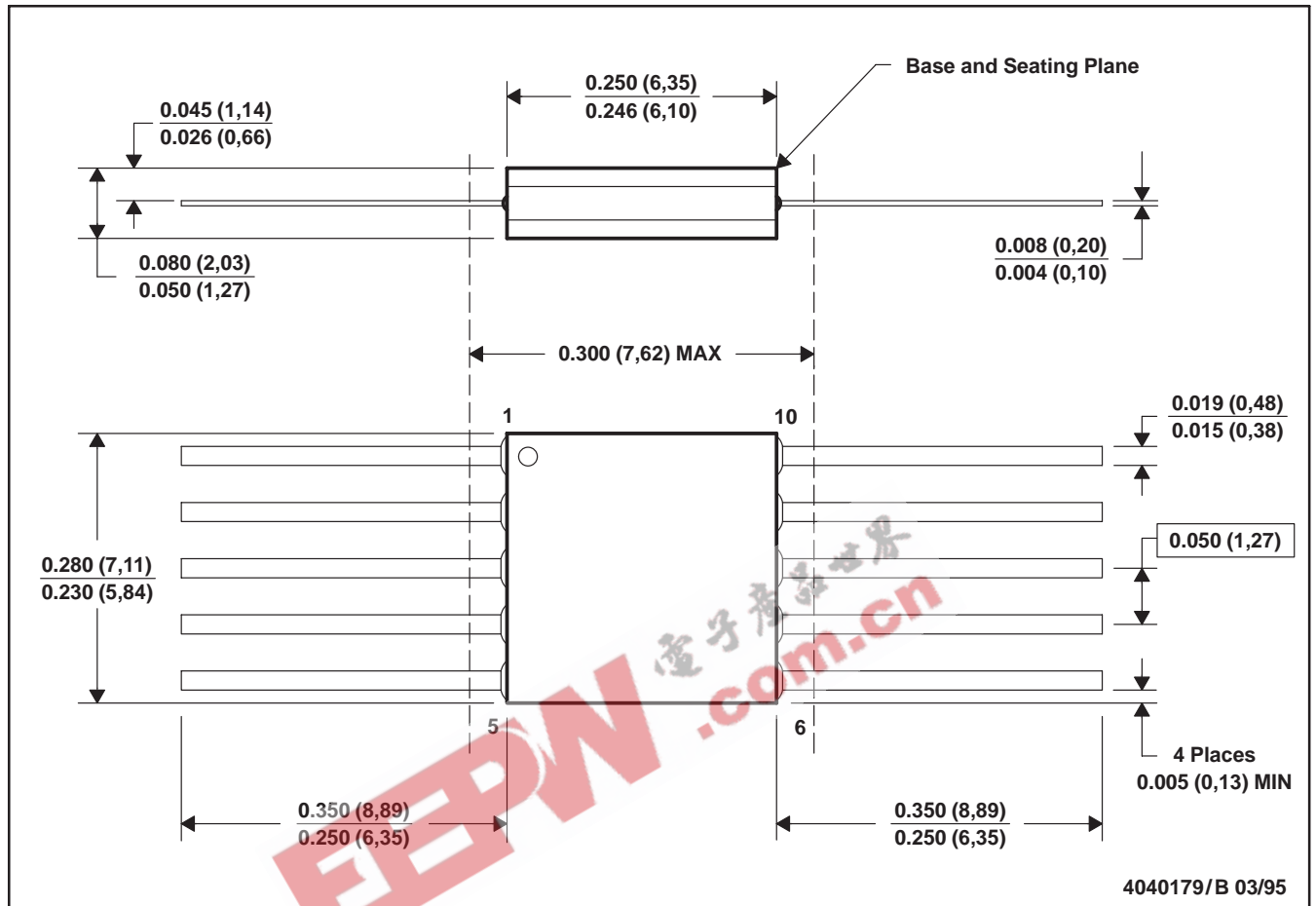
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

MECHANICAL DATA

MCFP001A – JANUARY 1995 – REVISED DECEMBER 1995

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK

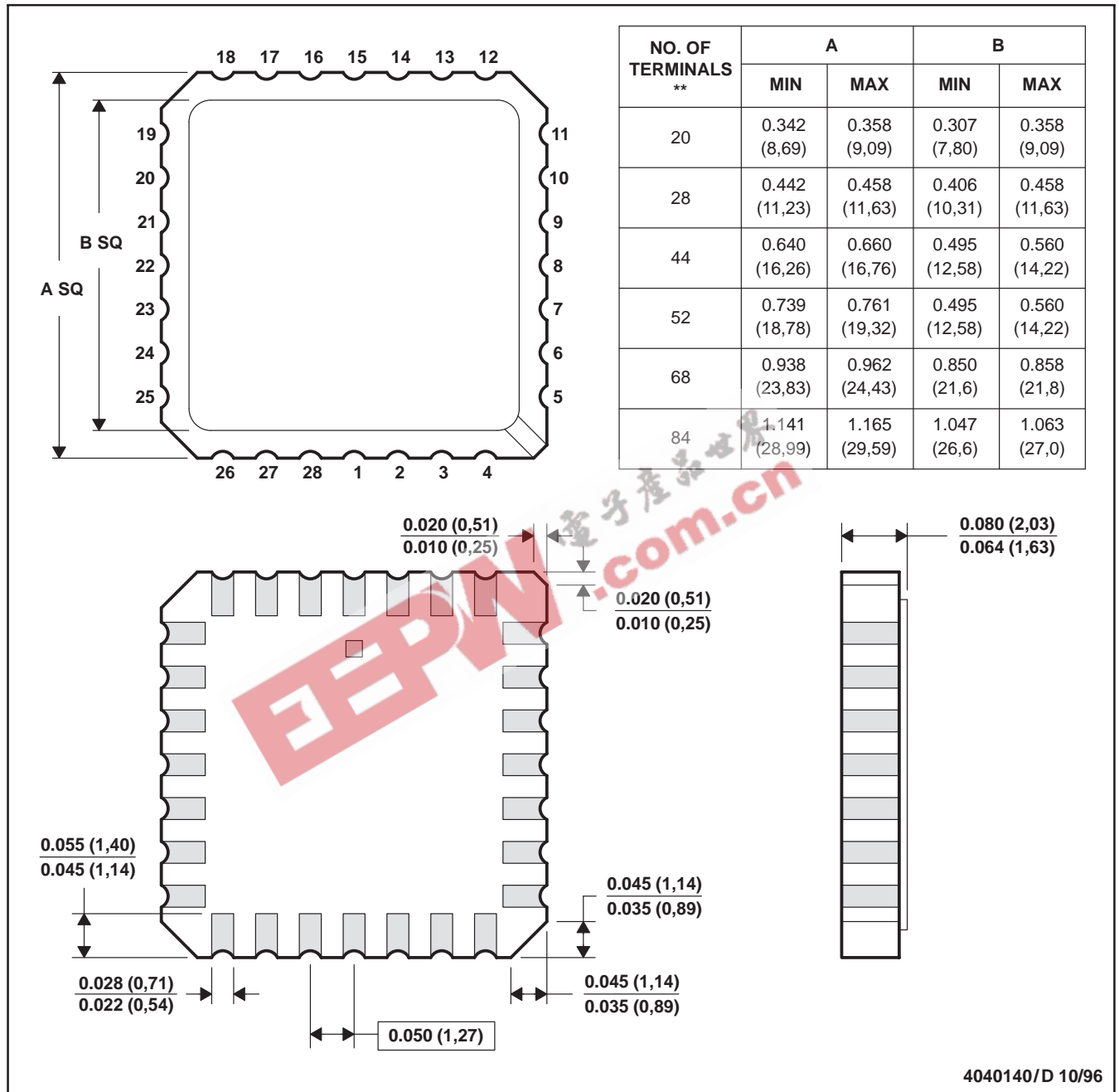


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



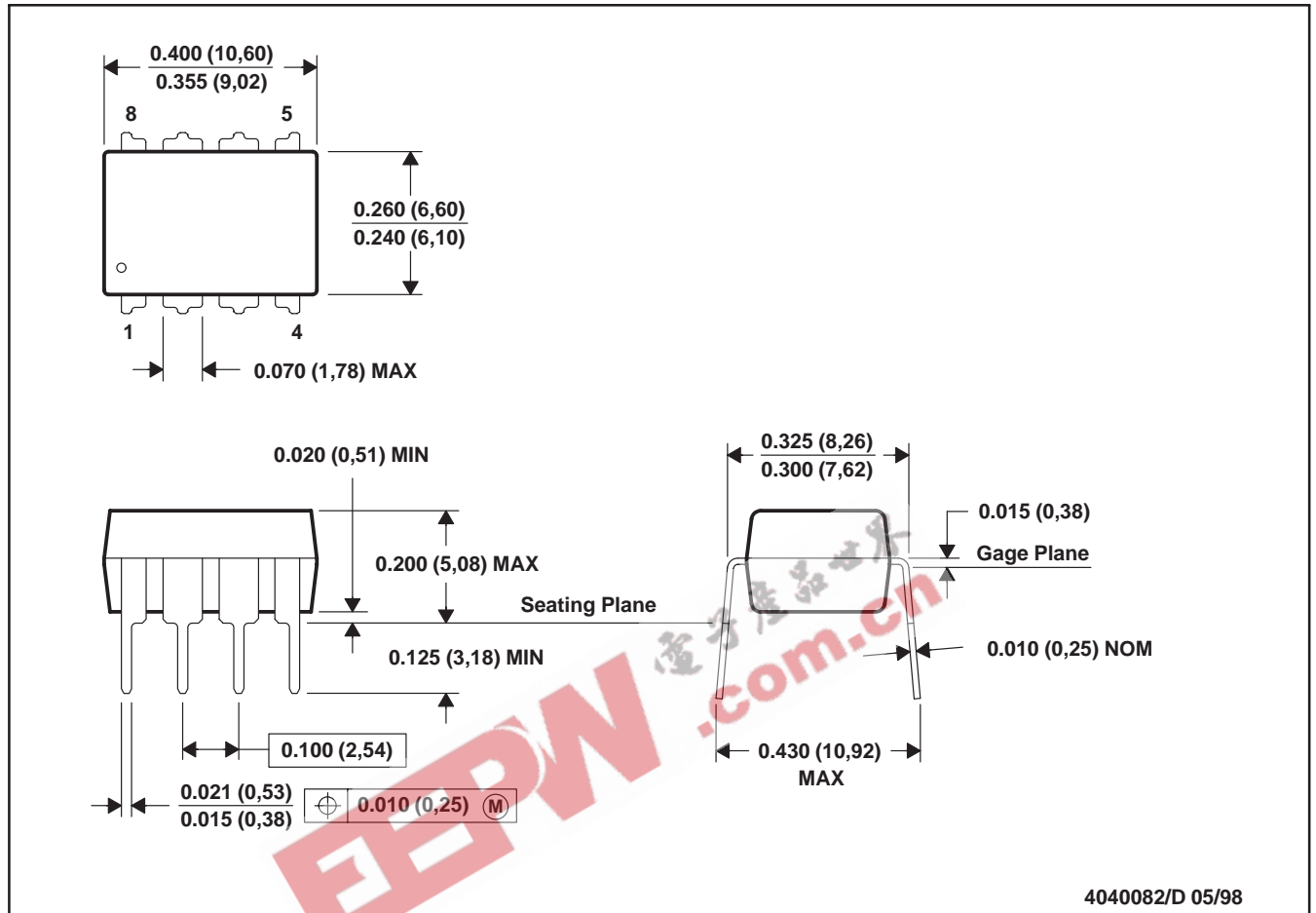
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

MECHANICAL DATA

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



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