## FEATURES

- **Simple Voltage Conversion, Including**
  - **Negative Converter**
  - **Voltage Doubler**
- **Wide Operating Range…1.5 V to 10 V**
- **Requires Only Two External (Noncritical) Capacitors**
- **No External Diode Over Full Temperature and Voltage Range**
- **Typical Open-Circuit Voltage Conversion Efficiency…99.9%**
- **Typical Power Efficiency…98%**
- **Full Testing at 3 V**

## APPLICATIONS

- **On-Board Negative Supplies**
- **Data-Acquisition Systems**
- **Portable Electronics**

**D, DGK, OR P PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| NC | 1 | 8 $V_{CC}$ |
| CAP+ | 2 | 7 OSC |
| GND | 3 | 6 LV |
| CAP− | 4 | 5 $V_{OUT}$ |
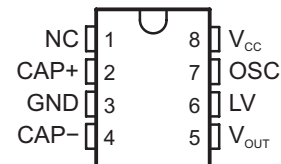
NC − No internal connection

## DESCRIPTION/ORDERING INFORMATION

The TL7660 is a CMOS switched-capacitor voltage converter that perform supply-voltage conversions from positive to negative. With only two noncritical external capacitors needed for the charge pump and charge reservoir functions, an input voltage within the range from 1.5 V to 10 V is converted to a complementary negative output voltage of −1.5 V to −10 V. The device can also be connected as a voltage doubler to generate output voltages up to 18.6 V with a 10-V input.

The basic building blocks of the IC include a linear regulator, an RC oscillator, a voltage-level translator, and four power MOS switches. To ensure latch-up-free operation, the circuitry automatically senses the most negative voltage in the device and ensures that the N-channel switch source-substrate junctions are not forward biased. The oscillator frequency runs at a nominal 10 kHz (for $V_{CC}$ = 5 V), but that frequency can be decreased by adding an external capacitor to the oscillator (OSC) terminal or increased by overdriving OSC with an external clock.

For low-voltage operation ($V_{IN}$ < 3.5 V), LV should be tied to GND to bypass the internal series regulator. Above 3.5 V, LV should be left floating to prevent device latchup.

The TL7660C is characterized for operation over a free-air temperature range of −40°C to 85°C. The TL7660I is characterized for operation over a free-air temperature range of −40°C to 125°C.

### ORDERING INFORMATION

| $T_A$ | PACKAGE[1] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING[2] |
|---|---|---|---|---|
| −40°C to 85°C | MSOP/VSSOP – DGK | Reel of 250 | TL7660CDGKT | TM_ |
| | | Reel of 2500 | TL7660CDGKR | |
| | PDIP – P | Tube of 50 | TL7660CP | TL7660CP |
| | SOIC – D | Tube of 75 | TL7660CD | 7660C |
| | | Reel of 2500 | TL7660CDR | |
| −40°C to 125°C | MSOP/VSSOP – DGK | Reel of 250 | TL7660IDGKT | TN_ |
| | | Reel of 2500 | TL7660IDGKR | |
| | PDIP – P | Tube of 50 | TL7660IP | TL7660IP |
| | SOIC – D | Tube of 75 | TL7660ID | 7660I |
| | | Reel of 2500 | TL7660IDR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DGK: The actual top-side marking has one additional character that indicates the assembly/test site.
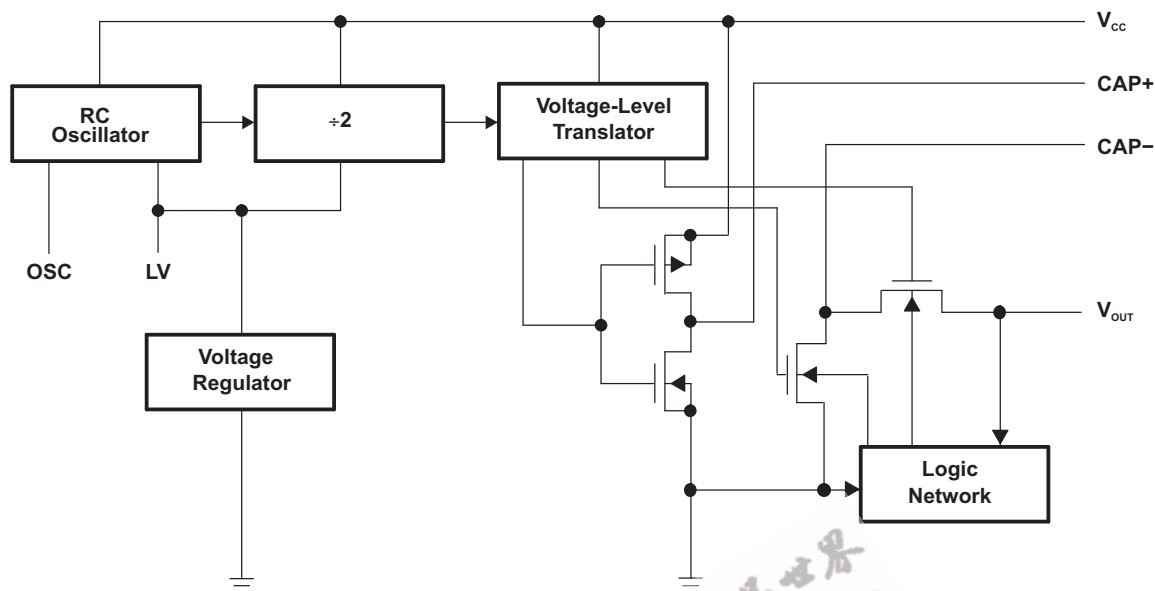
![Warning symbol] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## FUNCTIONAL BLOCK DIAGRAM



## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

|        |                                      |                          | MIN            | MAX            | UNIT |
|--------|--------------------------------------|--------------------------|----------------|----------------|------|
| $V_{CC}$ | Supply voltage                     | TL7660                   |                | 10.5           | V    |
| $V_I$  | OSC and LV input voltage range[2]    | $V_{CC}$ < 5.5 V         | −0.3           | $V_{CC}$ + 0.3 | V    |
|        |                                      | $V_{CC}$ > 5.5 V         | $V_{CC}$ − 5.5 | $V_{CC}$ + 0.3 |      |
| $I_{LV}$ | Current into LV[2]                 | $V_{CC}$ > 3.5 V         |                | 20             | µA   |
| $t_{OS}$ | Output short-circuit duration      | $V_{SUPPLY}$ ± 5.5 V     |      Continuous |                |      |
| $\theta_{JA}$ | Package thermal impedance[3][4] | D package              |                | 97             | °C/W |
|        |                                      | DGK package              |                | 172            |      |
|        |                                      | P package                |                | 85             |      |
| $T_J$  | Junction temperature                 |                          |                | 150            | °C   |
| $T_{stg}$ | Storage temperature range         |                          | −55            | 150            | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Connecting any input terminal to voltages greater than $V_{CC}$ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to power up of the TL7660.
(3) Maximum power dissipation is a function of $T_J$(max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

|        |                                 |          | MIN  | MAX | UNIT |
|--------|---------------------------------|----------|------|-----|------|
| $V_{CC}$ | Supply voltage                | TL7660   | 1.5  | 10  | V    |
| $T_A$  | Operating free-air temperature  | TL7660C  | −40  | 85  | °C   |
|        |                                 | TL7660I  | −40  | 125 |      |

## Electrical Characteristics

$V_{CC}$ = 5 V, $C_{OSC}$ = 0, LV = Open, $T_A$ = 25°C (unless otherwise noted) (see Figure 1)

| PARAMETER | | TEST CONDITIONS | $T_A$[1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | $R_L$ = ∞ | 25°C | | 45 | 110 | μA |
| | | | −40°C to 85°C | | | 120 | |
| | | | −40°C to 125°C | | | 135 | |
| $V_{CC,LOW}$ | Supply voltage range (low) | $R_L$ = 10 kΩ, LV = GND | Full range | 1.5 | | 3.5 | V |
| $V_{CC,HIGH}$ | Supply voltage range (high) | $R_L$ = 10 kΩ, LV Open | Full range | 3 | | 10 | V |
| $R_{OUT}$ | Output source resistance | $I_O$ = 20 mA | 25°C | | 45 | 70 | Ω |
| | | | −40°C to 85°C | | | 85 | |
| | | | −40°C to 125°C | | | 135 | |
| | | $V_{CC}$ = 2 V, $I_O$ = 3 mA, LV = GND | 25°C | | | 125 | |
| | | | −40°C to 85°C | | | 200 | |
| | | | −40°C to 125°C | | | 250 | |
| $f_{OSC}$ | Oscillator frequency | | 25°C | | 10 | | kHz |
| $\eta_{POWER}$ | Power efficiency | $R_L$ = 5 kΩ | 25°C | 96 | 98 | | % |
| | | | −40°C to 125°C | 95 | | | |
| $\eta_{VOUT}$ | Voltage conversion efficiency | $R_L$ = ∞ | 25°C | 99 | 99.9 | | % |
| | | | −40°C to 125°C | 99 | | | |
| $Z_{OSC}$ | Oscillator impedance | $V_{CC}$ = 2 V | 25°C | | | 1 | MΩ |
| | | $V_{CC}$ = 5 V | | | 100 | | kΩ |

(1)  Full range is −40°C to 85°C for the TL7660C and −40°C to 125°C for the TL7660I.
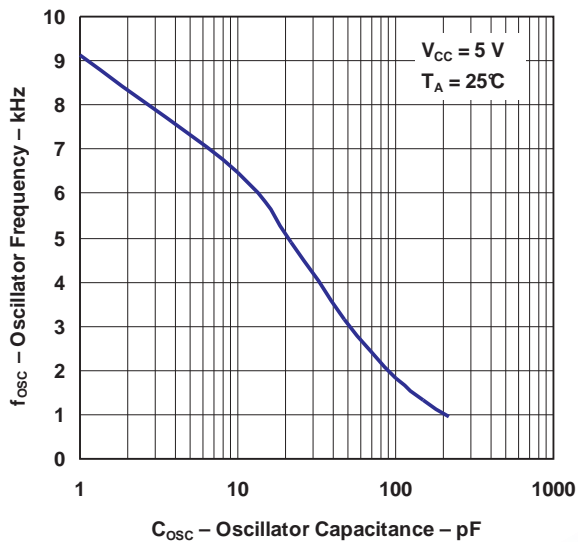
## Electrical Characteristics

$V_{CC}$ = 3 V, $C_{OSC}$ = 0, LV = GND, (unless otherwise noted) (see Figure 1)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current[1] | $R_L$ = ∞ | 25°C | | 24 | 50 | μA |
| | | | −40°C to 85°C | | | 60 | |
| | | | −40°C to 125°C | | | 75 | |
| $R_{OUT}$ | Output source resistance | $I_O$ = 10 mA | 25°C | | 60 | 100 | Ω |
| | | | −40°C to 85°C | | | 110 | |
| | | | −40°C to 125°C | | | 120 | |
| $f_{OSC}$ | Oscillator frequency | $C_{OSC}$ = 0 | 25°C | 5 | 9 | | kHz |
| | | | −40°C to 125°C | 3 | | | |
| $\eta_{POWER}$ | Power efficiency | $R_L$ = 5 kΩ | 25°C | 96 | 98 | | % |
| | | | −40°C to 125°C | 95 | | | |
| $\eta_{VOUT}$ | Voltage conversion efficiency | $R_L$ = ∞ | 25°C | 99 | | | % |
| | | | −40°C to 125°C | 99 | | | |

(1)  Derate linearly above 50°C by 5.5 mW/°C.

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## TYPICAL CHARACTERISTICS

**OSCILLATOR FREQUENCY
vs
OSCILLATOR CAPACITANCE**

$V_{CC} = 5 \text{ V}$
$T_A = 25°C$

$f_{OSC}$ – Oscillator Frequency – kHz

$C_{OSC}$ – Oscillator Capacitance – pF

**OSCILLATOR FREQUENCY
vs
TEMPERATURE**

$V_{CC} = 10 \text{ V}$

$V_{CC} = 5 \text{ V}$

$f_{OSC}$ – Oscillator Frequency – kHz

$T_A$ – Free-Air Temperature – °C
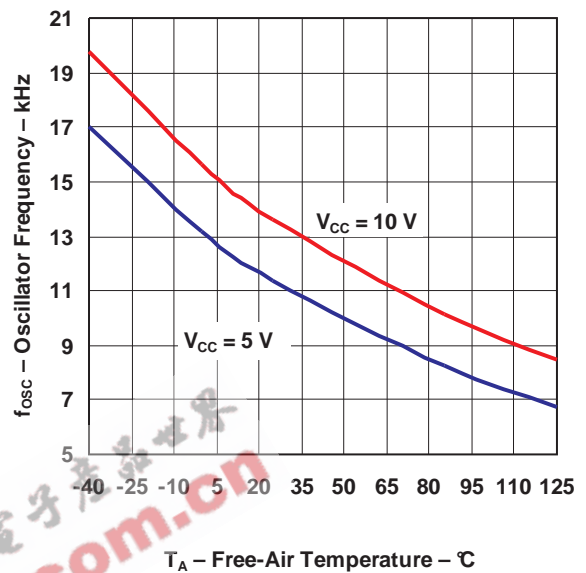
**OUTPUT RESISTANCE
vs
TEMPERATURE**

$R_{OUT}$ – Output Source Resistance – Ω

$V_{CC} = 2 \text{ V}$
$I_O = 3 \text{ mA}$

$V_{CC} = 5 \text{ V}$
$I_O = 20 \text{ mA}$

$V_{CC} = 10 \text{ V}$
$I_O = 20 \text{ mA}$

$T_A$ – Free-Air Temperature – °C
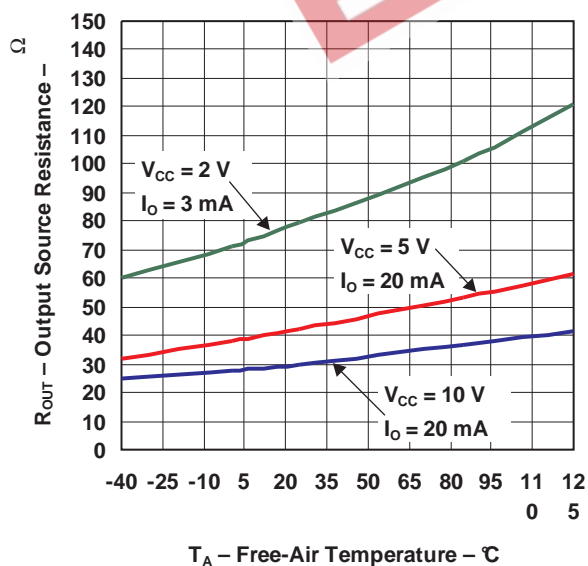
**SUPPLY VOLTAGE
vs
TEMPERATURE**

$V_{CC}$ – Supply Voltage – V

Supply Voltage Range
(No Diode Required)

$T_A$ – Free-Air Temperature – °C

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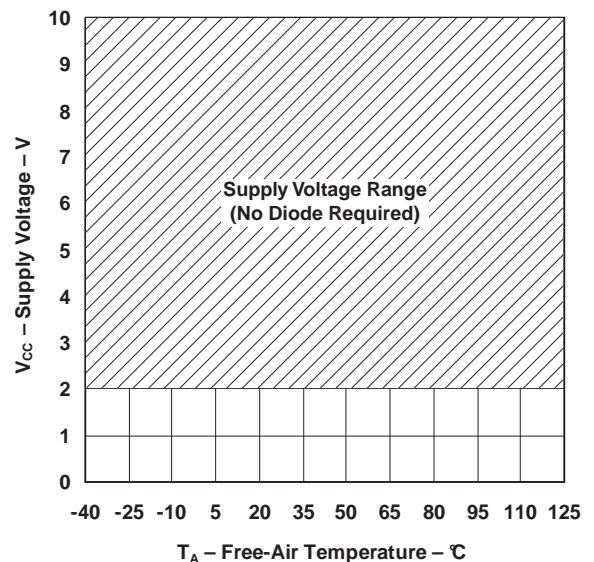
## TYPICAL CHARACTERISTICS (continued)

OUTPUT RESISTANCE
vs
SUPPLY VOLTAGE
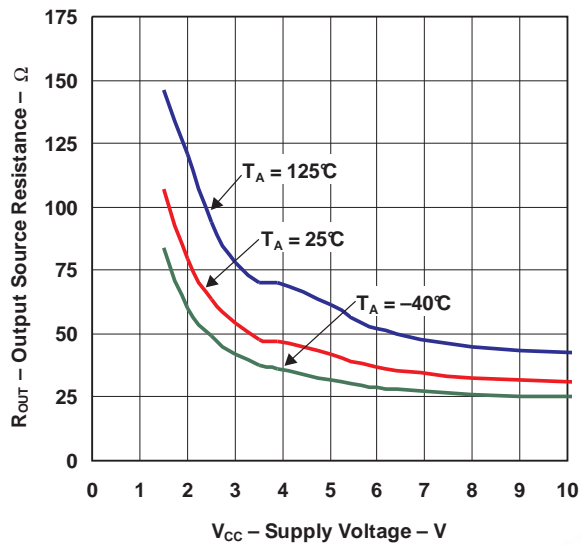


OUTPUT RESISTANCE
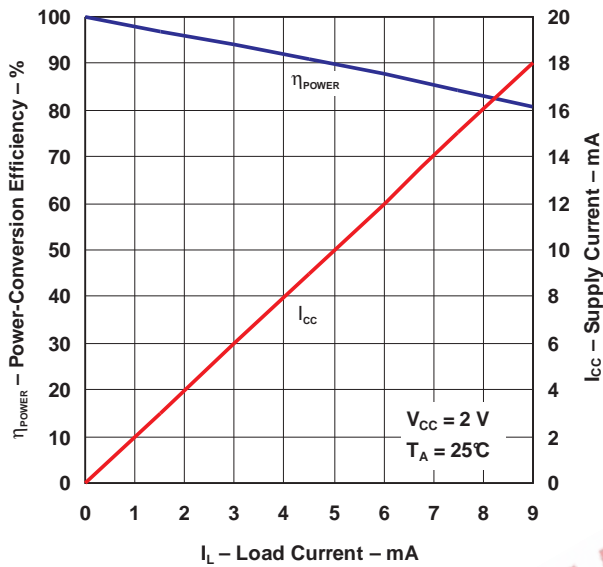vs
OSCILLATOR FREQUENCY
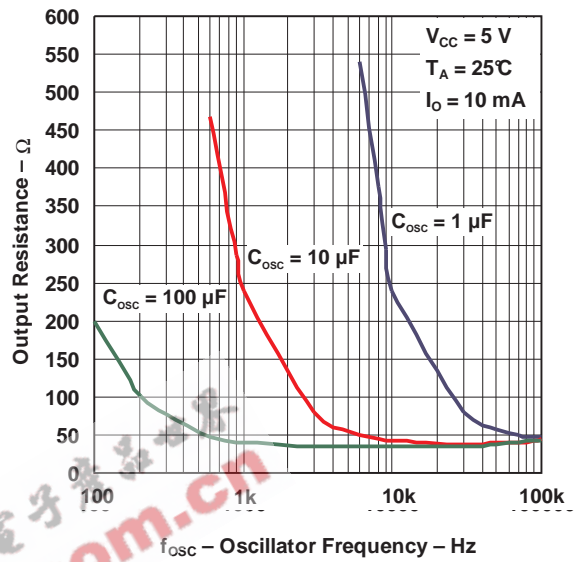


OUTPUT VOLTAGE
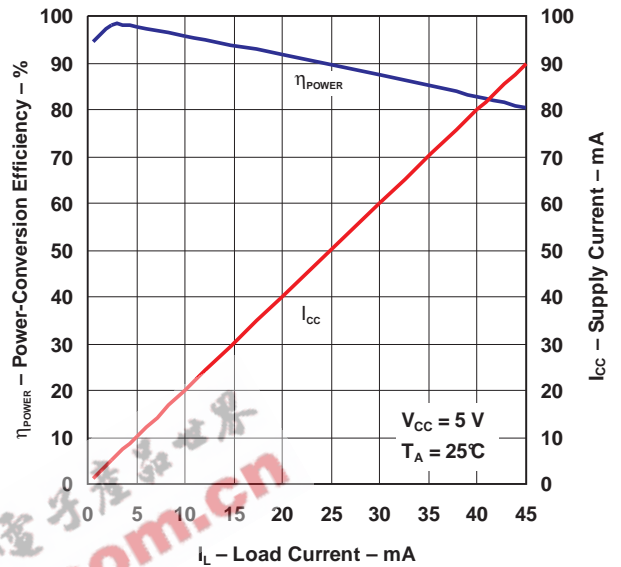vs
LOAD CURRENT



OUTPUT VOLTAGE
vs
LOAD CURRENT

**TL7660**
**CMOS VOLTAGE CONVERTER**
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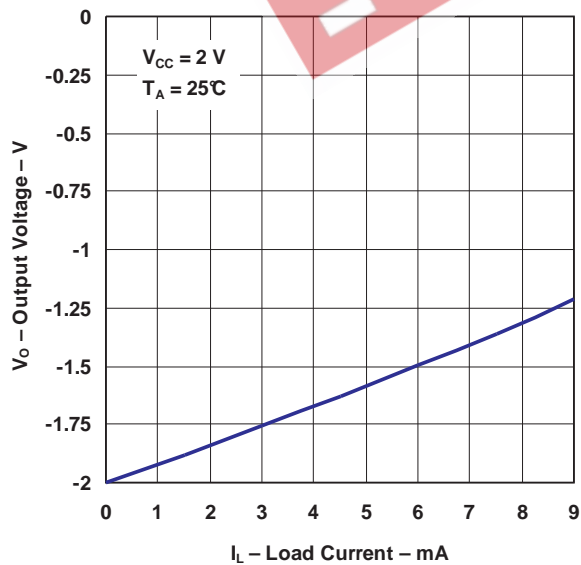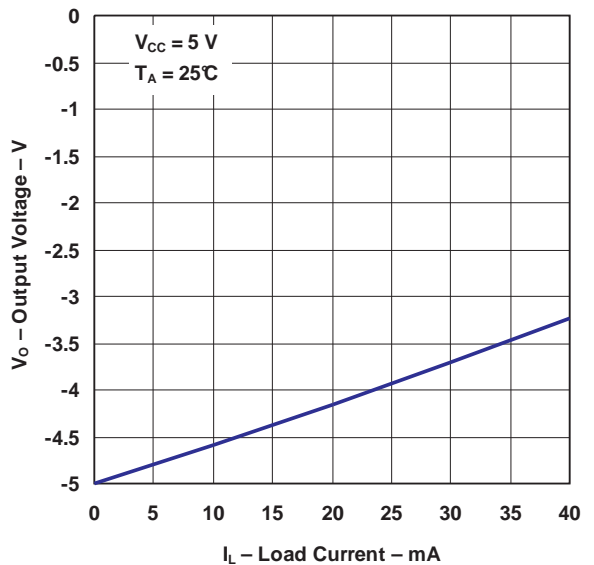
## TYPICAL CHARACTERISTICS (continued)

**EFFICIENCY AND SUPPLY CURRENT**
**vs**
**LOAD CURRENT**



**EFFICIENCY AND SUPPLY CURRENT**
**vs**
**LOAD CURRENT**



**EFFICIENCY**
**vs**
**OSCILLATOR FREQUENCY**
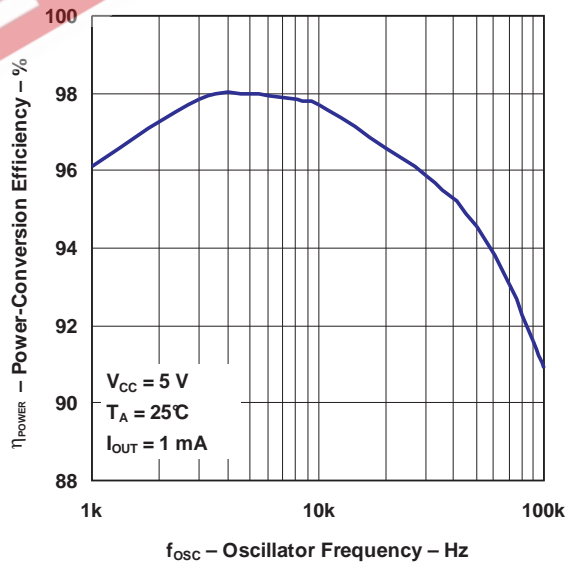
## APPLICATION INFORMATION
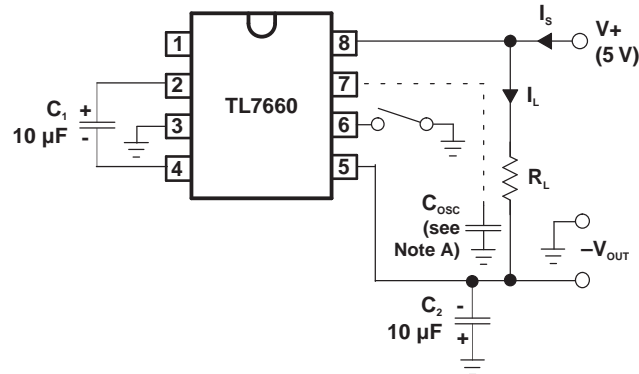


A. In the circuit, there is no external capacitor applied to terminal 7. However when device is plugged into a test socket,there is usually a very small but finite stray capacitance present on the order of 10 pF.

**Figure 1. Test Circuit**

The TL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors which may be inexpensive 10 µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor $C_1$ is charged to a voltage, $V_{CC}$, for the half cycle when switches $S_1$ and $S_3$ are closed. (Note: Switches $S_2$ and $S_4$ are open during this half cycle.) During the second half cycle of operation, switches $S_2$ and $S_4$ are closed, with $S_1$ and $S_3$ open, thereby shifting capacitor $C_1$ negatively by $V_{CC}$ volts. Charge is then transferred from $C_1$ to $C_2$ such that the voltage on $C_2$ is exactly $V_{CC}$, assuming ideal switches and no load on $C_2$. The TL7660 approaches this ideal situation more closely than existing non-mechanical circuits. In the TL7660, the four switches of Figure 2 are MOS power switches: $S_1$ is a p-channel device, and $S_2$, $S_3$, and $S_4$ are n-channel devices. The main difficulty with this design is that in integrating the switches, the substrates of $S_3$ and $S_4$ must always remain reverse biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start up and under output short circuit conditions ($V_{OUT} = V_{CC}$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this results in high power losses and probable device latchup. This problem is eliminated in the TL7660 by a logic network which senses the output voltage ($V_{OUT}$) together with the level translators and switches the substrates of $S_3$ and $S_4$ to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TL7660 is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low-voltage operation, the LV terminal should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 V, the LV terminal must be left open to insure latchup proof operation and prevent device damage.
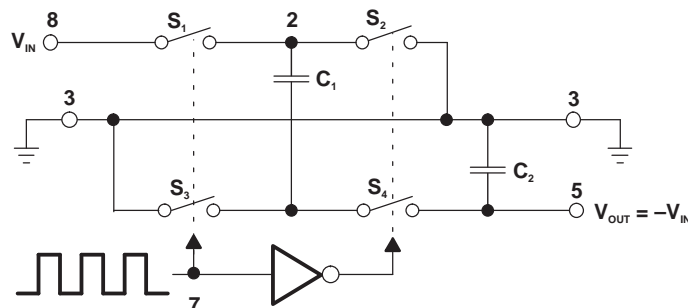


**Figure 2. Idealized Negative-Voltage Converter**

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## APPLICATION INFORMATION (continued)

### Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met.

- The driver circuitry consumes minimal power.
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TL7660 approaches these conditions for negative voltage conversion if large values of $C_1$ and $C_2$ are used.

Energy is only lost in the transfer of charge between capacitors if a change in voltage occurs. The energy lost is defined by:

$$E = \tfrac{1}{2}\, C_1 (V_1{}^2 - V_2{}^2)$$

Where $V_1$ and $V_2$ are the voltages on $C_1$ during the pump and transfer cycles. If the impedances of $C_1$ and $C_2$ are relatively high at the pump frequency (see Figure 2) compared to the value of $R_L$, there is a substantial difference in the voltages $V_1$ and $V_2$. Therefore, it is not only desirable to make $C_2$ as large as possible to eliminate output voltage ripple but also to employ a correspondingly large value for $C_1$ in order to achieve maximum efficiency of operation.

### Do's and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5 V.
- Do not short circuit the output to $V_{CC}$ supply for supply voltages above 5.5 V for extended periods, however, transient conditions including start-up are okay.
- When using polarized capacitors, the positive terminal of $C_1$ must be connected to terminal 2 of the TL7660, and the positive terminal of $C_2$ must be connected to GND.
- If the voltage supply driving the TL7660 has a large source impedance (25 Ω − 30 Ω), then a 2.2-µF capacitor from terminal 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
- Ensure that the output (terminal 5) does not go more positive than GND (terminal 3). Device latch up occurs under these conditions. A 1N914 or similar diode placed in parallel with $C_2$ prevents the device from latching up under these conditions (anode to terminal 5, cathode to terminal 3).

## APPLICATION INFORMATION (continued)

### Typical Applications

#### Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the TL7660 for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5 V.
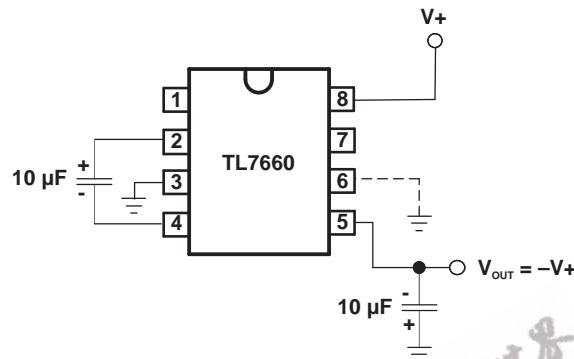


**Figure 3. Simple Negative-Voltage Converter**

The output characteristics of the circuit in Figure 3 can be approximated by an ideal voltage source in series with a resistance. The voltage source has a value of $-V_{CC}$. The output impedance ($R_O$) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of $C_1$ and $C_2$, and the ESR (equivalent series resistance) of $C_1$ and $C_2$. A good first order approximation for $R_O$ is:

$$R_O \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1})$$
$$R_O \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 1/f_{PUMP}C_1 + ESR_{C2}$$

Where $f_{PUMP} = f_{OSC}/2$ , $R_{SWX}$ = MOSFET switch resistance.

Combining the four RSWX terms as RSW, we see that:

$$R_O \approx 2(R_{SW}) + 1/f_{PUMP}C_1 + 4(ESR_{C1}) + ESR_{C2}$$

$R_{SW}$, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs). Careful selection of $C_1$ and $C_2$ reduces the remaining terms, minimizing the output impedance. High value capacitors reduce the $1/f_{PUMP}C_1$ component, and low ESR capacitors lower the ESR term. Increasing the oscillator frequency reduces the $1/f_{PUMP}C_1$ term but may have the side effect of a net increase in output impedance when $C_1 > 10$ µF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where $f_{OSC} = 10$ kHz and $C = C1 = C2 = 10$ µF:

$$R_O \approx 2(23) + 1/(5 \times 10^3)(10^{-5}) + 4(ESR_{C1}) + ESR_{C2}$$
$$R_O \approx 46 + 20 + 5 (ESR_C)$$

Because the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/f_{PUMP}C_1$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10 Ω.

## APPLICATION INFORMATION (continued)

### Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by two voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of $C_2$ at the instant it goes from being charged by $C_1$ (current flow into $C_2$) to being discharged through the load (current flowing out of $C_2$). The magnitude of this current change is $2 \times I_{OUT}$, hence the total drop is $2 \times I_{OUT} \times eSR_{C2}$ V. Segment B is the voltage change across $C_2$ during time $t_2$, the half of the cycle when $C_2$ supplies current to the load. The drop at B is $I_{OUT} \times t_2/C_2$ V. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \approx (1/(2f_{PUMP}C_2) + 2(ESR_{C2})) \times I_{OUT}$$

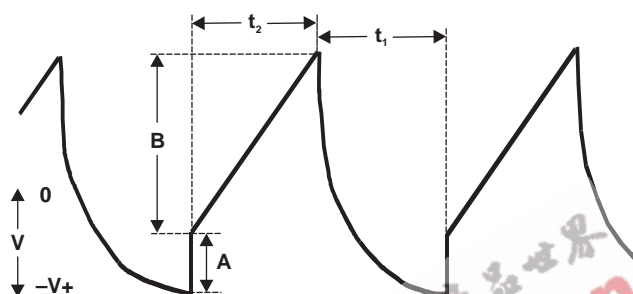Again, a low ESR capacitor results in a higher performance output.



**Figure 4. Output Ripple**

### Paralleling Devices

Any number of TL7660 voltage converters may be paralleled to reduce output resistance (see Figure 5). The reservoir capacitor, $C_2$, serves all devices, while each device requires its own pump capacitor, $C_1$. The resultant output resistance would be approximately:

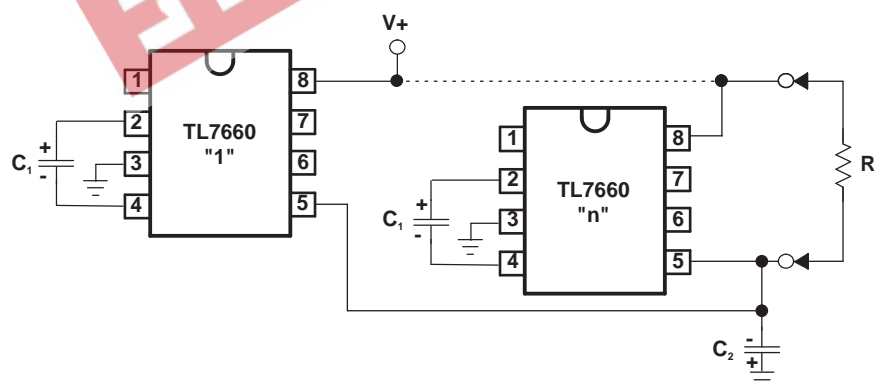$$R_{OUT} = R_{OUT} \text{ (of TL7660)}/n \text{ (number of devices)}$$



**Figure 5. Paralleling Devices**

## APPLICATION INFORMATION (continued)

### Cascading Devices

The TL7660 may be cascaded as shown to produced larger negative multiplication of the initial supply voltage (see Figure 6). However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n \, (V_{IN})$$

Where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TL7660 $R_{OUT}$ values.
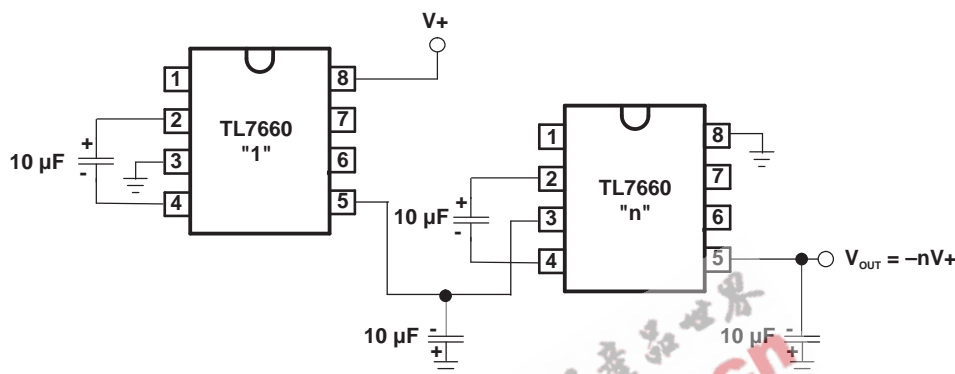
**Figure 6. Cascading Devices for Increased Output Voltage**

### Changing the TL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. To prevent possible device latchup, a 1-kΩ resistor must be used in series with the clock output. When the external clock frequency is generated using TTL logic, the addition of a 10-kΩ pullup resistor to $V_{CC}$ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.
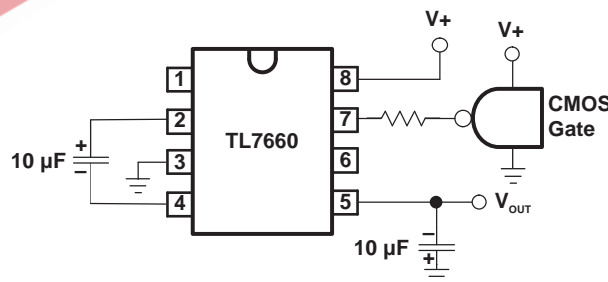
**Figure 7. External Clocking**

## APPLICATION INFORMATION (continued)

It is also possible to increase the conversion efficiency of the TL7660 at low load levels by lowering the oscillator frequency (see Figure 8). This reduces the switching losses. However, lowering the oscillator frequency causes an undesirable increase in the impedance of the pump ($C_1$) and reservoir ($C_2$) capacitors; this is overcome by increasing the values of $C_1$ and $C_2$ by the same factor that the frequency has been reduced. For example, the addition of a 100-pF capacitor between terminal 7 (OSC) and $V_{CC}$ lowers the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of $C_1$ and $C_2$ (from 10 µF to 100 µF).
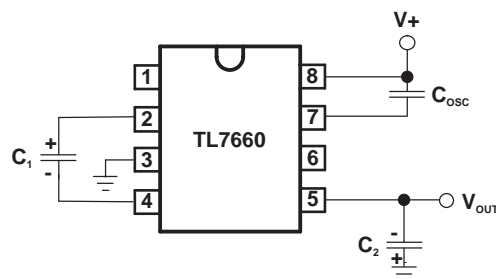


**Figure 8. Lowering Oscillator Frequency**

### Positive Voltage Doubling

The TL7660 may be used to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the TL7660 are used to charge $C_1$ to a voltage level of $V_{CC} - V_F$ (where $V_{CC}$ is the supply voltage and $V_F$ is the forward voltage drop of diode D1). On the transfer cycle, the voltage on $C_1$ plus the supply voltage ($V_{CC}$) is applied through diode $D_2$ to capacitor $C_2$. The voltage thus created on $C_2$ becomes $(2V_{CC}) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes $D_1$ and $D_2$.

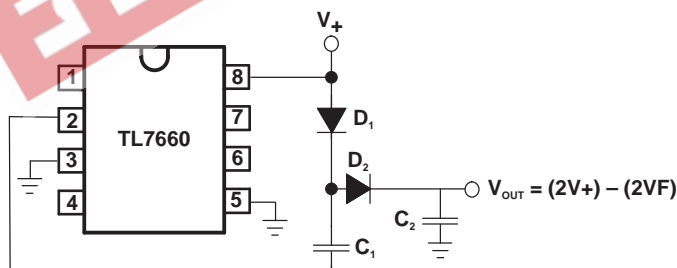The source impedance of the output ($V_{OUT}$) depends on the output current.



**Figure 9. Positive-Voltage Doubler**

## APPLICATION INFORMATION (continued)

**Combined Negative Voltage Conversion and Positive Supply Doubling**

Figure 10 combines the functions shown in Figure 3 and Figure 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 V and −5 V from an existing 5-V supply. In this instance, capacitors $C_1$ and $C_3$ perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors $C_2$ and $C_4$ are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration that combines both functions, however, in that the source impedances of the generated supplies are somewhat higher, due to the finite impedance of the common charge pump driver at terminal 2 of the device.
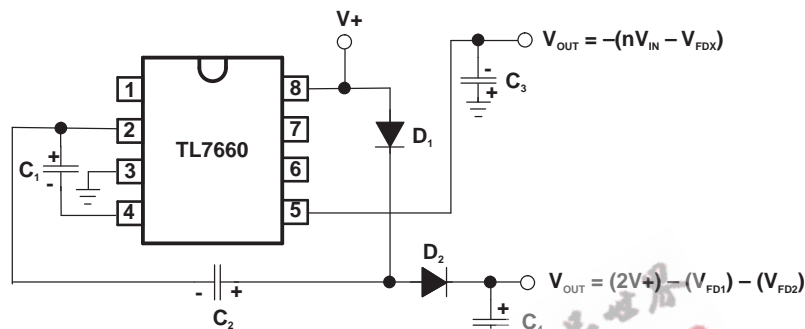


**Figure 10. Combined Negative-Voltage Converter and Positive-Voltage Doubler**

**Voltage Splitting**

The bidirectional characteristics can also be used to split a higher supply in half (see Figure 11. The combined load is evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit and then the circuit of Figure 6, 15 V can be converted (via 7.5 V, and −7.5 V) to a nominal −15 V, although with rather high series output resistance (~250 Ω).
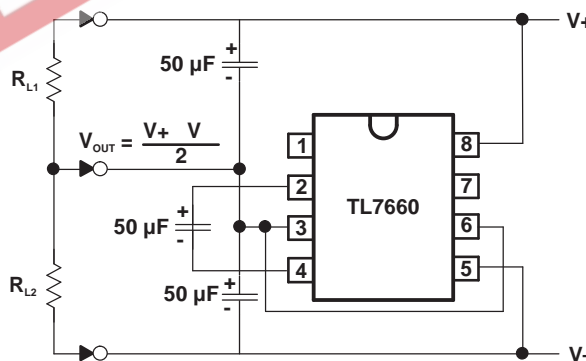


**Figure 11. Splitting a Supply in Half**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TL7660CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDGKT | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDGKTG4 | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL7660CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL7660ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDGKT | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDGKTG4 | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL7660IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL7660IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**P (R-PDIP-T8)**         **PLASTIC DUAL-IN-LINE**



4040082/D 05/98

NOTES: A. All linear dimensions are in inches (millimeters).
      B. This drawing is subject to change without notice.
      C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm
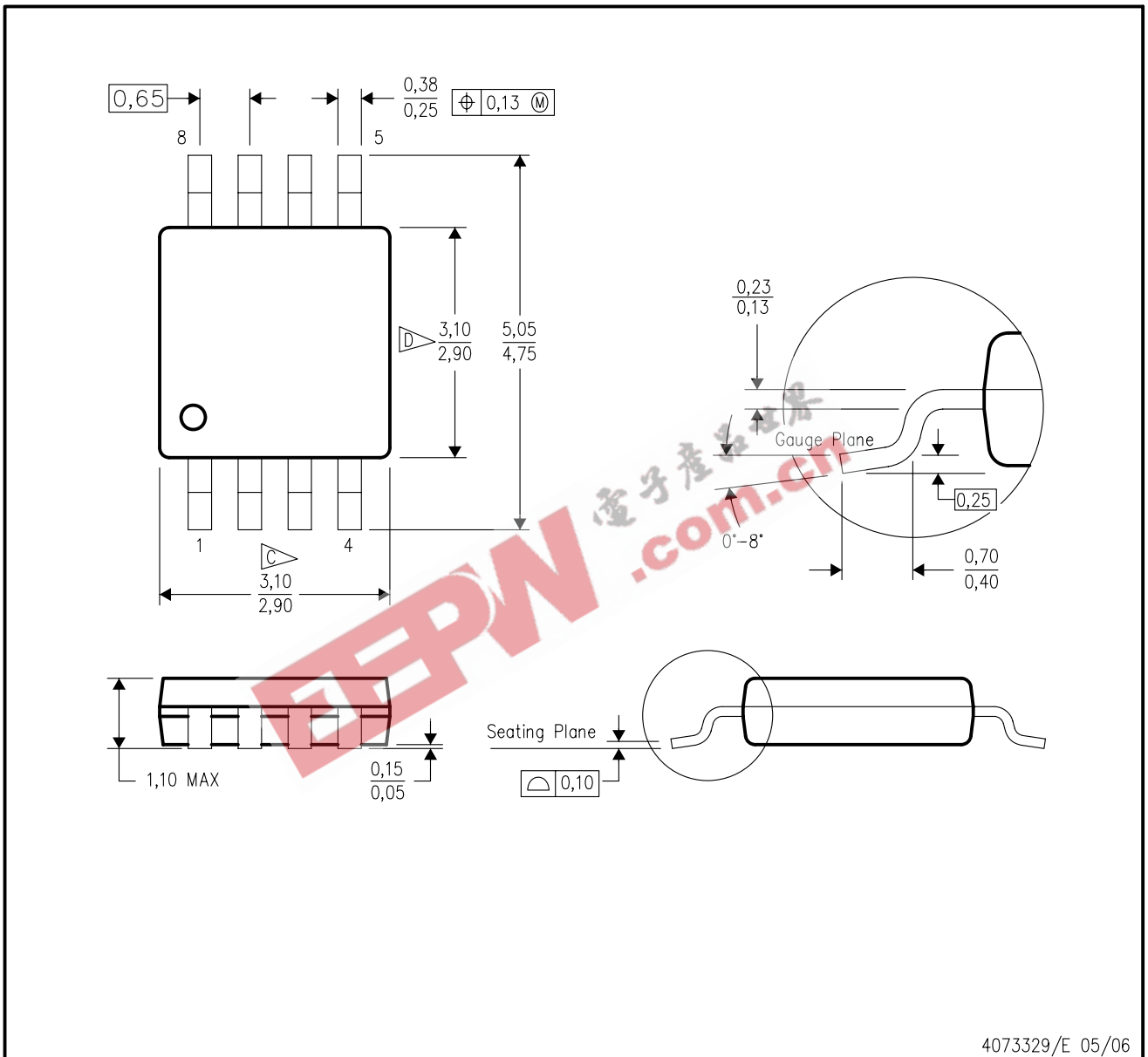
## DGK (S−PDSO−G8)                    PLASTIC SMALL−OUTLINE PACKAGE



4073329/E 05/06

NOTES:    A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C⊳ Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D⊳ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E.    Falls within JEDEC MO−187 variation AA, except interlead flash.

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## D (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)
C

8    5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1    4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
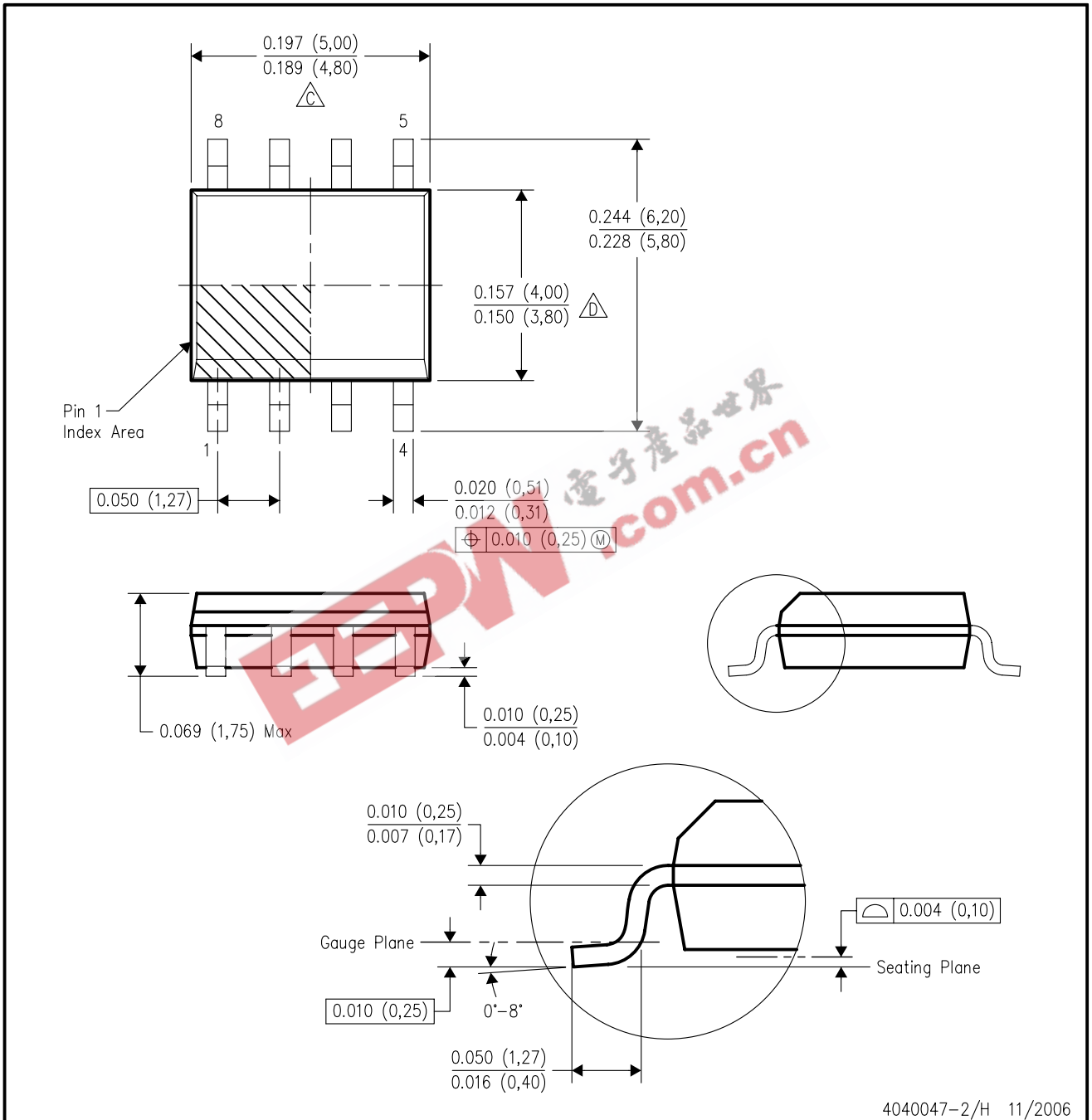0.016 (0,40)

4040047−2/H  11/2006

NOTES:   A.   All linear dimensions are in inches (millimeters).
        B.   This drawing is subject to change without notice.
        C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
            not exceed .006 (0,15) per end.
        D.   Body width does not include interlead flash.  Interlead flash shall not exceed .017 (0,43) per side.
        E.   Reference JEDEC MS−012 variation AA.

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