

TL1464I

QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

- High-Speed Drive Controller for PNP Power Transistor
- Internal-Regulator Provides a Stable 1.5 V Reference Supply
- Low Start-Up Voltage 3.1 V
- Internal Short-Circuit Protection
- Internal Undervoltage Lockout Protection
- Internal Shut-Down Circuit by Channel
- Controllable Base Current of External Transistor

description

The TL1464I incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the TL1464I contains an on-chip 1.5 V regulator, four error amplifiers, an oscillator, two dead-time comparators, undervoltage lockout circuitry, short circuit protection, standby control circuitry, and output circuits.

The external speed-up capacitors provide exceptional rise and fall time performance for the PNP power transistor.

The TL1464I operates from 3.1 V supply voltage and 2 pair of four-outputs (CH-1/CH-3, CH-2/CH-4 the same period) at the inverse phase of each other. As a result, the TL1464I provides high-efficiency power supply.

FUNCTION TABLE

| INPUTS | | OUTPUT FUNCTIONS | | | | |
|--------------------------|--|------------------|----------|----------|----------|----------|
| STANDBY | STANDBY-2 TO4 | VREF | OUTPUT-1 | OUTPUT-2 | OUTPUT-3 | OUTPUT-4 |
| $V_I \leq 0.4 \text{ V}$ | $V_I \leq 0.4 \text{ V}, V_I \geq 2.4 \text{ V}$ | L | OFF | OFF | OFF | OFF |
| $V_I \geq 2.4 \text{ V}$ | $V_I \geq 2.4 \text{ V}$ | H | ON | ON | ON | ON |
| | $V_I \geq 0.4 \text{ V}$ | H | ON | See Note | See Note | See Note |

NOTE: When the STANDBY input is high ($\geq 2.4 \text{ V}$), OUTPUT-2 to 4 are controlled individually. If STANDBY-2 input is low ($\leq 0.4 \text{ V}$), OUTPUT-2 is turned off. When CH-2 standby mode is released, CH-2 can do the soft-start function.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

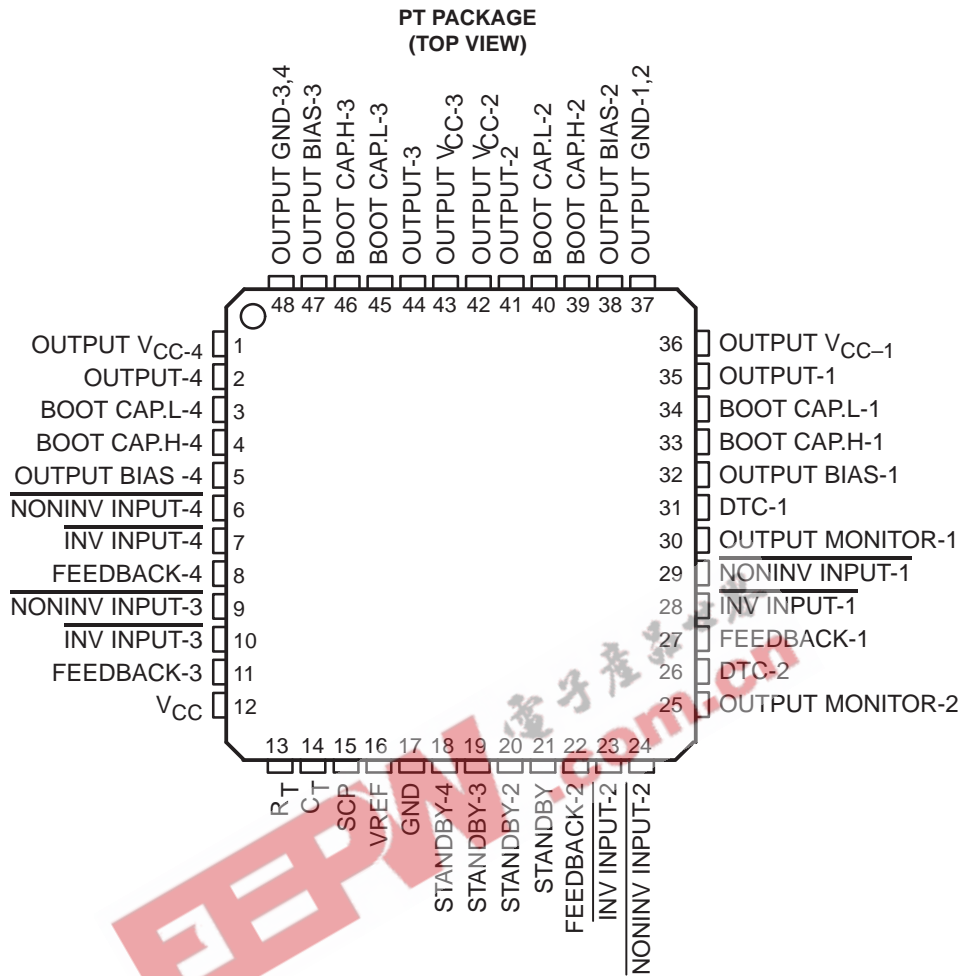
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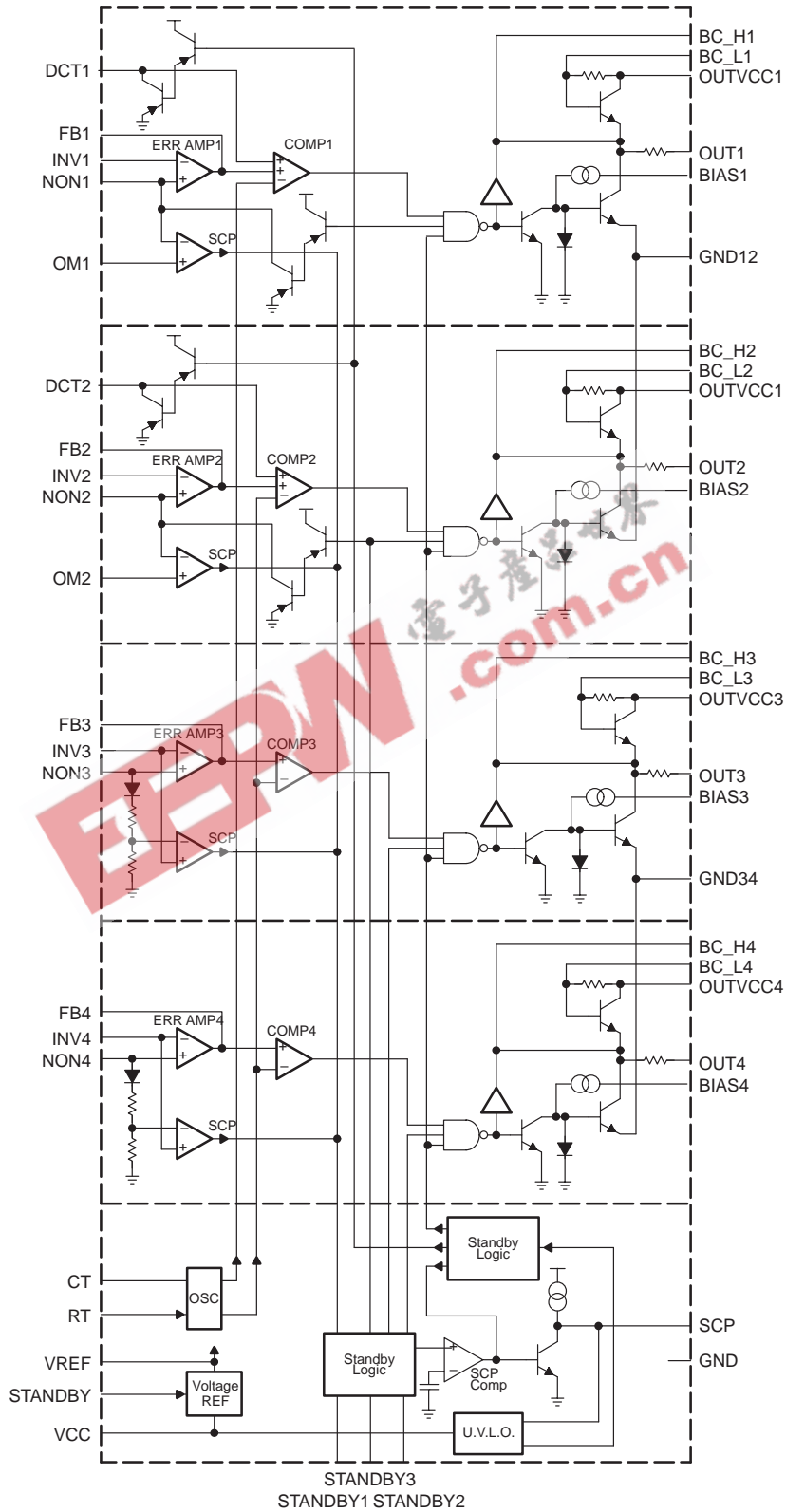
SLVS266 – FEBRUARY 2000



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SLVS266 – FEBRUARY 2000

functional block diagram



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QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------------------|-----|-----|--|
| BOOT CAP.H-1 | 33 | | Boot-strap capacitor connect pin (CH-1) |
| BOOT CAP.L-1 | 34 | | |
| BOOT CAP.H-2 | 39 | | Boot-strap capacitor connect pin (CH-2) |
| BOOT CAP.L-2 | 40 | | |
| BOOT CAP.H-3 | 46 | | Boot-strap capacitor connect pin (CH-3) |
| BOOT CAP.L-3 | 45 | | |
| BOOT CAP.H-4 | 4 | | Boot-strap capacitor connect pin (CH-4) |
| BOOT CAP.L-4 | 3 | | |
| C _T | 14 | | Timing capacitor connect pin |
| DTC-1 | 31 | | Dead-time control input pin (CH-1) |
| DTC-2 | 26 | | Dead-time control input pin (CH-2) |
| FEEDBACK-1 | 27 | | Error amplifier output pin (CH-1) |
| FEEDBACK-2 | 22 | | Error amplifier output pin (CH-2) |
| FEEDBACK-3 | 11 | | Error amplifier output pin (CH-3) |
| FEEDBACK-4 | 8 | | Error amplifier output pin (CH-4) |
| GND | 17 | | Ground pin |
| INV INPUT-1 | 28 | | Error amplifier inverting input pin (CH-1) |
| INV INPUT-2 | 23 | | Error amplifier inverting input pin (CH-2) |
| INV INPUT-3 | 10 | | Error amplifier inverting input pin (CH-3) |
| INV INPUT-4 | 7 | | Error amplifier inverting input pin (CH-4) |
| NONINV INPUT-1 | 29 | | Error amplifier noninverting input pin (CH-1) |
| NONINV INPUT-2 | 24 | | Error amplifier noninverting input pin (CH-2) |
| NONINV INPUT-3 | 9 | | Error amplifier noninverting input pin (CH-3) |
| NONINV INPUT-4 | 6 | | Error amplifier noninverting input pin (CH-4) |
| OUTPUT-1 | 35 | | Output pin (CH-1) |
| OUTPUT-2 | 41 | | Output pin (CH-2) |
| OUTPUT-3 | 44 | | Output pin (CH-3) |
| OUTPUT-4 | 2 | | Output pin (CH-4) |
| OUTPUT BIAS-1 | 32 | | Output ON current setup pin (CH-1) |
| OUTPUT BIAS-2 | 38 | | Output ON current setup pin (CH-2) |
| OUTPUT BIAS-3 | 47 | | Output ON current setup pin (CH-3) |
| OUTPUT BIAS-4 | 5 | | Output ON current setup pin (CH-4) |
| OUTPUT GND-1,2 | 37 | | Output ground pin (CH-1,2) |
| OUTPUT GND-3,4 | 48 | | Output ground pin (CH-3,4) |
| OUTPUT MONITOR-1 | 30 | | Output monitor comparator input pin (CH-1) |
| OUTPUT MONITOR-2 | 25 | | Output monitor comparator input pin (CH-2) |
| OUTPUT V _{CC} -1 | 36 | | Output supply pin (CH-1) |
| OUTPUT V _{CC} -2 | 42 | | Output supply pin (CH-2) |
| OUTPUT V _{CC} -3 | 43 | | Output supply pin (CH-3) |
| OUTPUT V _{CC} -4 | 1 | | Output supply pin (CH-4) |
| R _T | 13 | | Timing resistor connect pin |
| SCP | 15 | | Short-circuit protection capacitor connect pin |

TL1464I QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

Terminal Functions (Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-----------------|-----|-----|---|
| STANDBY | 21 | | Output-1 to 4 control pin. Input L level voltage (0.4 V max). All outputs function and VREF are shutdown. |
| STANDBY-2 | 20 | | Output-2 control pin. Input L level voltage (0.4 V max), output-2 function is shutdown. |
| STANDBY-3 | 19 | | Output-3 control pin. Input L level voltage (0.4 V max), output-3 function is shutdown. |
| STANDBY-4 | 18 | | Output-4 control pin. Input L level voltage (0.4 V max), output-4 function is shutdown. |
| V _{CC} | 12 | | Power supply pin |

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V _{CC} (see Note 1) | 13 V |
| Amplifier input voltage, V _{IC} | 13 V |
| Output voltage, V _O | 13 V |
| Peak output current (sink), I _(SINK) | 100 mA |
| Peak output current (source), I _(SOURCE) | 1 A |
| Continuous total dissipation at (or below) 25°C free-air temperature (unit), P _D | 695 mW |
| Continuous total dissipation at (or below) 25°C free-air temperature (using board), P _D (see Note 2) | 1315 mW |
| Operating free-air temperature range, T _A | –20°C to 75°C |
| Storage temperature range, T _{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.
2. Using 1.6 × 50 × 50 mm glass epoxy resin.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---------|-----|----------------------|------|
| Supply voltage, V _{CC} | 3.1 | | 12 | V |
| Amplifier input voltage, V _{IC} | CH-1,2 | | V _{CC} –1.8 | V |
| | CH-3,4 | 0 | V _{CC} –1.8 | |
| Standby input voltage, V _I (pins 18, 19, 20, 21) | H level | 2.4 | V _{CC} | V |
| | L level | | 0.4 | |
| Output voltage, V _O | | | 12 | V |
| Current into feedback terminal, I _(CAMP) | | | –45 | μA |
| Feedback resistor, R _(NF) | 100 | | | kΩ |
| Boot-strap capacitor, C _(BOOT) | 100 | 500 | | pF |
| Bias resistor, R _(BIAS) | 1.2 | | 20 | |
| Bias capacitor, C _(BIAS) | | 30 | 200 | pF |
| Timing resistor, R _(T) | 7 | | 50 | kΩ |
| Timing capacitor, C _(T) | 68 | | 1000 | pF |
| Oscillation frequency, f _(OSC) | 0.05 | | 2 | MHz |
| Operating free-air temperature, T _A | –20 | | 75 | °C |

TL1464I

QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6\text{ V}$, $f = 1\text{ MHz}$ (unless otherwise noted)

reference section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--|--|-------|-------|-----------|------|
| V_{ref} | Output voltage (pin 16) | $T_A = 25^\circ\text{C}$, $I_{(OR)} = -1\text{ mA}$ | 1.485 | 1.50 | 1.515 | V |
| $R_{(EGIN)}$ | Input regulation | $V_{OS} = 3.1\text{ V to }12\text{ V}$, $I_{(OR)} = -1\text{ mA}$ | | 2 | 12.5 | mV |
| $R_{(EFL)}$ | Output regulation | $I_{(OR)} = -0.1\text{ mA to }-1\text{ mA}$ | | 1 | 7.5 | mV |
| $V_{(RTC1)}$ | Output voltage change with temperature | $T_A = 20^\circ\text{C to }25^\circ\text{C}$ | | -0.2% | $\pm 2\%$ | |
| $R_{(RTC2)}$ | | $T_A = 25^\circ\text{C to }75^\circ\text{C}$ | | -0.2% | $\pm 2\%$ | |
| I_{OS} | Short-circuit output current | $V_{ref} = 0\text{ V}$ | 4 | 8 | | mA |

undervoltage lockout section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|--------------------------|-----|-----|-----|------|
| V_{IH} | Upper threshold voltage | $T_A = 25^\circ\text{C}$ | | 2.7 | | V |
| V_{IL} | Lower threshold voltage | | | 2.5 | | V |
| V_{hys} | Hysteresis | | 0.1 | 0.2 | | V |
| V_R | Reset threshold voltage (V_{CC}) | | 2.2 | 2.3 | | V |

output voltage monitor section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|----------------------|---|-----|-------------------|------|------|
| $V_{IO(M)}$ | Input offset voltage | $T_A = 25^\circ\text{C}$ (CH-1,2) | | 0 | | V |
| | | $V_I = 1.5\text{ V}$ (pins 6 and 9), $T_A = 25^\circ\text{C}$ (CH-3,4) | | 10.5 | | |
| $I_{(BOM)}$ | Input bias current | $V_I = 0\text{ V}$ | | -200 | -500 | nA |
| $V_{(IOM)}$ | Input voltage range | $V_{CC} = 3.1\text{ V} \sim 12\text{ V}$ | | 0 to $V_{CC}-1.8$ | | V |

protection control section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|----------------------------------|--------------------------|------|------|------|---------------|
| $V_{(tPC)}$ | Input threshold voltage (pin 15) | $T_A = 25^\circ\text{C}$ | 1.45 | 1.50 | 1.55 | V |
| $V_{(stby)}$ | Standby voltage (pin 15) | | 40 | 70 | 100 | mV |
| V_I | Latched input voltage (pin 15) | | | 10 | 30 | mV |
| $I_{(bPC)}$ | Input source current (pin 15) | $T_A = 25^\circ\text{C}$ | -1 | -3 | -6 | μA |

oscillator section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|-----------------------------------|---|-----|-------|-----------|------|
| $f_{(OSC)}$ | Frequency | $C_t = 100\text{ pF}$, $R_t = 10\text{ k}\Omega$ | | 1 | | MHz |
| $f_{(dev)}$ | Standard deviation of frequency | All values are constant | | 7% | | |
| $f_{(dV)}$ | Frequency change with voltage | $V_{CC} = 3\text{ V} \sim 12\text{ V}$ | | 1% | | |
| $f_{(dT1)}$ | Frequency change with temperature | $T_A = 20^\circ\text{C to }25^\circ\text{C}$ | | -0.5% | $\pm 4\%$ | |
| $f_{(dT2)}$ | | $T_A = 25^\circ\text{C to }75^\circ\text{C}$ | | 0.5% | $\pm 4\%$ | |

TL1464I

QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6\text{ V}$, $f = 1\text{ MHz}$ (unless otherwise noted) (continued)

dead-time control section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---------------------------|-------------------------------|-----|-----|-----|---------------|
| $I_{(Idt)}$ | Input current | | | -1 | -4 | μA |
| $I_{(dt)}$ | Latched mode sink current | $T_A = 25^\circ\text{C}$ | 0.3 | 1 | 2 | mA |
| $V_{(dt)}$ | Latched input voltage | $I_{(dt)} = 100\ \mu\text{A}$ | | | 0.5 | V |
| V_{IO} | Input threshold voltage | Zero duty cycle | 0.6 | 0.7 | 0.8 | V |
| $V_{(tt00)}$ | | 100% duty cycle | 1.3 | 1.4 | 1.5 | |

error-amplifier section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--------------------------------------|--|--|----------------------|-----------|---------------|
| V_{IO} | Input offset voltage | $V_O = 1\text{ V}$ | | | ± 10 | mV |
| I_{IO} | Input offset current | $V_O = 1\text{ V}$ | | | ± 100 | nA |
| I_{IB} | Input bias current | $V_O = 1\text{ V}$ | | -200 | -500 | nA |
| V_{ICR} | Common-mode input voltage | CH-1,2 | $V_{CC} = 3.1\text{ V} \sim 12\text{ V}$ | -0.1 to $V_{CC}-1.8$ | | V |
| | | CH-3,4 | | 0 to $V_{CC}-1.8$ | | |
| $A_{(v)}$ | Open-loop voltage amplification | $R_I = 200\ \text{k}\Omega$ | 60 | 75 | | dB |
| B_1 | Unity-gain bandwidth | | | 6 | | MHz |
| CMRR | Common-mode rejection ratio | $V_{IC} = -0.1\text{ V} \sim V_{CC} - 1.8\text{ V}$ | 60 | 80 | | dB |
| V_{OM+} | Maximum output voltage swing | | $V_{ref}-0.1$ | | 0.2 | V |
| V_{OM-} | | | | | | |
| $I_{O(vr+)}$ | Output current (sink) | $V_{ID} = -0.1\text{ V}, V_O = 1.25\text{ V}$ | 0.5 | 1 | | mA |
| I_{I+} | Sink current (pin 24) (standby mode) | $V_I = 0.3\text{ V}$ (pin 24) $V_I = 0\text{ V}$ (pin 20) | 0.1 | 0.5 | | mA |
| I_{OM-} | Output current (source) | $V_{ID} = 0.1\text{ V}, V_O = 0.75\text{ V}$ | -45 | -85 | | μA |

output section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|-----------------------|------------------------------------|-----|-----|------|-------------|
| $I_{(SINK)}$ | Output current (sink) | $R_{(BIAS)} = 2.4\ \text{k}\Omega$ | 15 | 20 | 25 | mA |
| | | $R_{(BIAS)} = 5.8\ \text{k}\Omega$ | 7.5 | 10 | 12.5 | |

total device

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|------------------------|---------------------------------|-----|-----|-----|---------------|
| $I_{O(CS)}$ | Standby supply current | Standby pin input voltage = 0 V | | 1 | 200 | μA |
| $I_{O(CA)}$ | Average supply current | $R_f = 10\ \text{k}\Omega$ | | 4 | 7 | mA |

TL1464I

QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS266 – FEBRUARY 2000

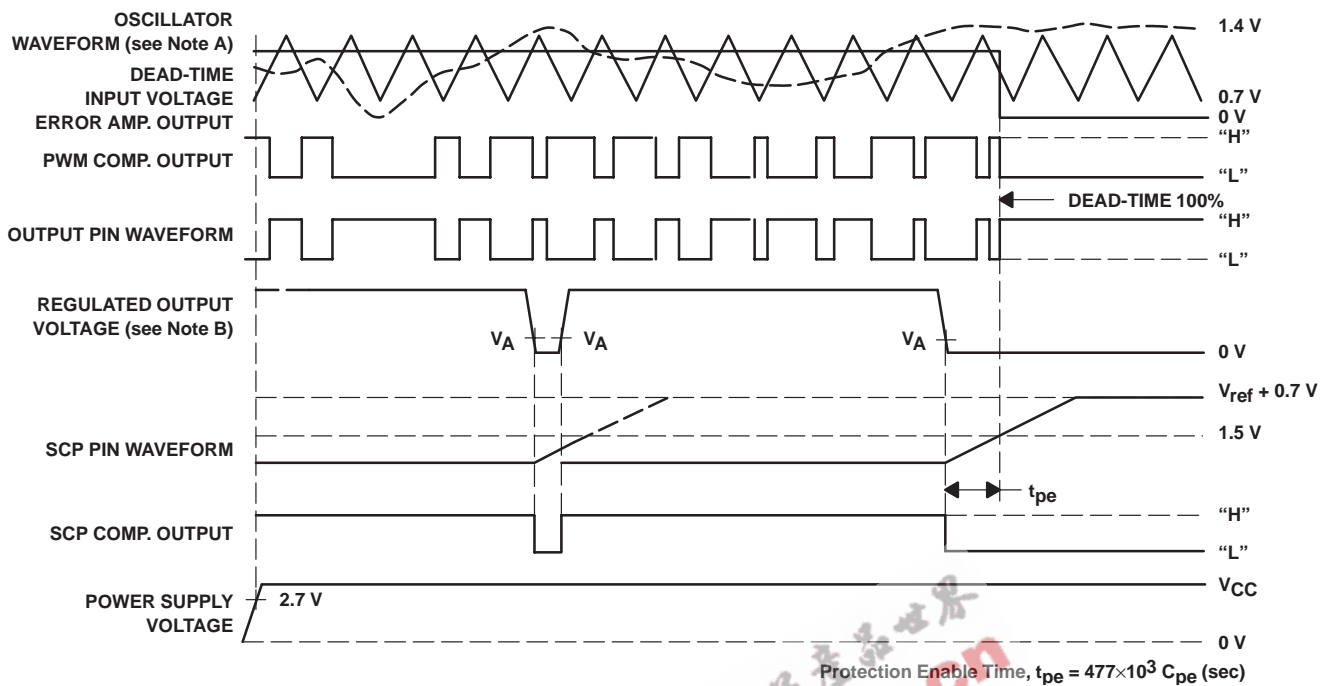


Figure 1. Timing Diagram (CH-1/CH-2)

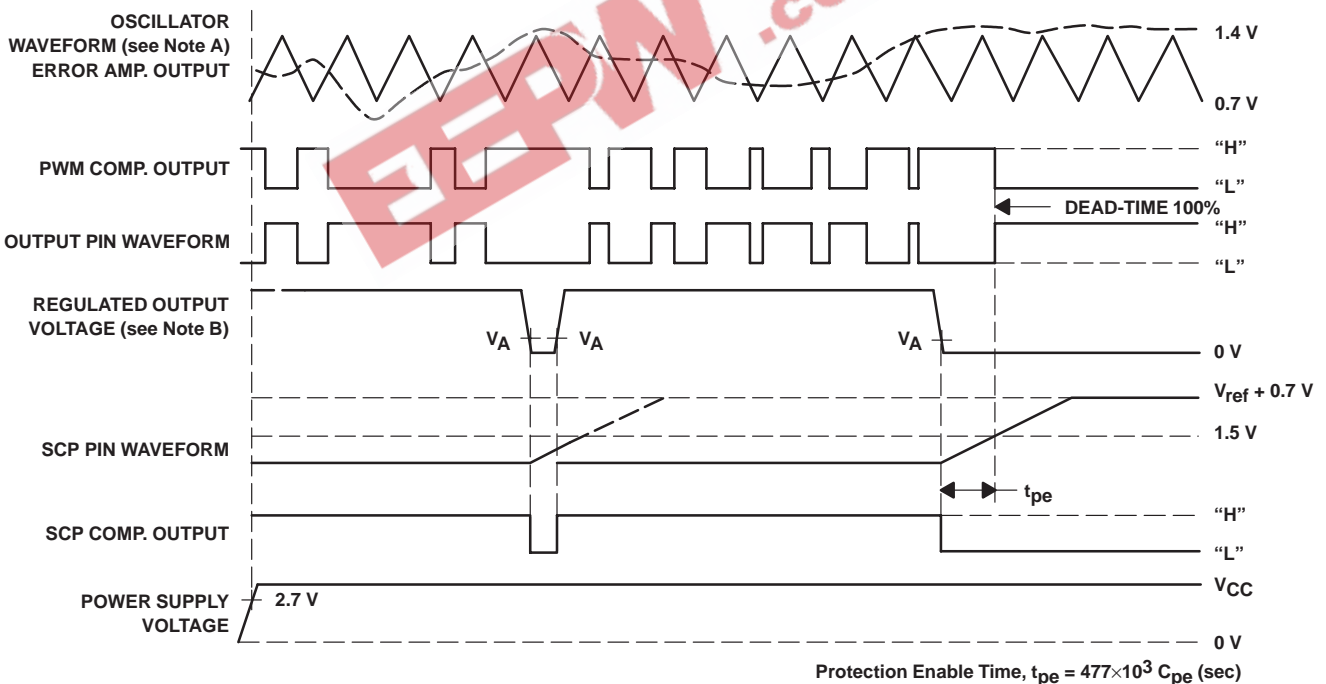


Figure 2. Timing Diagram (CH-3/CH-4)

- NOTES: A. Oscillator waveform of CH-1 and CH-2 is inverting output each other.
 B. V_A = input voltage of pin 29 (pin 24)

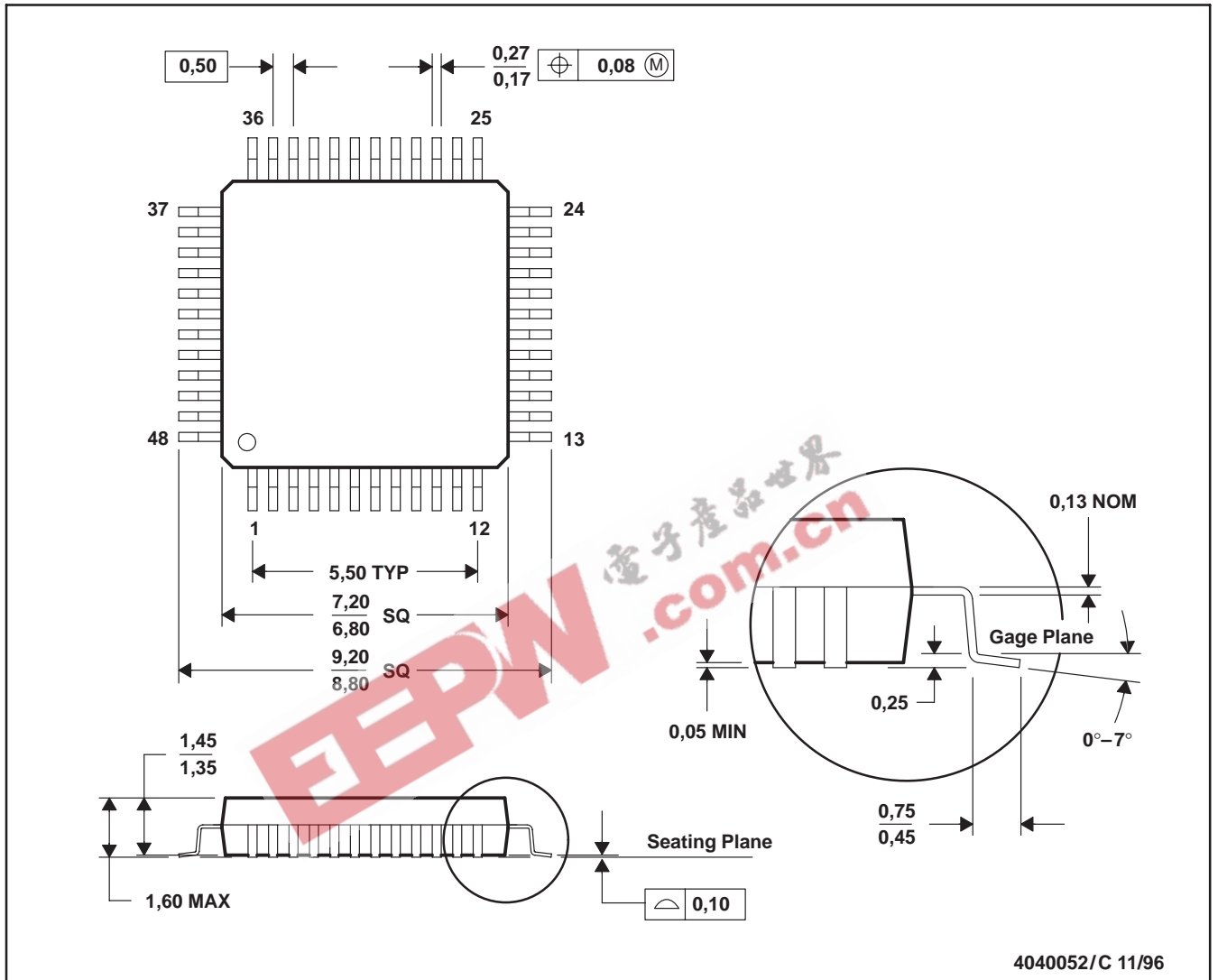
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QUAD PULSE-WIDTH-MODULATION CONTROL CIRCUIT

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MECHANICAL DATA

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. This may also be a thermally enhanced plastic package with leads connected to the die pads.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TL1464IPT | ACTIVE | LQFP | PT | 48 | 250 | TBD | CU NIPDAU | Level-2-220C-1 YEAR |
| TL1464IPTG4 | ACTIVE | LQFP | PT | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TL1464IPTR | ACTIVE | LQFP | PT | 48 | 1000 | TBD | CU NIPDAU | Level-2-220C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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