

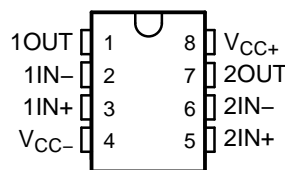
## FEATURES

- Operating Voltage... $\pm 2$  V to  $\pm 18$  V
- Low Offset Voltage...1 mV Max at 25°C, TL5580A
- Wide GBW...12 MHz Typ
- Slew Rate...5 V/ $\mu$ s Typ
- Low THD...0.0005% Typ
- Low-Noise Voltage...7 nV/ $\sqrt{\text{Hz}}$  at 1 kHz Typ

## APPLICATIONS

- Audio
- Test Equipment
- Industrial Process Controls
- Data-Acquisition Systems
- Active Filters
- Power-Supply Regulation

D, P, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The TL5580 is a dual bipolar operational amplifier that combines both high dc and ac performance with its low offset voltage, high-gain bandwidth, low harmonic distortion, and low-noise characteristics. In addition, its output is capable of driving 600- $\Omega$  loads. All these characteristics make the device ideally suited for use in audio, active filtering, and industrial measurement applications.

## ORDERING INFORMATION

$T_A$	$V_{IO}$ (25°C, MAX)	PACKAGE (1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	Standard grade 1.5 mV	PDIP – P	Tube of 50	TL5580IP	TL5580IP
		SOIC – D	Tube of 75	TL5580ID	Z5580
			Reel of 2500	TL5580IDR	
		TSSOP – PW	Tube of 150	TL5580IPW	Z5580
			Reel of 2000	TL5580IPWR	
				PDIP – P	
	A grade 1 mV	SOIC – D	Tube of 75	TL5580AID	Z5580A
			Reel of 2500	TL5580AIDR	
		TSSOP – PW	Tube of 150	TL5580AIPW	Z5580A
Reel of 2000			TL5580AIPWR		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

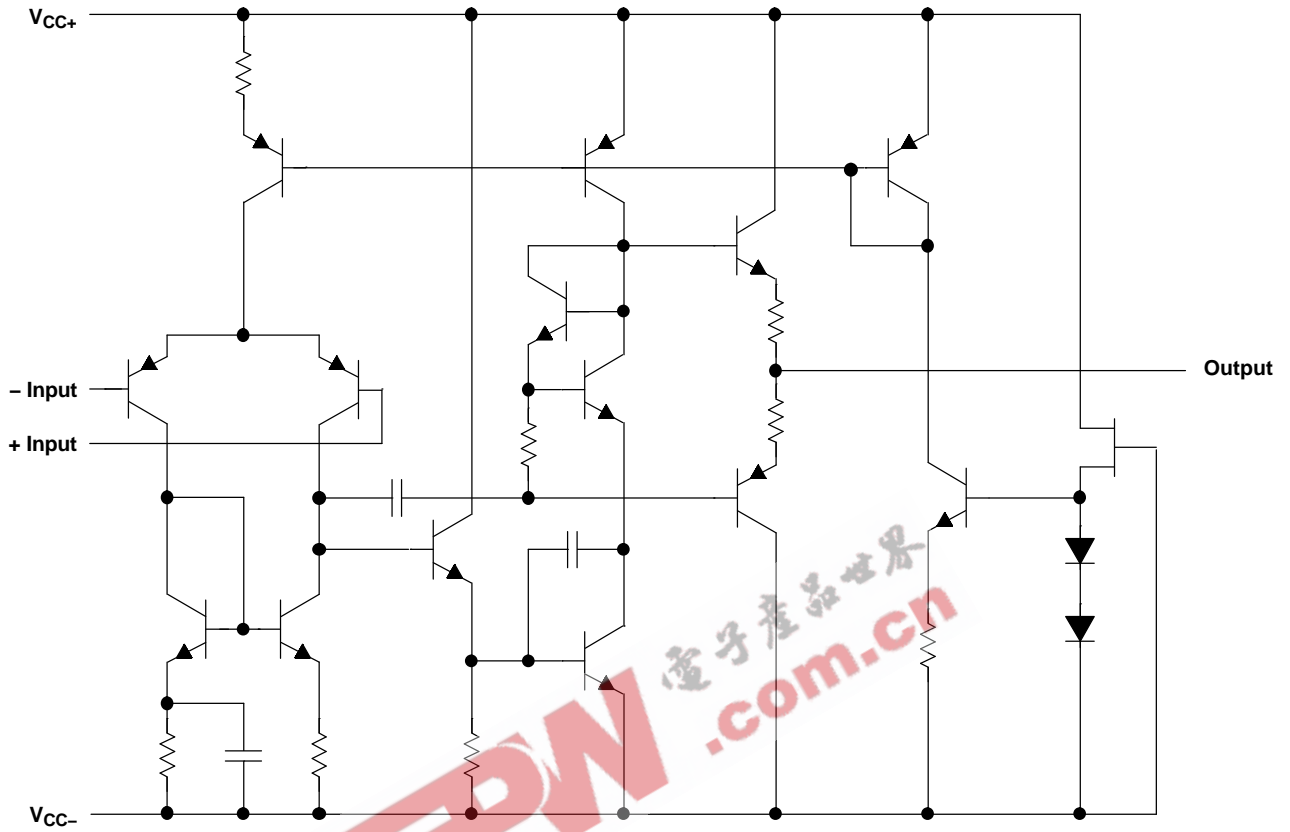


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# TL5580, TL5580A DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A—JUNE 2005—REVISED JULY 2005

## EQUIVALENT SCHEMATIC



### Absolute Maximum Ratings<sup>(1)</sup>

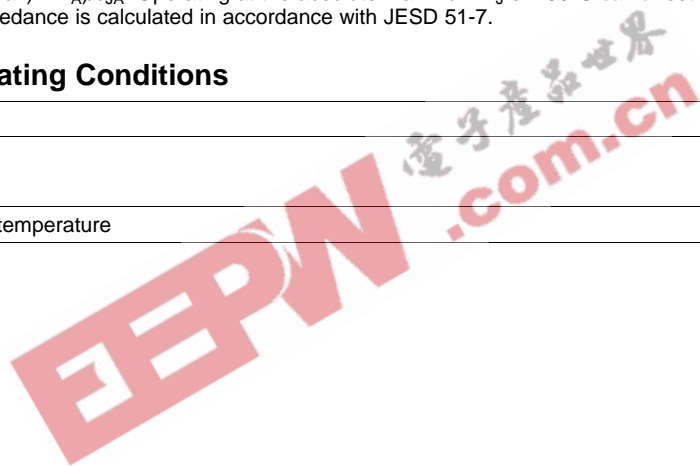
over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC±</sub>	Supply voltage		±18	V
V <sub>I</sub>	Input voltage (any input)		±15	V
V <sub>ID</sub>	Differential input voltage		±30	V
I <sub>O</sub>	Output current		±50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(2)(3)</sup>	D package		97
		P package		85
		PW package		149
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–60	125	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage	2	16	V
V <sub>CC-</sub>		–2	–16	
T <sub>A</sub>	Operating free-air temperature	–40	85	°C



# TL5580, TL5580A DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

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## Electrical Characteristics

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S \leq 10\text{ k}\Omega$	25°C		0.3	1	mV
			-40°C to 85°C			1.35	
			25°C		0.3	1.5	
			-40°C to 85°C			2	
$\alpha V_{IO}$	Average temperature coefficient of input offset voltage		-40°C to 85°C		1.8	5	$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current		25°C		5	75	nA
			-40°C to 85°C			100	
$I_{IB}$	Input bias current		25°C		100	500	nA
			-40°C to 85°C			800	
$A_{VD}$	Large-signal differential-voltage amplification	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	25°C		90	110	dB
			-40°C to 85°C			87	
$V_{OM}$	Output voltage swing	$R_L \geq 2\text{ k}\Omega$	25°C		12.75 -12.25	$\pm 13.5$	V
			-40°C to 85°C			12.5 -12	
$V_{ICR}$	Common-mode input voltage range		25°C		$\pm 13$	$\pm 13.5$	V
			-40°C to 85°C			$\pm 12$	
CMRR	Common-mode rejection ratio	$R_S \leq 10\text{ k}\Omega, V_{ICR} = -12\text{ V to } 12\text{ V}$	25°C		90	110	dB
			-40°C to 85°C			85	
$k_{SVR}^{(1)}$	Supply-voltage rejection ratio	$R_S \leq 10\text{ k}\Omega$	25°C		85	110	dB
			-40°C to 85°C			83	
$I_{CC}$	Supply current (all amplifiers)		25°C		6	9	mA
			-40°C to 85°C				

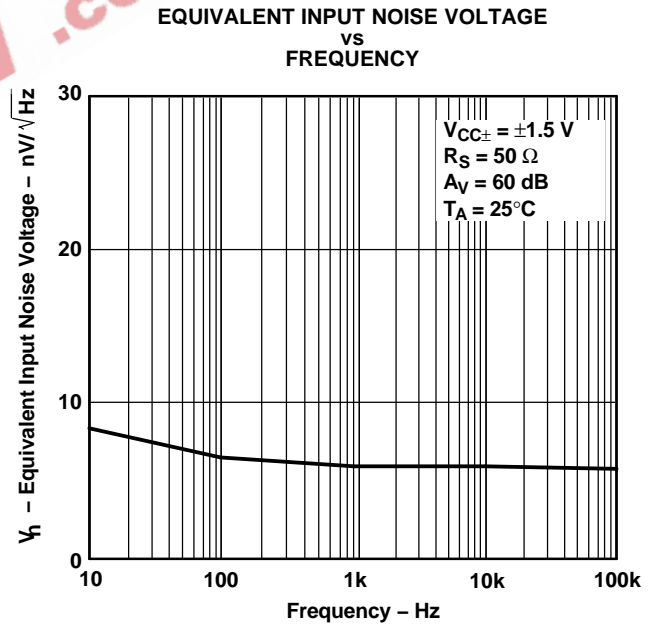
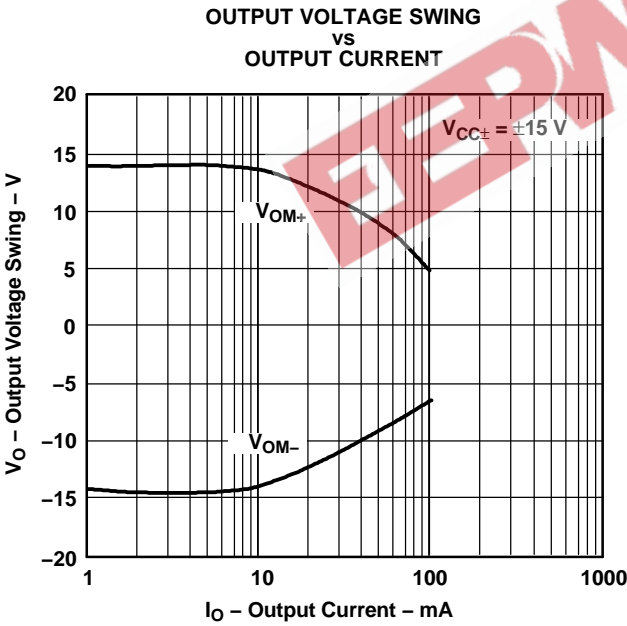
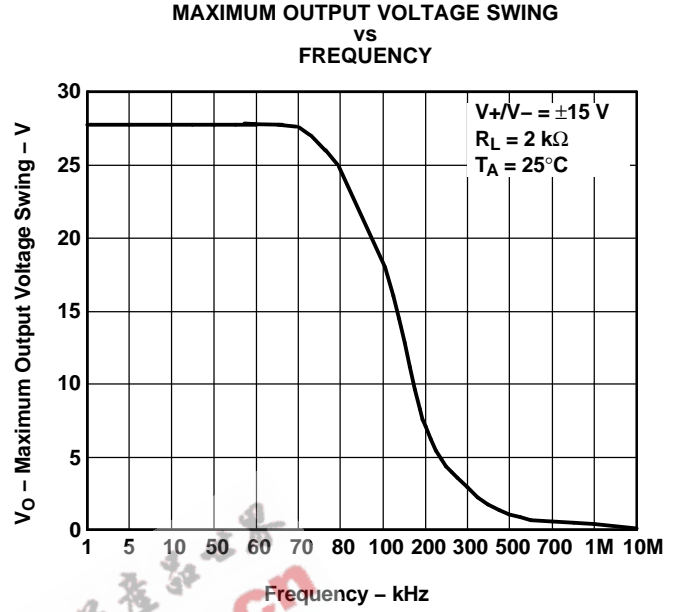
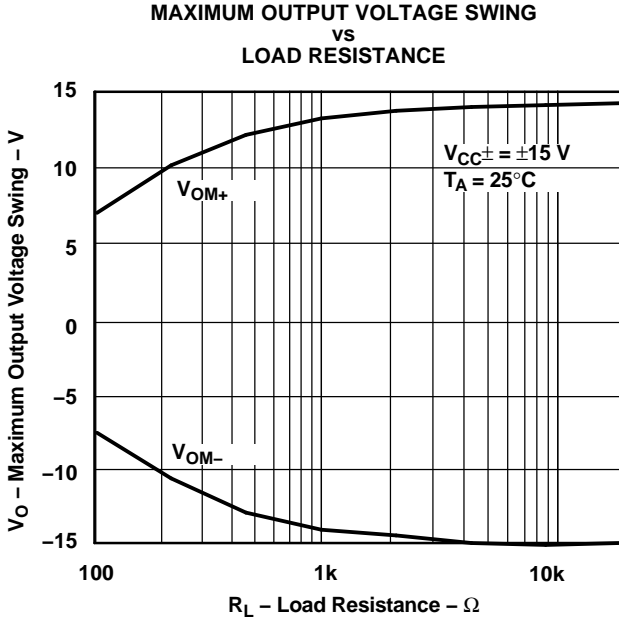
(1) Measured with  $V_{CC\pm}$  varied simultaneously

## Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}, T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \geq 2\text{ k}\Omega$	5	$\text{V}/\mu\text{s}$
GBW	Gain bandwidth product	$f = 10\text{ kHz}$	12	MHz
THD	Total harmonic distortion	$V_O = 5\text{ V}, R_L = 2\text{ k}\Omega, f = 1\text{ kHz}, A_{VD} = 20\text{ dB}$	0.0005	%
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	7	$\text{nV}/\sqrt{\text{Hz}}$

**TYPICAL CHARACTERISTICS**



TL5580, TL5580A  
 DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A-JUNE 2005-REVISED JULY 2005

TYPICAL CHARACTERISTICS (continued)

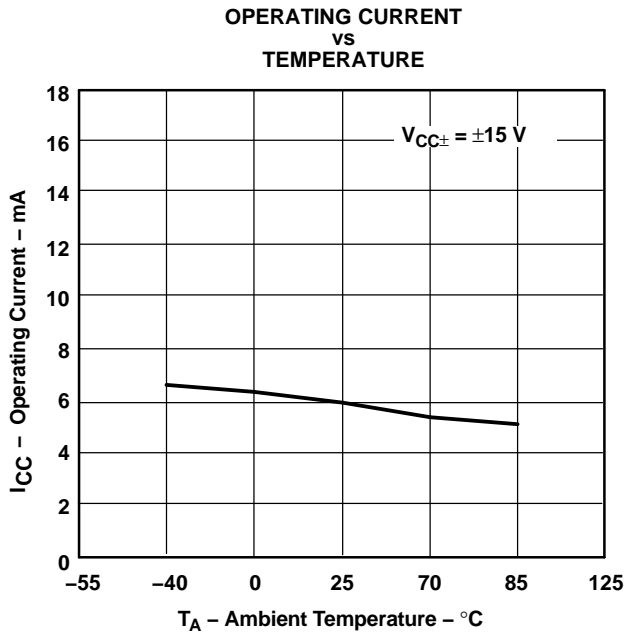


Figure 5.

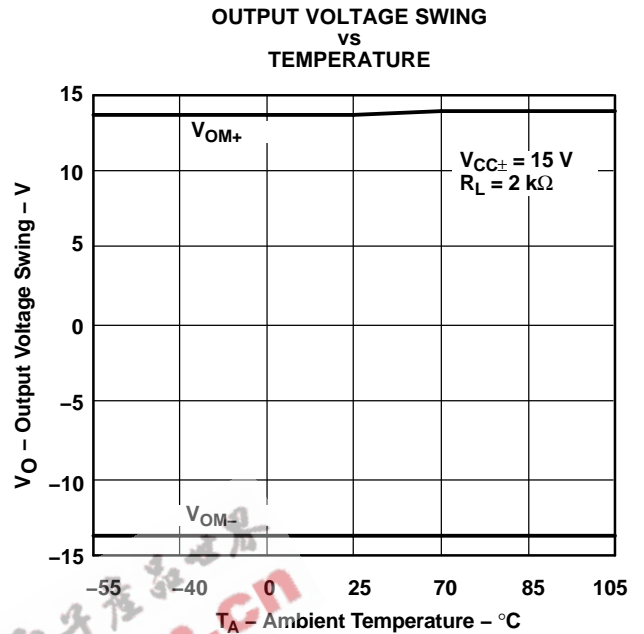


Figure 6.

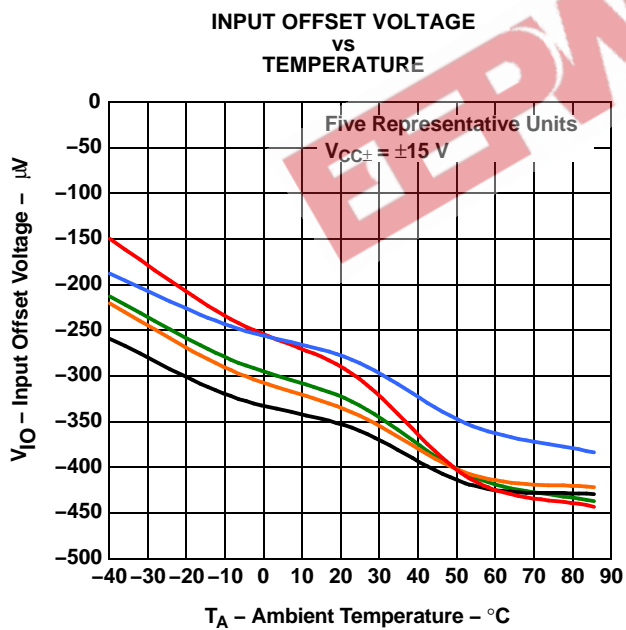


Figure 7.

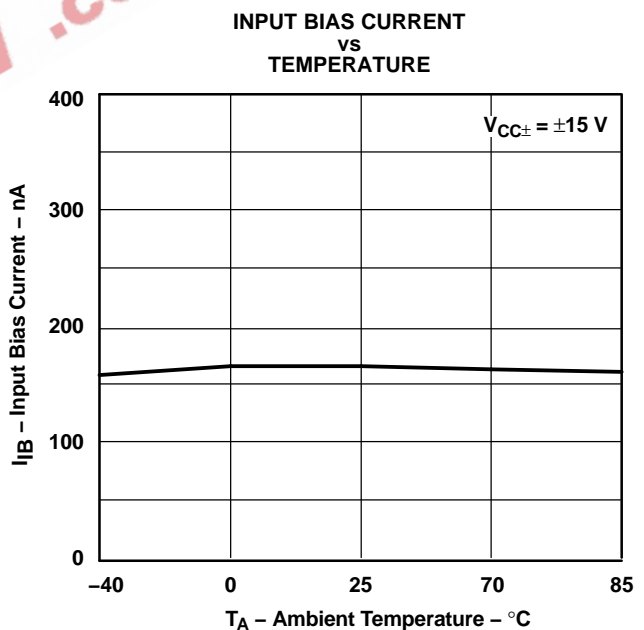


Figure 8.

**TYPICAL CHARACTERISTICS (continued)**

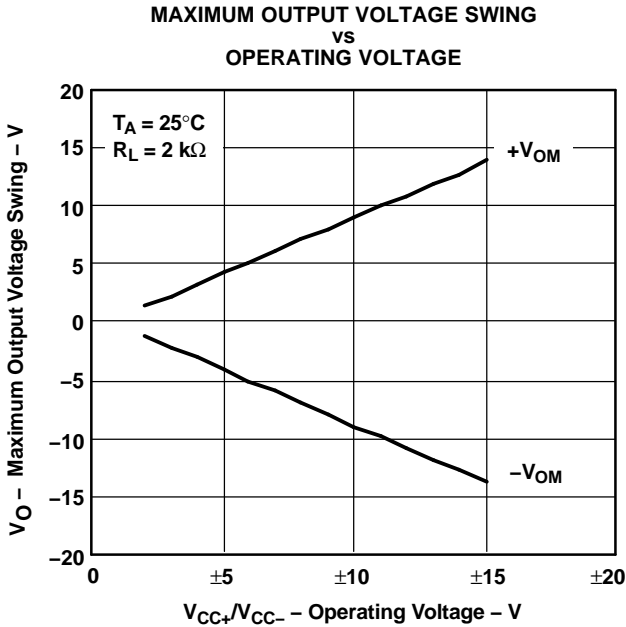


Figure 9.

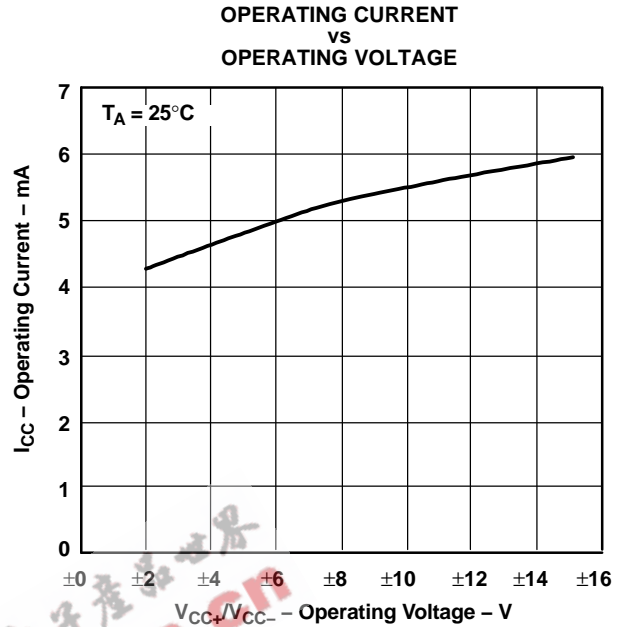


Figure 10.

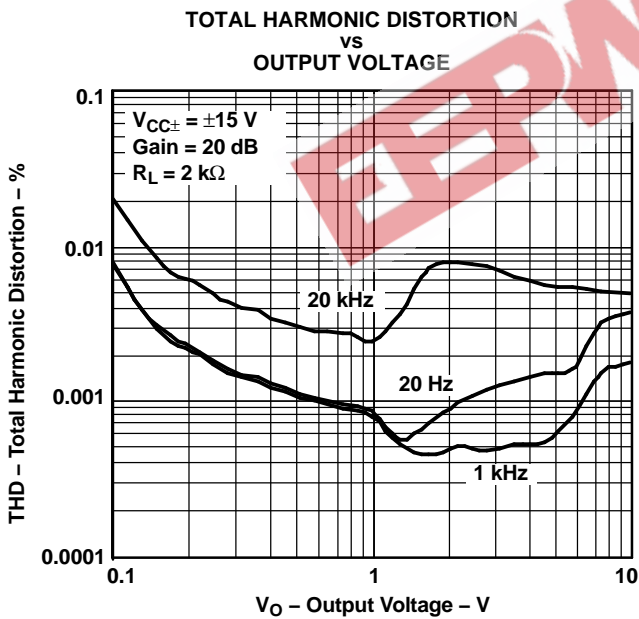


Figure 11.

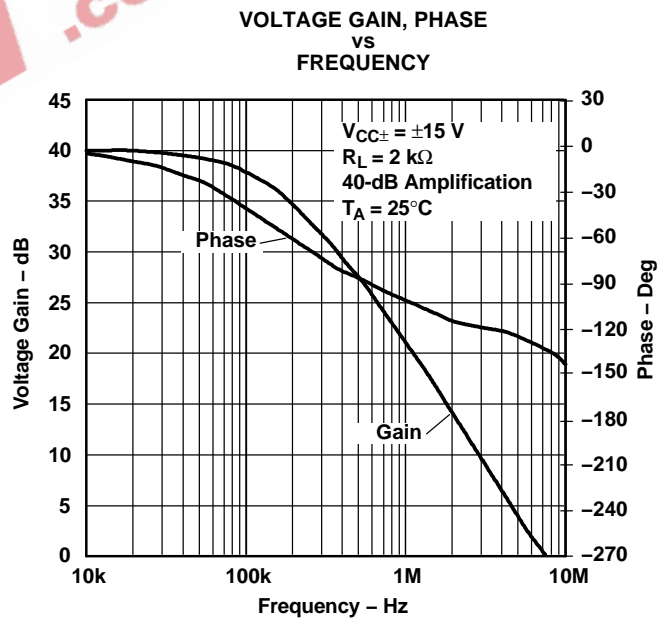


Figure 12.

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL5580AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580AIP E4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.



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**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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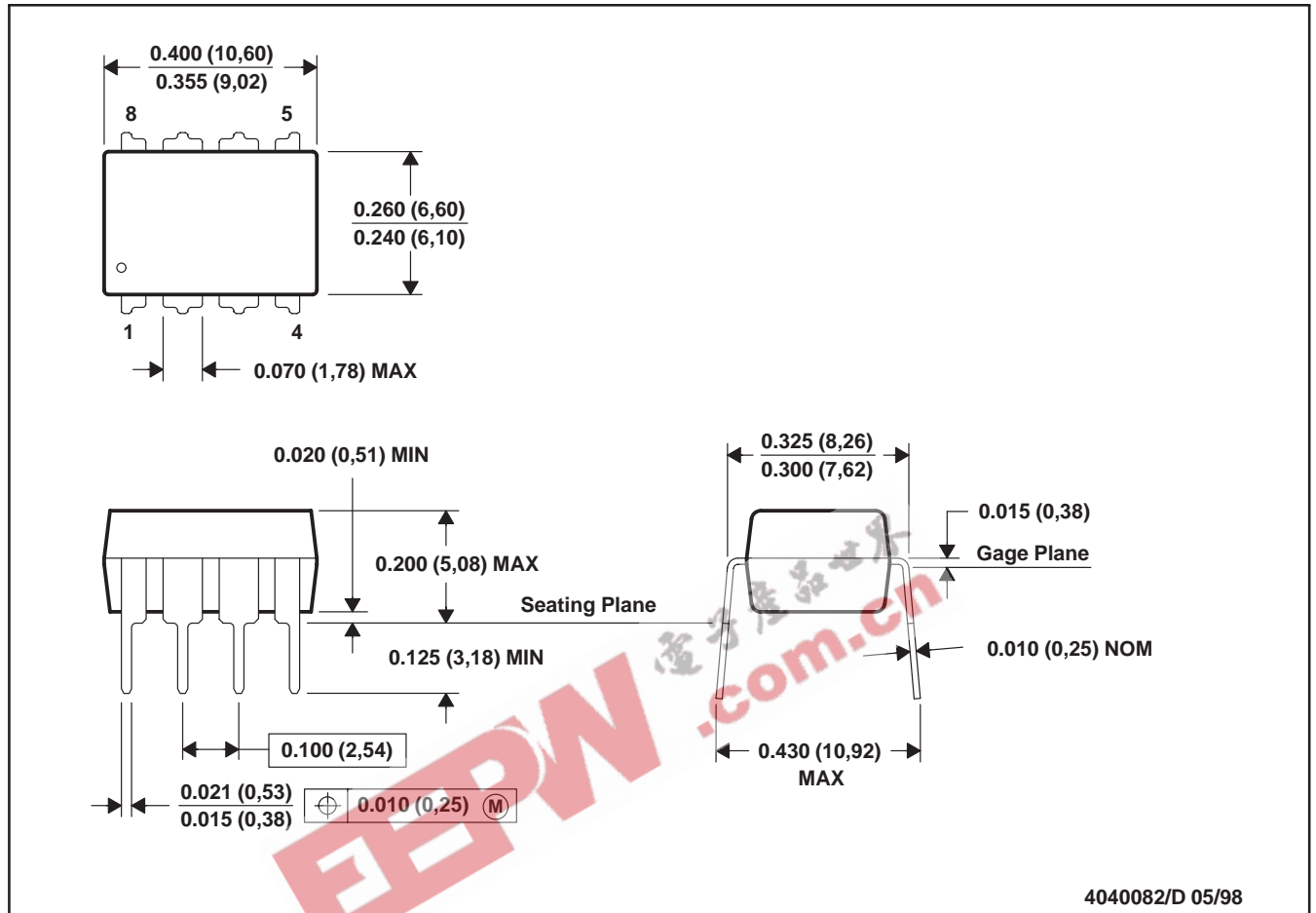
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# MECHANICAL DATA

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE



4040082/D 05/98

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

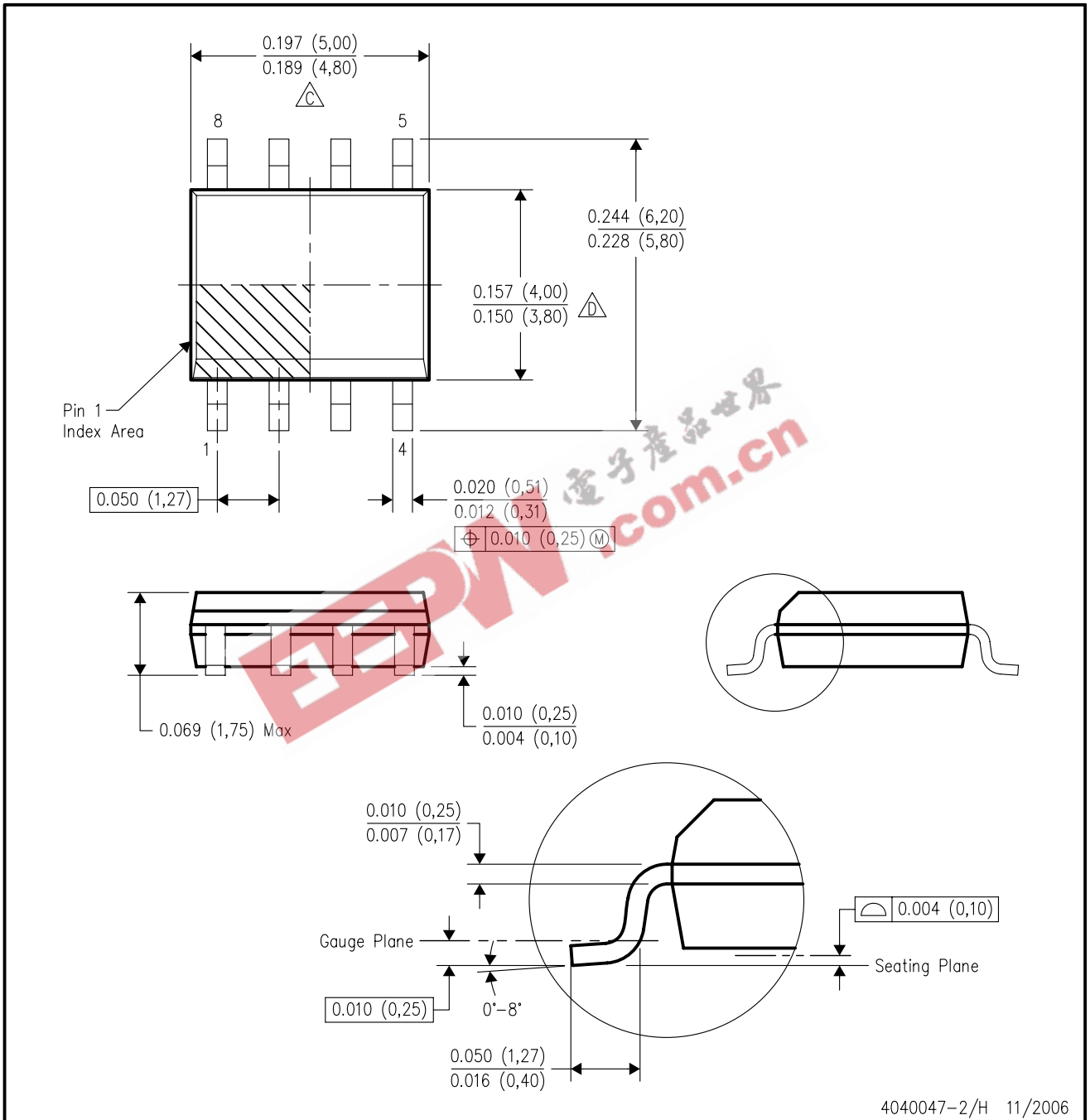


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# MECHANICAL DATA

## D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

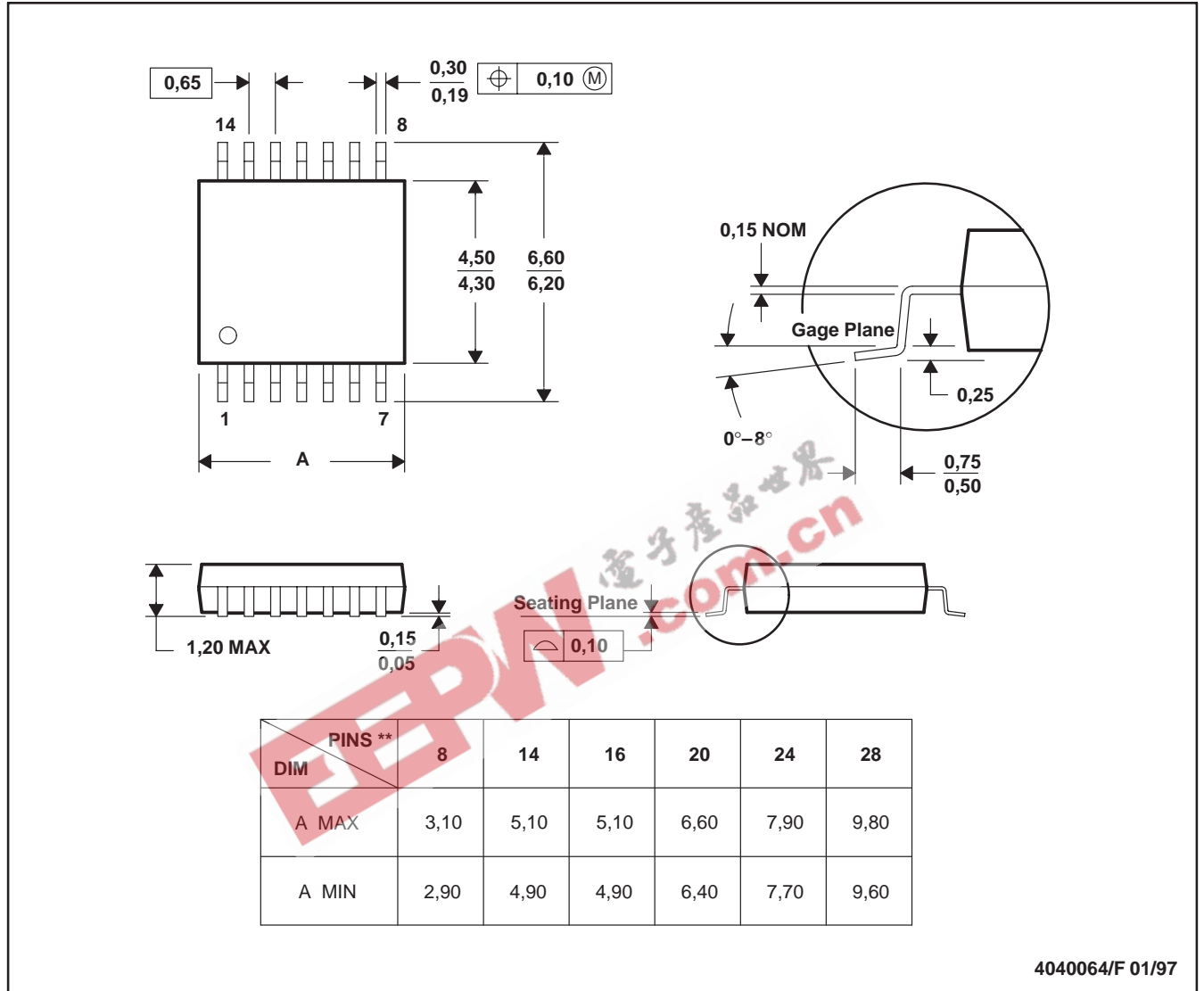
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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