

# TLP701

Industrial inverters  
 Inverter for air conditioners  
 IGBT/Power MOS FET gate drive

TLP701 consists of a GaAlAs light-emitting diode and an integrated photodetector.

This unit is 6-lead SDIP package. The TLP701 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The TLP701 is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP701 is capable of "direct" gate driving of low-power IGBTs.

- Peak output current :  $\pm 0.6$  A (max)
- Guaranteed performance over temperature :  $-40$  to  $100^\circ\text{C}$
- Supply current : 2 mA (max)
- Power supply voltage : 10 to 30 V
- Threshold input current :  $I_{FLH} = 5$  mA (max)
- Switching time ( $t_{pLH} / t_{pHL}$ ) : 700 ns (max)
- Common mode transient immunity :  $\pm 10$  kV/ $\mu\text{s}$  (min)
- Isolation voltage : 5000 Vrms (min)
- Construction mechanical rating

	7.62-mm pitch standard type	10.16-mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

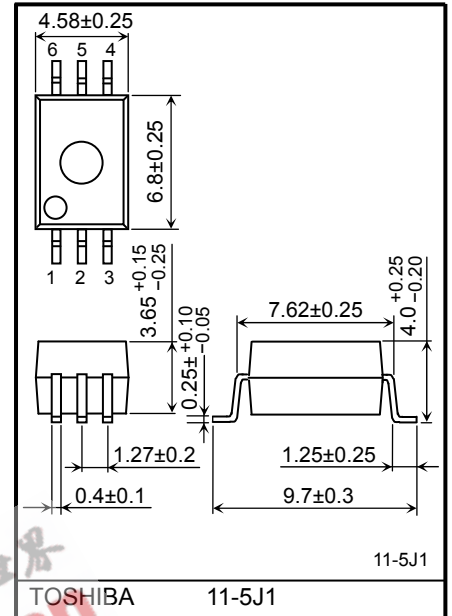
- UL Recognized : UL1577, File No. E67349
- Option (D4) TÜV approved : EN60747-5-2 Certificate No. R50033433  
 Maximum operating insulation voltage : 890 Vpk  
 Highest permissible over voltage : 8000 Vpk

( Note ) When a EN60747-5-2 approved type is needed, please designate the "Option(D4)"

### Truth Table

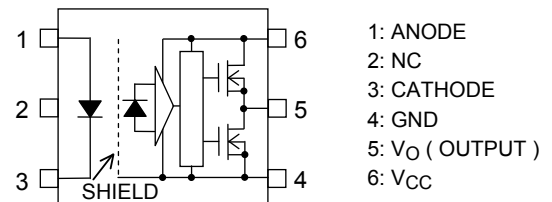
Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Unit in mm

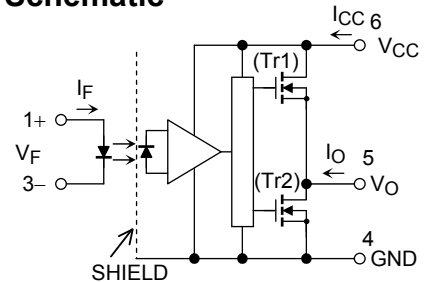


Weight : 0.26 g (typ.)

### Pin Configuration (Top View)



### Schematic



A 0.1- $\mu\text{F}$  bypass capacitor must be connected between pins 6 and 4. (See Note 6.)

**Absolute Maximum Ratings (Ta = 25 °C)**

Characteristics		Symbol	Rating	Unit
LED	Forward current	I <sub>F</sub>	20	mA
	Forward current derating (Ta ≥ 85°C)	ΔI <sub>F</sub> /ΔTa	-0.54	mA/°C
	Peak transient forward current (Note 1)	I <sub>FP</sub>	1	A
	Reverse voltage	V <sub>R</sub>	5	V
	Junction temperature	T <sub>j</sub>	125	°C
Detector	“H” peak output current (Note 2)	I <sub>OPH</sub>	-0.6	A
	“L” peak output current (Note 2)	I <sub>OPL</sub>	0.6	A
	Output voltage	V <sub>O</sub>	35	V
	Supply voltage	V <sub>CC</sub>	35	V
	Junction temperature	T <sub>j</sub>	125	°C
Operating frequency (Note 3)	f	25	kHz	
Operating temperature range	T <sub>opr</sub>	-40 to 100	°C	
Storage temperature range	T <sub>stg</sub>	-55 to 125	°C	
Lead soldering temperature (10 s) (Note 4)	T <sub>sol</sub>	260	°C	
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)	BV <sub>S</sub>	5000	V <sub>rms</sub>	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width P<sub>W</sub> ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P<sub>W</sub> ≤ 2 μs, f ≤ 15 kHz

Note 3: Exponential waveform I<sub>OPH</sub> ≤ -0.3 A (≤ 2 μs), I<sub>OPL</sub> ≤ +0.3 A (≤ 2 μs), Ta = 100 °C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Note 6: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.  
The total lead length between capacitor and coupler should not exceed 1 cm.

**Recommended Operating Conditions**

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	I <sub>F</sub> (ON)	7.5	—	10	mA
Input voltage, OFF	V <sub>F</sub> (OFF)	0	—	0.8	V
Supply voltage	V <sub>CC</sub>	10	—	30	V
Peak output current	I <sub>OPH</sub> / I <sub>OPL</sub>	—	—	± 0.2	A
Operating temperature	T <sub>opr</sub>	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) < 0.5 μs.

## Electrical Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		V <sub>F</sub>	—	I <sub>F</sub> = 5 mA, Ta = 25 °C		—	1.55	1.70	V
Temperature coefficient of forward voltage		ΔV <sub>F</sub> /ΔTa	—	I <sub>F</sub> = 5 mA		—	-2.0	—	mV/°C
Input reverse current		I <sub>R</sub>	—	V <sub>R</sub> = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance		C <sub>T</sub>	—	V = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output current (Note 8)	"H" Level	I <sub>OPH1</sub>	1	V <sub>CC</sub> = 15 V I <sub>F</sub> = 5 mA	V <sub>6-5</sub> = 4 V	-0.2	-0.38	—	A
		I <sub>OPH2</sub>			V <sub>6-5</sub> = 10 V	-0.4	-0.60	—	
	"L" Level	I <sub>OPL1</sub>	2	V <sub>CC</sub> = 15 V I <sub>F</sub> = 0 mA	V <sub>5-4</sub> = 2 V	0.2	0.36	—	
		I <sub>OPL2</sub>			V <sub>5-4</sub> = 10 V	0.4	0.62	—	
Output voltage	"H" Level	V <sub>OH</sub>	3	V <sub>CC</sub> = 10 V	I <sub>O</sub> = -100 mA, I <sub>F</sub> = 5 mA	6.0	8.5	—	V
	"L" Level	V <sub>OL</sub>			4	I <sub>O</sub> = 100 mA, V <sub>F</sub> = 0.8 V	—	0.4	
Supply current	"H" Level	I <sub>CCH</sub>	5	V <sub>CC</sub> = 10 to 30 V V <sub>O</sub> = Open	I <sub>F</sub> = 10 mA	—	1.4	2.0	mA
	"L" Level	I <sub>CCL</sub>			6	I <sub>F</sub> = 0 mA	—	1.3	
Threshold input current	L → H	I <sub>FLH</sub>	—	V <sub>CC</sub> = 15 V, V <sub>O</sub> > 1 V		—	2.5	5	mA
Threshold input voltage	H → L	V <sub>FHL</sub>	—	V <sub>CC</sub> = 15 V, V <sub>O</sub> < 1 V		0.8	—	—	V
Supply voltage		V <sub>CC</sub>	—	—		10	—	30	V

(\*): All typical values are at Ta = 25°C

Note 8: Duration of I<sub>O</sub> time ≤ 50 μs, 1 pulse

Note 9: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.

It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

## Isolation Characteristics (Ta = 25 °C)

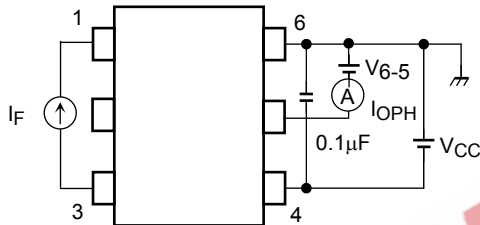
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C <sub>S</sub>	V = 0 V, f = 1MHz (Note 5)	—	1.0	—	pF
Isolation resistance	R <sub>S</sub>	R.H. ≤ 60 %, V <sub>S</sub> = 500 V (Note 5)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	BV <sub>S</sub>	AC, 1 minute	5000	—	—	V <sub>rms</sub>
		AC, 1 second, in oil	—	10000	—	
		DC, 1 minute, in oil	—	10000	—	V <sub>dc</sub>

## Switching Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

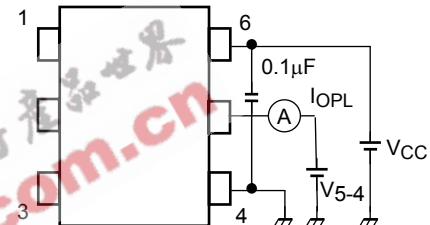
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	V <sub>CC</sub> = 30 V R <sub>g</sub> = 47 Ω C <sub>g</sub> = 3 nF	I <sub>F</sub> = 0 → 5 mA	100	—	700	ns
	H → L			I <sub>F</sub> = 5 → 0 mA	100	—	700	
Output rise time (10–90 %)	t <sub>r</sub>	7	V <sub>CC</sub> = 30 V R <sub>g</sub> = 47 Ω C <sub>g</sub> = 3 nF	I <sub>F</sub> = 0 → 5 mA	—	50	—	ns
Output fall time (90–10 %)	t <sub>f</sub>			I <sub>F</sub> = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF	t <sub>pHL</sub> - t <sub>pLH</sub>	8	V <sub>CM</sub> = 1000 Vp-p V <sub>CC</sub> = 30 V Ta = 25 °C	I <sub>F</sub> = 0, 5 mA	-500	—	500	V/μs
Common mode transient immunity at HIGH level output	CM <sub>H</sub>			I <sub>F</sub> = 5 mA V <sub>O</sub> (min) = 26 V	-10000	—	—	
Common mode transient immunity at LOW level output	CM <sub>L</sub>			I <sub>F</sub> = 0 mA V <sub>O</sub> (max) = 1 V	10000	—	—	

(\*): All typical values are at Ta = 25 °C.

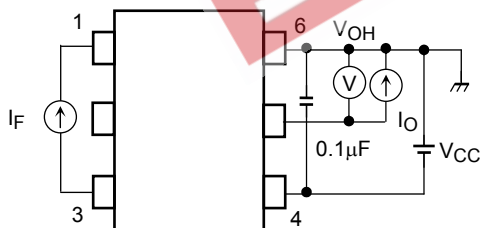
**Test Circuit 1: I<sub>OPH</sub>**



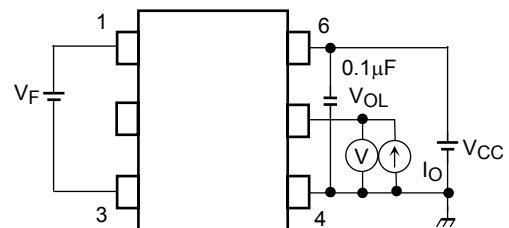
**Test Circuit 2: I<sub>OPL</sub>**



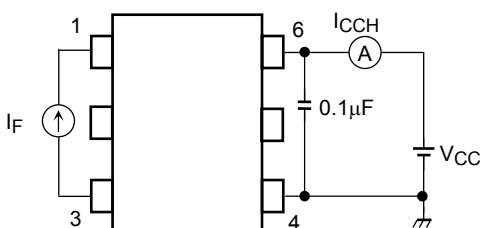
**Test Circuit 3: V<sub>OH</sub>**



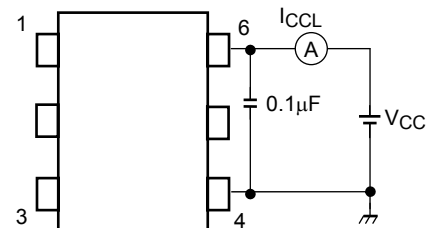
**Test Circuit 4: V<sub>OL</sub>**



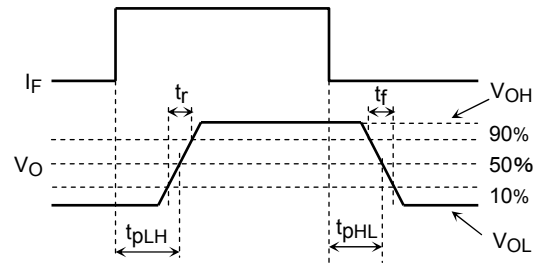
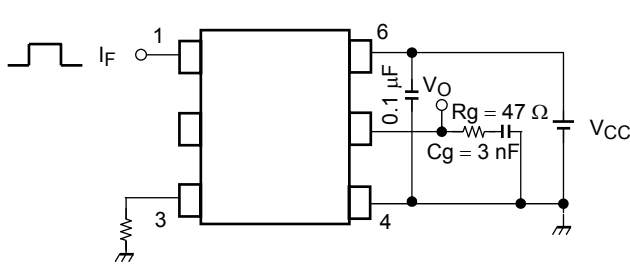
**Test Circuit 5: I<sub>CCH</sub>**



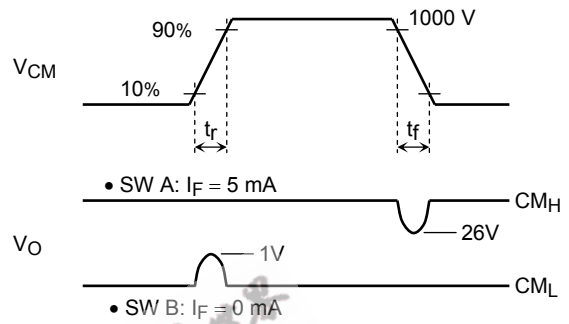
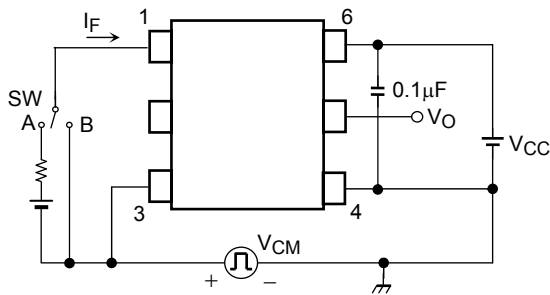
**Test Circuit 6: I<sub>CCL</sub>**



Test Circuit 7:  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_r$ ,  $t_f$ , PDD



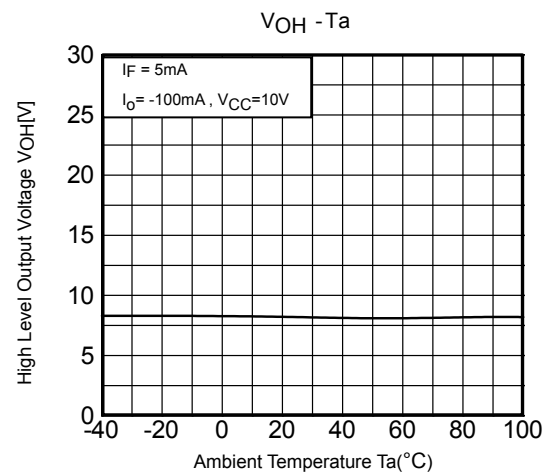
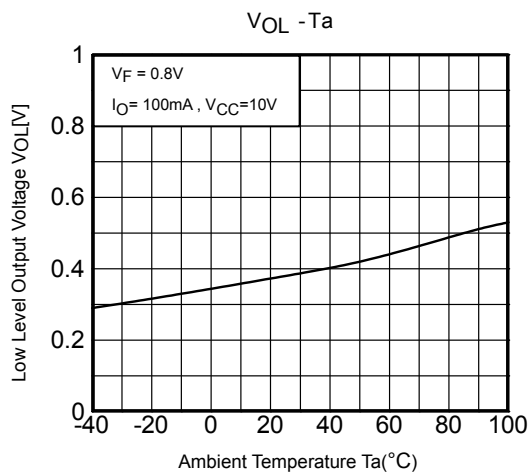
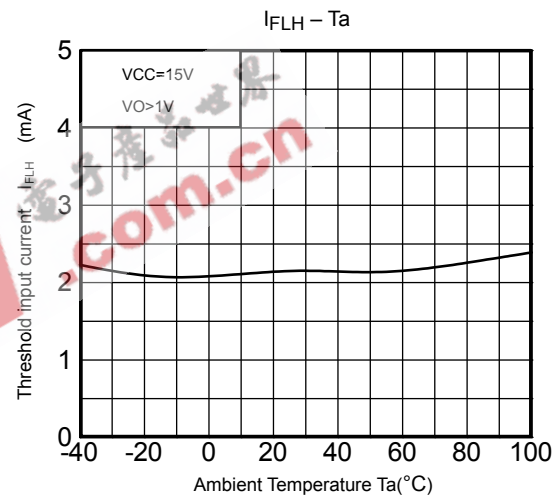
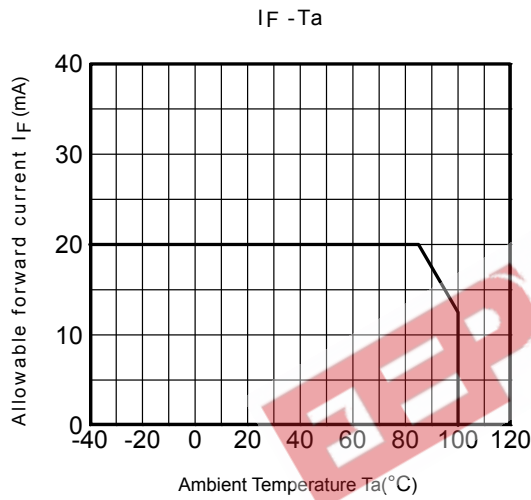
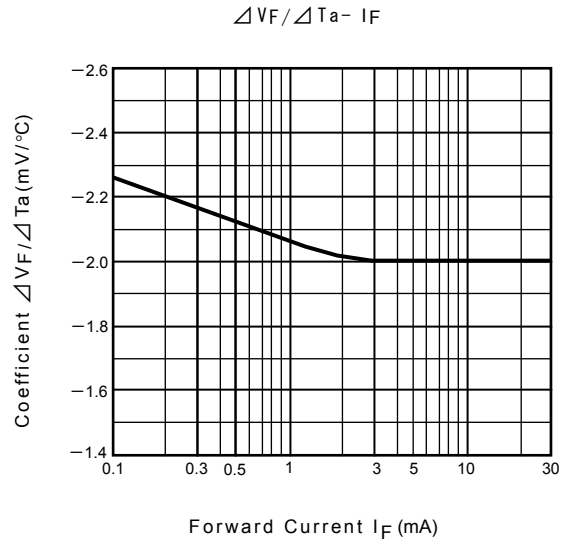
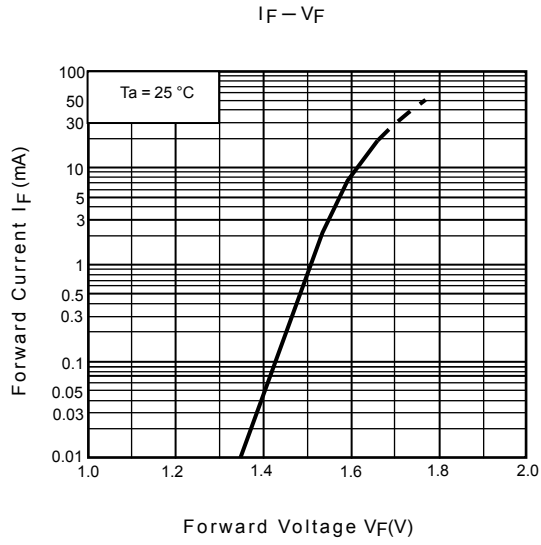
Test Circuit 8:  $CM_H$ ,  $CM_L$



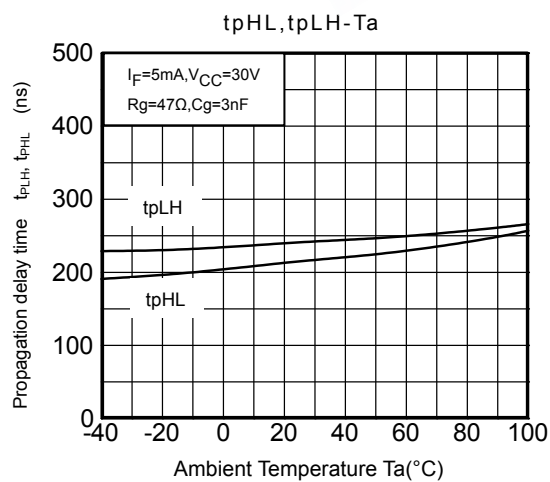
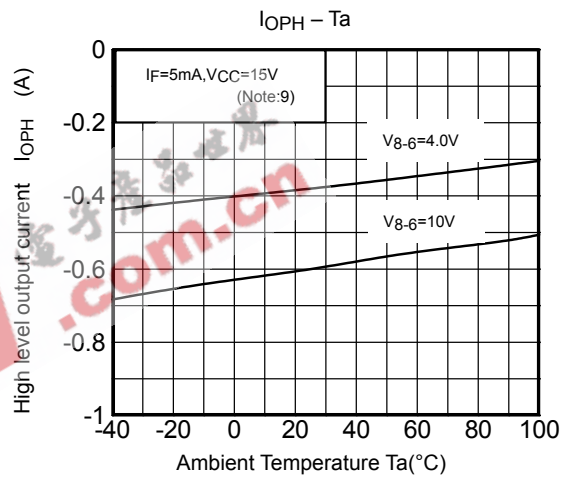
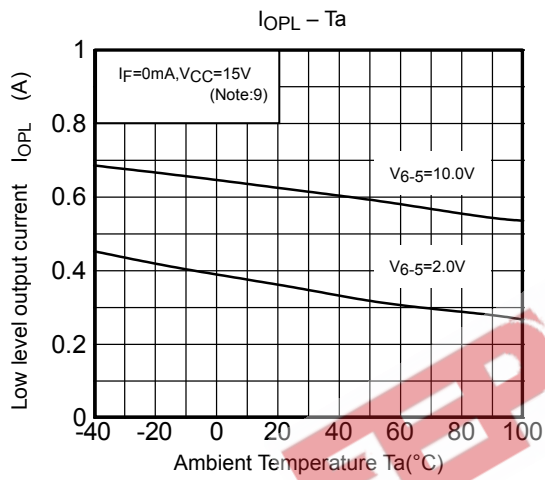
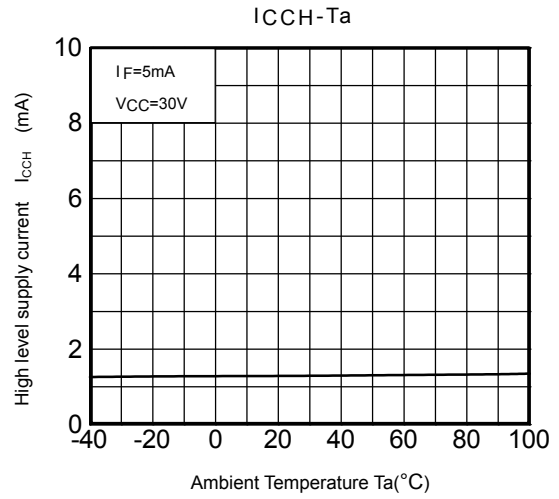
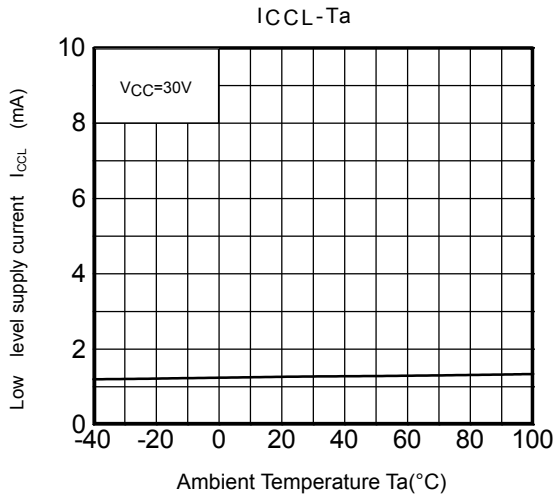
$$CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

$$CM_H = -\frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$CM_L$  ( $CM_H$ ) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.



\*: The above graphs show typical characteristics.



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