

DUAL WIDE BAND OPERATIONAL AMPLIFIER WITH HIGH OUTPUT CURRENT

■ LOW NOISE : 3nV/√Hz, 1.2pA/√Hz ■ HIGH OUTPUT CURRENT : 200mA

■ VERY LOW HARMONIC AND INTERMODU-LATION DISTORTION

HIGH SLEW RATE : 40V/μsSPECIFIED FOR 25Ω LOAD

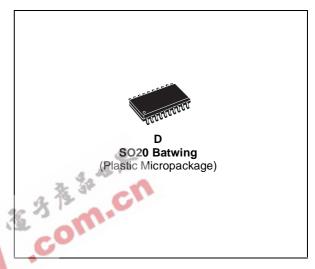
DESCRIPTION

The TS612 is a dual operational amplifier featuring a high output current (200mA min.), large gain-bandwidth product (130MHz) and capable of driving a 25Ω load with a 160mA output current at $\pm 6V$ power supply.

This device is particularly intended for applications where multiple carriers must be amplified simultaneously with very low intermodulation products.

The TS612 is housed in SO20 batwing plastic package for a very low thermal resistance.

The TS612 is fitted out with Power Down function in order to decrease the consumption.

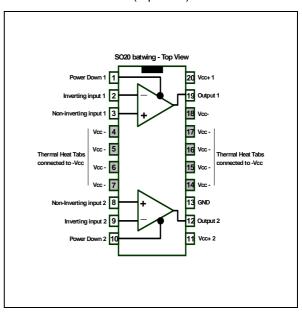


ORDER CODE

Part Number	Temperature Range	Package
Part Number	remperature Namye	D
TS612ID	-40, +85°C	•

D=Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



APPLICATION

■ UPSTREAM line driver for Asymmetric Digital Subscriber Line (ADSL) (NT).

December 2002 1/10

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage 1)	±7	V
V _{id}	Differential Input Voltage ²⁾	±2	V
V _{in}	Input Voltage Range 3)	±6	V
T _{oper}	Operating Free Air Temperature Range TS612ID, TS612IPT	-40 to + 85	°C
T _{std}	Storage Temperature	-65 to +150	°C
Tj	Maximum Junction Temperature	150	°C
	Output Short Circuit Duration	4)	
SO20-Bat	wing		
R _{thjc}	Thermal Resistance Junction to Case	25	°C/W
R _{thja}	Thermal Resistance Junction to Ambient Area	45	°C/W
P _{max.}	Maximum Power Dissipation (@25°C)	2.7	W

- All voltages values, except differential voltage are with respect to network terminal.
- 2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
- The magnitude of input and output voltages must never exceed V_{CC} +0.3V.
 An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.

OPERATING CONDITIONS

Symbol	Parameter		36 m	Value	Unit
V _{CC}	Supply Voltage		CO.	±2.5 to ±6	V
V _{icm}	Common Mode Input Voltage	1		(V_{CC}^{-}) +2 to (V_{CC}^{+}) -1	V

ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 6 Volts$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max	Unit
DC PER	FORMANCE		ı			<u> </u>
V	Input Offcot Voltage	T _{amb}	-6	-1	6	mV
V_{io}	Input Offset Voltage	$T_{min.} < T_{amb} < T_{max.}$			10	1111
ΔV_{io}	Differential Input Offset Voltage	T _{amb} = 25°C			6	mV
l _{io}	Input Offset Current	T _{amb}		0.2	3	μΑ
10	Imput Offset Guiterit	$T_{min.} < T_{amb} < T_{max.}$			5	μΛ
l _{ib}	Input Bias Current	T _{amb}		5	15	μА
·ID	Imput Blad Gulletti	$T_{min.} < T_{amb} < T_{max.}$			30	μπ
CMR	Common Mode Rejection Ratio	$V_{ic} = \pm 2V, T_{amb}$	90	108		dB
OWIT	Common Wode Rejection Ratio	$T_{min.} < T_{amb} < T_{max.}$	70			
SVR	Supply Voltage Rejection Ratio	$V_{ic} = \pm 6V \text{ to } \pm 4V, T_{amb}$	70	88		dB
OVIC	Cupply voltage Rejection Ratio	$T_{\text{min.}} < T_{\text{amb}} < T_{\text{max.}}$	50			
I _{CC}	Total Supply Current per Operator	No load, $V_{out} = 0$	CL	14		mA
DYNAM	IC PERFORMANCE and OUTPUT CI	HARACTERISTICS				_
V_{OH}	High Level Output Voltage	I _{out} = 160mA R _L connected to GND	4	4.5		V
V_{OL}	Low Level Output Voltage	I _{out} = 160mA R _L connected to GND		-4.5	-4	V
A_{VD}	Large Signal Voltage Gain	$V_{out} = 7V \text{ peak}$ $R_L = 25\Omega, T_{amb}$	6500	11000		V/V
		$T_{min.} < T_{amb} < T_{max.}$	5000			
GBP	Gain Bandwidth Product	A_{VCL} = +11, f = 20MHz R_L = 100 Ω	80	130		MHz
SR	Slew Rate	$A_{VCL} = +7, R_L = 50\Omega$	23	40		V/μs
I _{sink}	Output Short Circuit Current	$V_{id} = \pm 1V, T_{amb}$	±200	±320		mA
I _{source}	Carpat Grioti Griotit Garierit	$T_{min.} < T_{amb} < T_{max.}$	±180]
ФМ14	Phase Margin at A _{VCL} = 14dB	$R_L = 25\Omega//15pF$		60		0
ФМ6	Phase Margin at A _{VCL} = 6dB	$R_L = 25\Omega//15pF$		40		0
NOISE A	AND DISTORTION					
en	Equivalent Input Noise Voltage	f = 100kHz		3		nV/√Hz
in	Equivalent Input Noise Current	f = 100kHz		1.2		pA/√Hz
THD	Total Harmonic Distortion	$V_{out} = 4$ Vpp, f = 100kHz $A_{VCL} = -10$ $R_L = 25\Omega//15$ pF		-69		dB
HD2 ₋₁₀	2nd Harmonic Distortion	$V_{out} = 4Vpp, f = 100kHz$ $A_{VCL} = -10$ $Load = 25\Omega // 15pF$		-70		dBc
HD2 ₊₂	2nd Harmonic Distortion	$V_{out} = 4Vpp, f = 100kHz$ $A_{VCL} = +2$ Load =25 Ω //15pF		-74		dBc

Symbol	Parameter Test Condition		Min.	Тур.	Max	Unit
HD3 ₊₂	3rd Harmonic Distortion	$V_{out} = 4Vpp, f = 1MHz$ $A_{VCL} = +2$ Load =25 Ω //15pF		-79		dBc
HD3 ₋₁₀	3rd Harmonic Distortion	$V_{out} = 4Vpp, f = 100kHz$ $A_{VCL} = -10$ Load =25 Ω //15pF		-80		dBc
IM2 ₋₁₀	2nd Order Intermodulation Product	F1 = 80kHz, F2 = 70kHz V_{out} = 8Vpp, A_{VCL} = -10 Load = 25 Ω //15pF		-77		dBc
IM3 ₋₁₀	3rd Order Intermodulation Product	F1 = 80kHz, F2 = 70kHz V_{out} = 8Vpp, A_{VCL} = -10 Load = 25 Ω //15pF		-77		dBc



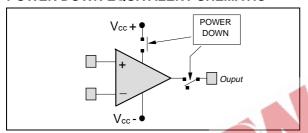
4/10

POWER DOWN MODE $V_{CC} = \pm 6 \text{Volts}, T_{amb} = 25 ^{\circ}\text{C}$

Symbol	Parameter		Min.	Тур.	Max	Unit
	Thershold Voltage for Power Down Mode					
V_{pdw}		Low Level		0	0.8	V
		High Level	2	3.3		
Icc _{pdw}	Power Down Mode Current Consumption				75	μA
R_{pdw}	Power Down Mode Ouput Impedance			1.4		MΩ
C_{pdw}	Power Down Mode Output Capacitance			33		pF

STANDBY CONTROL		OPERATOR STATUS		
pin (1) operator 1	pin (7) operator 2	operator 1	operator 2	
V _{high level}	V _{low level}	Standby	Active	
V _{high level}	V _{high level}	Standby	Standby	
V _{low level}	V _{low level}	Active	Active	
V _{low level}	V _{high level}	Active	Standby	

POWER DOWN EQUIVALENT SHEMATIC



OUPUT IMPEDANCE IN POWER DOWN MODE

In Power Down Mode the output of the driver is in "high impedance" state. It is really the case for the static mode. Regarding the dynamic mode, the impedance decreases due to a capacitive effect of the collector-substrat and base collector junction. The impedance behaviour comes capacitive, typically: $1.4 \text{M}\Omega$ // 33 pF.

INTERMODULATION DISTORTION

The curves shown below are the measurements results of a single operator wired as an adder with a gain of 15dB.

The operational amplifier is supplied by a symmetric $\pm 6V$ and is loaded with 25Ω .

Two synthesizers (Rhode & Schwartz SME) generate two frequencies (tones) (70 & 80kHz or 180 & 280kHz).

An HP3585 spectrum analyzer measures the spurious level at different frequencies.

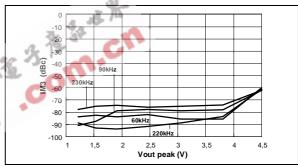
The curves are traced for different output levels (the value in the X ax is the value of each tone).

The output levels of the two tones are the same.

The generators and spectrum analyzer are phase locked to enhance measurement precision.

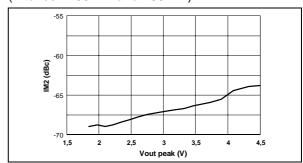
3rd ORDER INTERMODULATION

(2 tones: 70kHz and 80kHz)



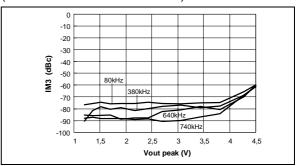
2nd ORDER INTERMODULATION

Spurious measurement @ 100kHz (2 tones : 180kHz and 280kHz)



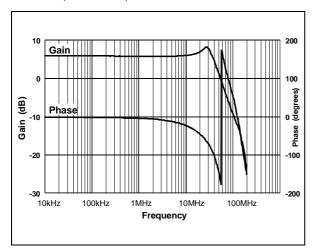
3rd ORDER INTERMODULATION

(2 tones: 180kHz and 280kHz)



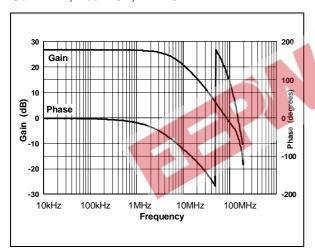
Closed Loop Gain and Phase vs. Frequency

Gain=+2, Vcc= \pm 6V, RL=25 Ω



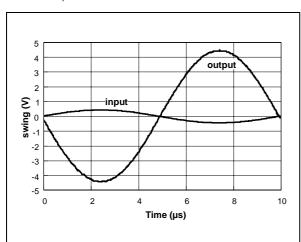
Closed Loop Gain and Phase vs. Frequency

Gain=+11, Vcc= \pm 6V, RL=25 Ω



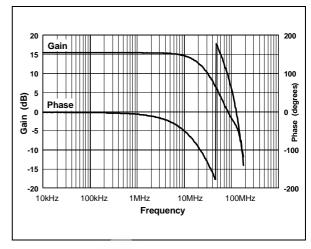
Maximum Output Swing

 $Vcc=\pm6V$, $RL=25\Omega$



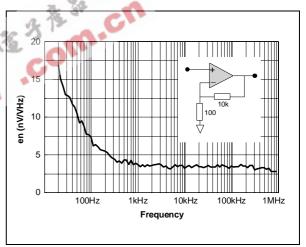
Closed Loop Gain and Phase vs. Frequency

Gain=+6, Vcc= \pm 6V, RL=25 Ω



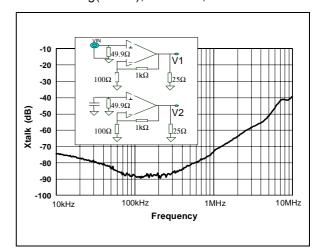
Equivalent Input Voltage Noise

Gain=+100, Vcc=±6V, no load



Channel Separation (Xtalk) vs. Frequency

XTalk=20Log(V2/V1), Vcc= \pm 6V, RL=25 Ω



6/10

ADSL CONCEPT

Asymmetric Digital Subscriber Line (ADSL), is a new modem technology, which converts the existing twisted-pair telephone lines into access paths for multimedia and high speed data communications.

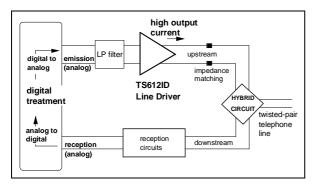
ADSL transmits more than 8 Mbps to a subscriber, and can reach 1Mbps from the subscriber to the central office. ADSL can literally transform the actual public information network by bringing movies, television, video catalogs, remote CD-ROMs, LANs, and the Internet into homes.

An ADSL modem is connected to a twisted-pair telephone line, creating three information channels: a high speed downstream channel (up to 1.1MHz) depending on the implementation of the ADSL architecture, a medium speed upstream channel (up to 130kHz) and a POTS (Plain Old Telephone Service), split off from the modem by filters.

THE LINE INTERFACE - ADSL Remote Terminal (RT):

The Figure 1 shows a typical analog line interface used for ADSL. The upstream and downstream signals are separated from the telephone line by using an hybrid circuit and a line transformer. On this note, the accent will be made on the emission path.

Figure 1 : Typical ADSL Line Interface

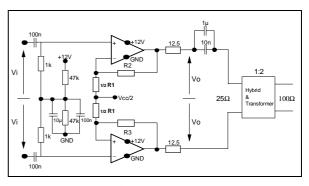


The TS612 is used as a dual line driver for the upstream signal.

For the remote terminal it is required to create an ADSL modem easy to plug in a PC. In such an application, the driver should be implemented with a +12 volts single power supply. This +12V supply is available on PCI connector of purchase.

The figure 2 shows a single +12V supply circuit that uses the TS612 as a remote terminal transmitter in differential mode.

Figure 2: TS612 as a differential line driver with a +12V single supply



The driver is biased with a mid supply (nominaly +6V), in order to maintain the DC component of the signal at +6V. This allows the maximum dynamic range between 0 and +12 V. Several options are possible to provide this bias supply (such as a virtual ground using an operational amplifier), such as a two-resistance divider which is the cheapest solution. A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the inverting input of the TS612. If we consider this bias current (5μ A) as the 1% of the current through the resistance divider (500μ A) to keep a stable mid supply, two $47k\Omega$ resistances can be used

The input provides two high pass filters with a break frequency of about 1.6kHz which is necessary to remove the DC component of the input signal. To avoid DC current flowing in the primary of the transformer, an output capacitor is used.

The $1\mu F$ capacitance provides a path for low frequencies, the 10nF capacitance provides a path for high end of the spectrum.

In differential mode the TS612 is able to deliver a typical amplitude signal of 18V peak to peak.

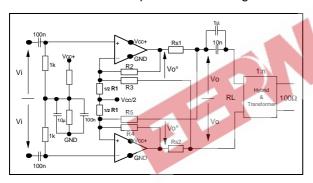
The dynamic line impedance is 100Ω . The typical value of the amplitude signal required on the line is up to 12.4V peak to peak. By using a 1:2 transformer ratio the reflected impedance back to the primary will be a quarter (25Ω) and therefore the amplitude of the signal required with this impedance will be the half $(6.2\ V\ peak\ to\ peak)$. Assuming the 25Ω series resistance $(12.5\Omega\ for\ both\ outputs)$ necessary for impedance matching, the output signal amplitude required is $12.4\ V\ peak\ to\ peak$. This value is acceptable for the TS612. In this case the load impedance is $25\Omega\ for\ each\ driver.$

For the ADSL upstream path, a lowpass filter is absolutely necessary to cutoff the higher frequencies from the DAC analog output. In this simple non-inverting amplification configuration, it will be easy to implement a Sallen-Key lowpass filter by using the TS612. For ADSL over POTS, a maximum frequency of 135kHz is reached. For ADSL over ISDN, the maximum frequency will be 276kHz.

INCREASING THE LINE LEVEL BY USING AN ACTIVE IMPEDANCE MATCHING

With passive matching, the output signal amplitude of the driver must be twice the amplitude on the load. To go beyond this limitation an active maching impedance can be used. With this technique it is possible to keep good impedance matching with an amplitude on the load higher than the half of the ouput driver amplitude. This concept is shown in figure 3 for a differential line.

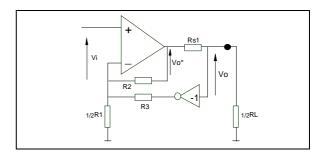
Figure 3: TS612 as a differential line driver with an active impedance matching



Component calculation:

Let us consider the equivalent circuit for a single ended configuration, figure 4.

Figure 4: Single ended equivalent circuit



Let us consider the unloaded system. Assuming the currents through R1, R2 and R3

as respectively:

$$\frac{2Vi}{R1}$$
, $\frac{(Vi-Vo^{\circ})}{R2}$ and $\frac{(Vi+Vo)}{R3}$

As Vo° equals Vo without load, the gain in this case becomes:

$$G = \frac{Vo(noload)}{Vi} = \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}$$

The gain, for the loaded system will be (1):

$$GL = \frac{Vo(withload)}{Vi} = \frac{1}{2} \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}, (1)$$

As shown in figure5, this system is an ideal generator with a synthesized impedance as the internal impedance of the system. From this, the output voltage becomes:

$$Vo = (ViG) - (RoIout),(2)$$

with Ro the synthesized impedance and lout the output current. On the other hand Vo can be expressed as:

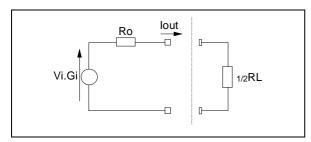
$$Vo = \frac{Vi\left(1 + \frac{2R2}{R1} + \frac{R2}{R3}\right)}{1 - \frac{R2}{R3}} - \frac{Rs \cdot 1Iout}{1 - \frac{R2}{R3}}, (3)$$

By identification of both equations (2) and (3), the synthesized impedance is, with Rs1=Rs2=Rs:

$$Ro = \frac{Rs}{1 - \frac{R2}{R3}}, (4)$$

8/10

Figure 5 : Equivalent schematic. Ro is the synthesized impedance



Unlike the level Vo° required for a passive impedance, Vo° will be smaller than 2Vo in our case. Let us write Vo°=kVo with k the matching factor varying between 1 and 2. Assuming that the current through R3 is negligeable, it comes the following resistance divider:

$$Ro = \frac{kVoRL}{RL + 2Rs1}$$

After choosing the k factor, Rs will equal to 1/2RL(k-1).

A good impedance matching assumes:

$$Ro=\frac{1}{2}RL,(5)$$

From (4) and (5) it becomes:

$$\frac{R2}{R3} = 1 - \frac{2Rs}{RL}, (6)$$

By fixing an arbitrary value for R2, (6) gives:

$$R3 = \frac{R2}{1 - \frac{2Rs}{RL}}$$

Finally, the values of R2 and R3 allow us to extract R1 from (1), and it comes:

$$R1 = \frac{2R2}{2\left(1 - \frac{R2}{R3}\right)GL - 1 - \frac{R2}{R3}}, (7)$$

with GL the required gain.

GL (gain for the loaded system)	GL is fixed for the application requirements GL=Vo/Vi=0.5(1+2R2/R1+R2/R3)/(1-R2/R3)
R1	2R2/[2(1-R2/R3)GL-1-R2/R3]
R2 (=R4)	Abritrary fixed
R3 (=R5)	R2/(1-Rs/0.5RL)
Rs	0.5RL(k-1)

CAPABILITIES

The table below shows the calculated components for different values of k. In this case $R2=1000\Omega$ and the gain=16dB. The last column displays the maximum amplitude level on the line regarding the TS612 maximum output capabilities (18Vpp diff.) and a 1:2 line transformer ratio.

P	Active n	natchin	g		
k	R1 (Ω)	R3 (Ω)	Rs (Ω)	TS612 Output Level to get 12.4Vpp on the line (Vpp diff)	Maximum Line level (Vpp diff)
1.3	820	1500	3.9	8	27.5
1.4	490	1600	5.1	8.7	25.7
1.5	360	2200	6.2	9.3	25.3
1.6	270	2400	7.5	9.9	23.7
1.7	240	3300	9.1	10.5	22.3
Passive matching				12.4	18

POWER CONSUMPTION IN COMMUNICATION

Conditions:

Passive impedance matching Transformer turns ratio: 2

Power Supply: 12V

Maximum level required on the line: 12.4Vpp Maximum output level of the driver: 12.4Vpp

Crest factor: 5.3 (Vp/Vrms)

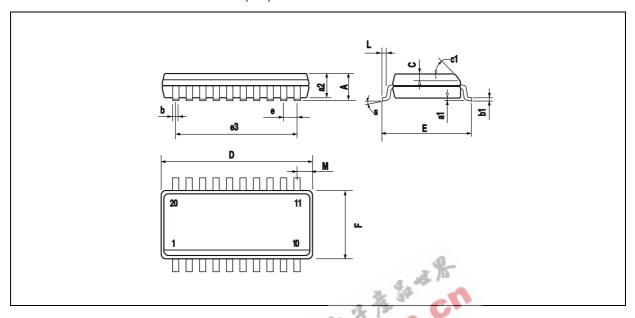
Power Supply: 12V

The TS612 power consumption during emission on 900 and 4550 meter twisted pair telephone

lines: 450mW

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC MICROPACKAGE (SO)



Dim.		Millimeters	132	·Ou.	Inches	
Dilli.	Min.	Тур.	Max.	Min.	Тур.	Max.
Α			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
С		0.5			0.020	
c1			45° (typ.)		•
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
е		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
М			0.75			0.030
S			8° (n	nax.)	•	•

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - All Rights Reserved STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom http://www.st.com

