TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TS61 Series

Voltage Detector

SOT-23

Pin Definition:

1. Output
2. Ground
3. Input

General Description

The TS61 series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. Detect voltage is extremely accurate with minimal temperature drift.
Both CMOS and N-channel open drain output configurations are available.

Features

- Highly Accurate: ±2%
- Detecting Voltage Temperature Characteristics:
  TYP ± 100ppm /°C
- Low Power Consumption, 0.7uA (typ) @V_{IN}=1.5V
- Detect Voltage Range: 1.6V ~ 6.0V
- Operating Voltage Range: 0.7V ~ 10V
- Output Configuration:
  N-Channel open drain or CMOS

Applications

- Battery-operated systems
- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

Ordering Information

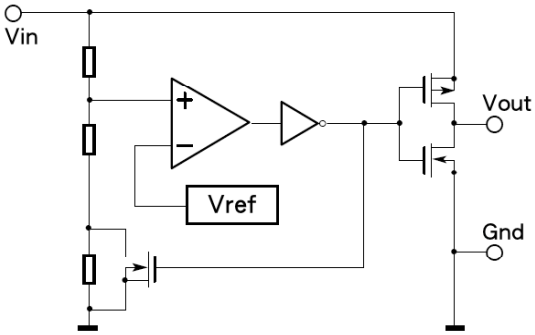
Part No.	Package	Packing
TS61C**xx**CX RF	SOT-23	3Kpcs / 7” Reel
TS61N**xx**CX RF	SOT-23	3Kpcs / 7” Reel

Note:

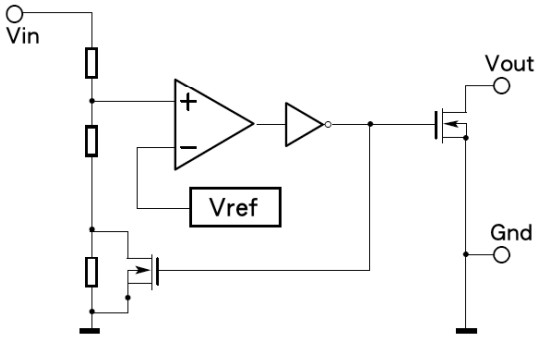
* Where **xx** denotes voltage option, available are
  20= 2.0V
  23= 2.3V
  24= 2.4V
  25= 2.5V
  27= 2.7V
  30= 3.0V
  33= 3.3V
  40= 4.0V
  42= 4.2V
  44= 4.4V
  45= 4.5V
  Contact factory for additional voltage option.
* TS61**C**: CMOS output
* TS61**N**: N-Channel Open Drain Output

Block Diagram

CMOS Output



N-Channel Open Drain Output



TS61 Series
Voltage Detector

Absolute Maximum Rating

Parameter		Symbol	Maximum	Unit
Input Voltage		V_{IN}	+12	V
Output Current		Io	50	mA
Output Voltage	CMOS	V_{OUT}	(Gnd – 0.3) to (V_{IN} + 0.3)	V
	N-channel open drain		(Gnd – 0.3) to 12	
Power Dissipation	SOT-23	P_D	150	mW
Operating Ambient Temperature Range		T_A	-40 ~ +85	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Stress above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation section of the specifications is not implied.

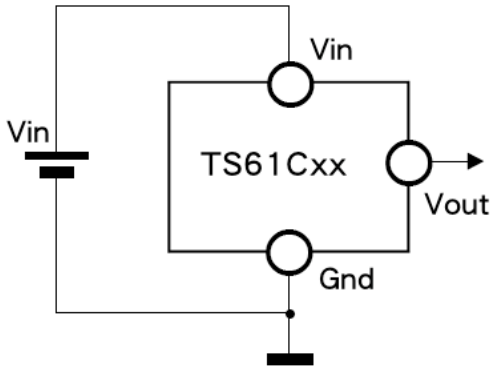
Electrical Specifications (Ta = 25 °C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Circuit
Detect Voltage		V_{DF}	V_{DF}x 0.98	V_{DF}	V_{DF}x 1.02	V	1
Hysteresis range		V_{HYS} / V_{DF}	2	--	8	%	1
Supply Current	V_{IN}=1.5V	Iss	--	0.7	2.3	μA	2
	V_{IN}=2.0V		--	0.8	2.7		
	V_{IN}=3.0V		--	0.9	3.0		
	V_{IN}=4.0V		--	1.0	3.2		
	V_{IN}=5.0V		--	1.1	3.6		
Operating Voltage	V_{DF}(T)=1.6V~6V	V_{IN}	0.7	--	10.0	V	1
Output Current	**N-channel V_{DS}=5V**						
	V_{IN}=1.0V	I_{OUT}	1.0	2.2	--	mA	3
	V_{IN}=2.0V		3.0	7.7	--		
	V_{IN}=3.0V		5.0	10.1	--		
	V_{IN}=4.0V		6.0	11.5	--		
	V_{IN}=5.0V		7.0	13.0	--		
	P-channel V_{DS}=2.1V (with CMOS output)						
	V_{IN}=8.0V	I_{OUT}	--	-10.0	-2.0	mA	4
Temperature Characteristics	-40°C ≤ T_A ≤ 85°C	$\frac{\Delta V_{DF}}{\Delta T_A \times V_{DF}}$	--	±100	--	ppm / °C	--
Delay Time	Vdr→ V_{OUT} inversion	t_{DLY}	--	--	0.2	ms	5

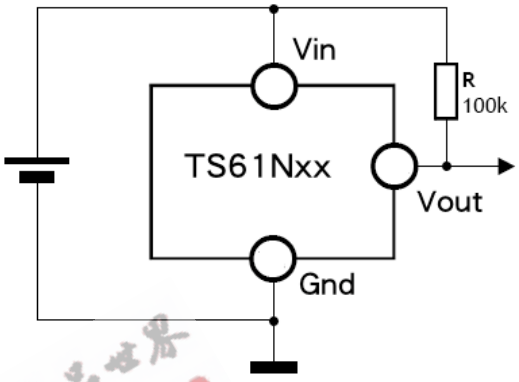
Note: V_{DF}(T): Established Detect Voltage Value, 1.6V ~ 6.0V ±2% for Standard Voltage Detectors
Release Voltage: V_{DR} = V_{DF} + V_{HYS}

Typical Application Circuit

CMOS Output

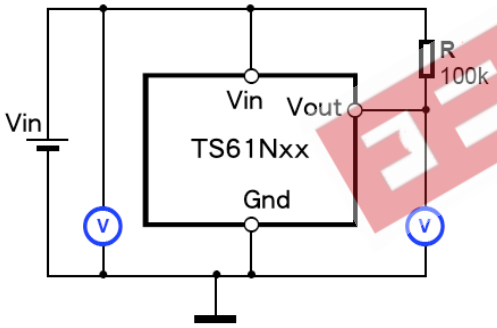


N-Channel Open Drain Output



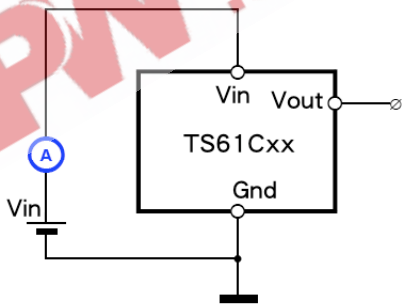
Measuring Circuit

Test Circuit 1

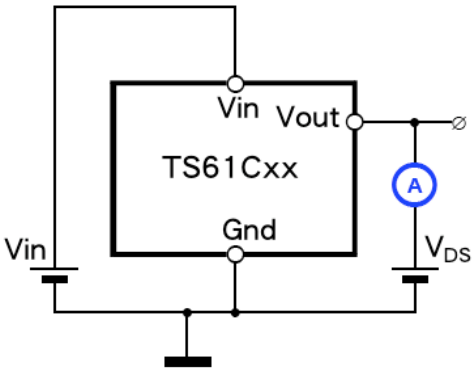


* Not Necessary with CMOS output product

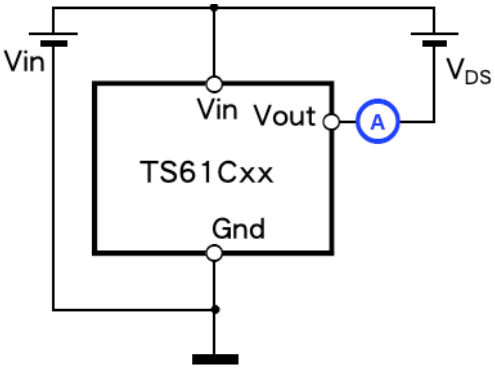
Test Circuit 2



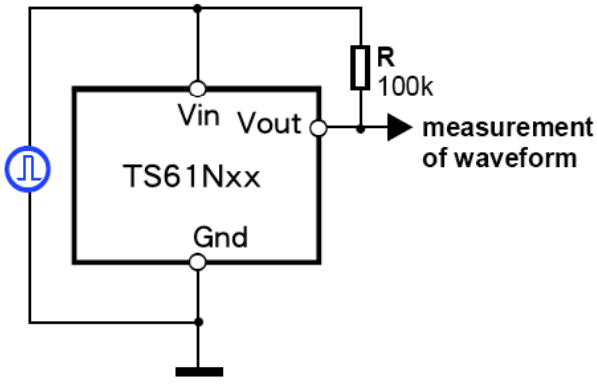
Test Circuit 3



Test Circuit 4



Test Circuit 5



* Not Necessary with CMOS output products

Directions for use

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the V_{IN} pin and the input CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. (refer to the Oscillation Description ① below).
3. When a resisted is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to the Oscillation Description ② below)
4. In order to stabilize the IC's operations, please ensure that V_{IN} pin's input frequency's rise and fall times are more than several μs/V.
5. Please use N-ch open drains configuration, when a resistor R_{IN} is connected between the V_{IN} pin and power source. In such cases, please ensure that R_{IN} is less than kΩ and that C is more than 0.1μF.

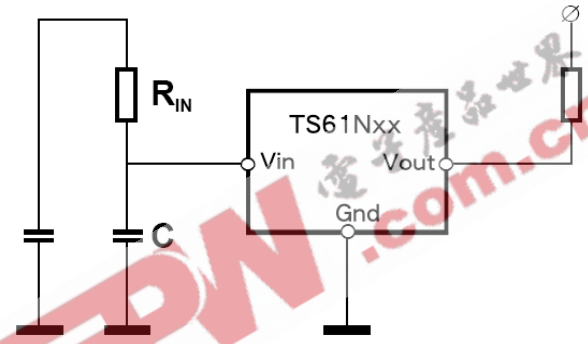


Diagram: Circuit using an input resistor

Oscillation Description

OUTPUT CURRENT OSCILLATION WITH THE CMOS OUTPUT CONFIGURATION

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow at R_L. Because a voltage drop (R_{IN} x I_{OUT}) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detec voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again. Oscillation may occur with this "release-detect-release" repetition. Further, this condition will also appear via means of a similar mechanism during detect operations.

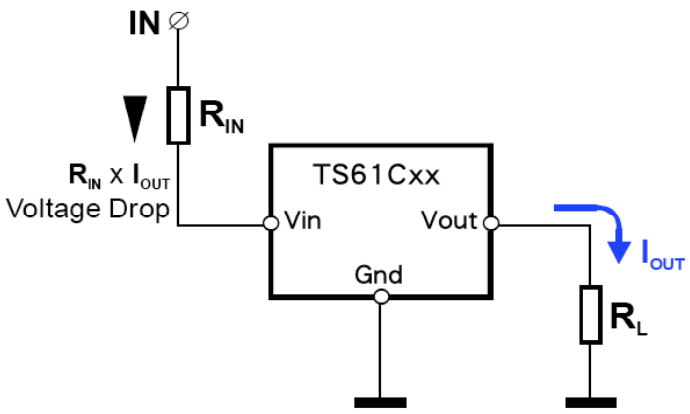


Diagram 1: Oscillation in relation to output current

Oscillation Description (Continue)

OUTPUT CURRENT OSCILLATION WITH THE CMOS OUTPUT CONFIGURATION

Since the TS61 series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations (refer to diagram 2). Since hysteresis exists during detect operation, oscillation is unlikely to occur.

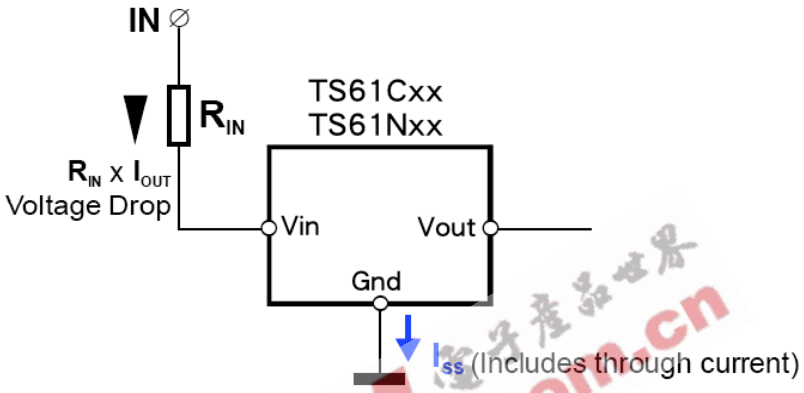
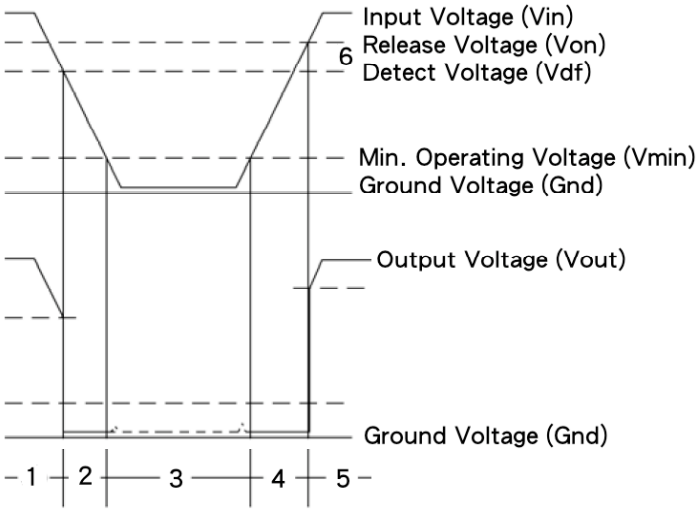


Diagram 2: Oscillation in relation to through current

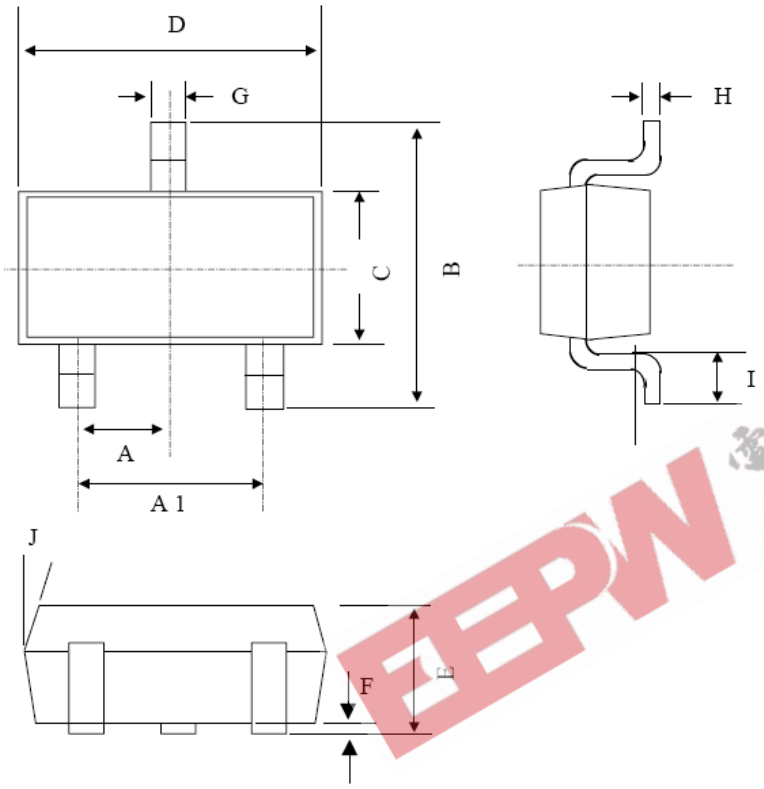
Function Description

1. When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN}. (A condition of high impedance exists with N-ch open drain output configurations).
2. When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage will be equal to the ground voltage (V_{SS}).
3. When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pull-up).
4. When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage V_{DR} level, the ground voltage (V_{SS}) level will be maintained.
5. When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN}. (A condition of high impedance exists with N-ch open drain output configurations.)
6. The difference between V_{DR} and V_{DF} represents the hysteresis range.

Timing Chart



SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	0.95 BSC		0.037 BSC	
A1	1.9 BSC		0.074 BSC	
B	2.60	3.00	0.102	0.118
C	1.40	1.70	0.055	0.067
D	2.80	3.10	0.110	0.122
E	1.00	1.30	0.039	0.051
F	0.00	0.10	0.000	0.004
G	0.35	0.50	0.014	0.020
H	0.10	0.20	0.004	0.008
I	0.30	0.60	0.012	0.024
J	5°	10°	5°	10°

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