INTEGRATED CIRCUITS
UNITRODE

UC1849
UC2849
UC3849

Secondary Side Average Current Mode Controller

FEATURES

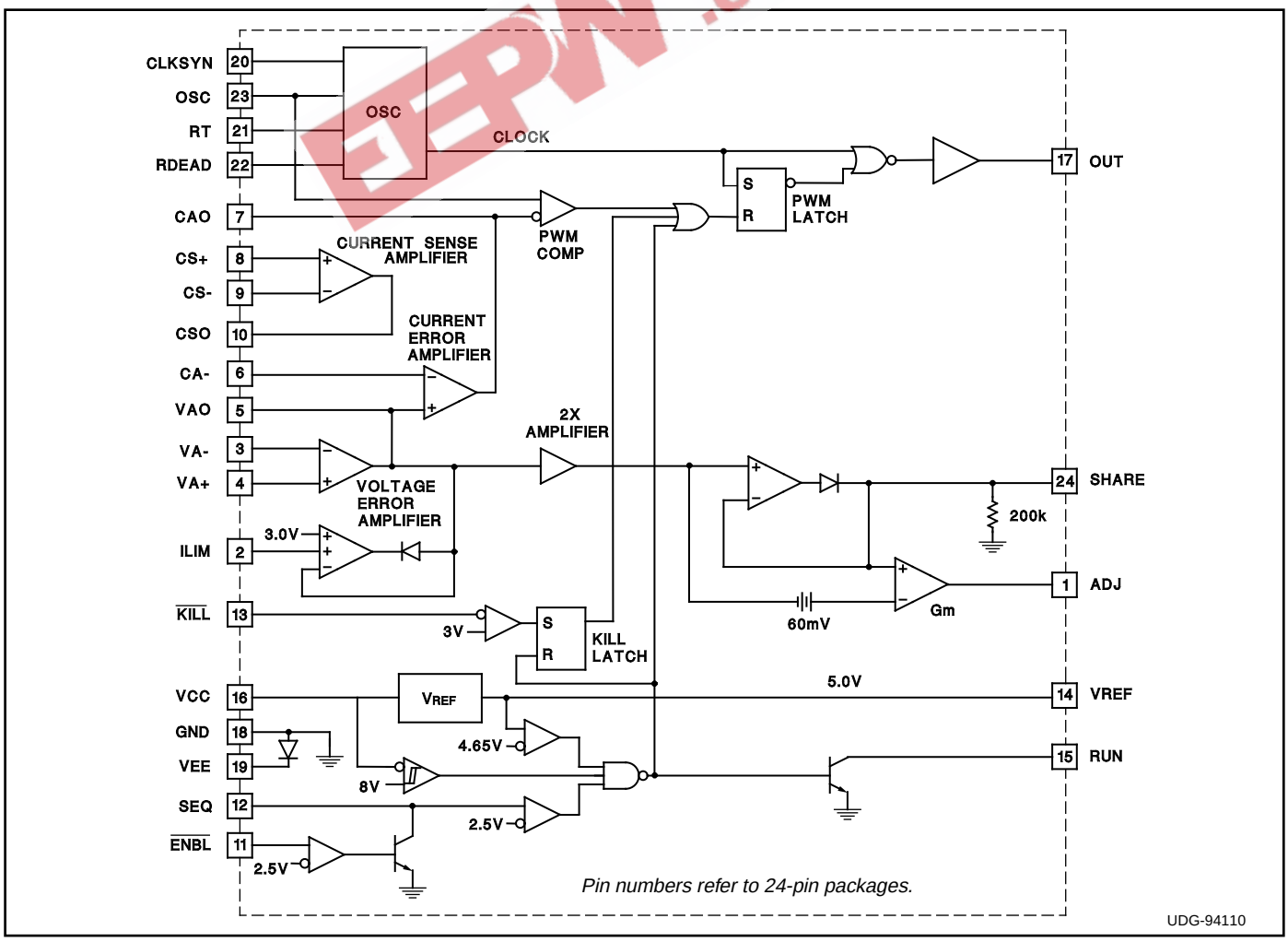
- Practical Secondary Side Control of Isolated Power Supplies
- 1MHz Operation
- Differential AC Switching Current Sensing
- Accurate Programmable Maximum Duty Cycle
- Multiple Chips Can be Synchronized to Fastest Oscillator
- Wide Gain Bandwidth Product (70MHz, Acl>10) Current Error and Current Sense Amplifiers
- Up to Ten Devices Can Easily Share a Common Load

DESCRIPTION

The UC1849 family of average current mode controllers accurately accomplishes secondary side average current mode control. The secondary side output voltage is regulated by sensing the output voltage and differentially sensing the AC switching current. The sensed output voltage drives a voltage error amplifier. The AC switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current sense amplifier. The outputs of the voltage error amplifier and current sense amplifier differentially drive a high bandwidth, integrating current error amplifier. The sawtooth waveform at the current error amplifier output is the amplified and inverted inductor current sensed through the resistor. This inductor current downslope compared to the PWM ramp achieves slope compensation, which gives an accurate and inherent fast transient response to changes in load.

The UC1849 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC1849 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. The UC1849 is an ideal controller to achieve high power, secondary side average current mode control.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 20V
Output Current Source or Sink 0.3A
Analog Input Voltages . . . . . .–0.3V to 7V
ILIM, $\overline{KILL}$, SEQ, $\overline{ENBL}$, RUN . . . . . .–0.3V to 7 V
CLKSYN Current Source 12mA
RUN Current Sink 15mA
SEQ Current Sink 20mA
RDEAD Current Sink 20mA
Share Bus Voltage (voltage with respect to GND) . . .0V to 6.2V
ADJ Voltage (voltage with respect to GND) . . . . . .0.9V to 6.3V
VEE (voltage with respect to GND) . . . . . .–1.5V
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

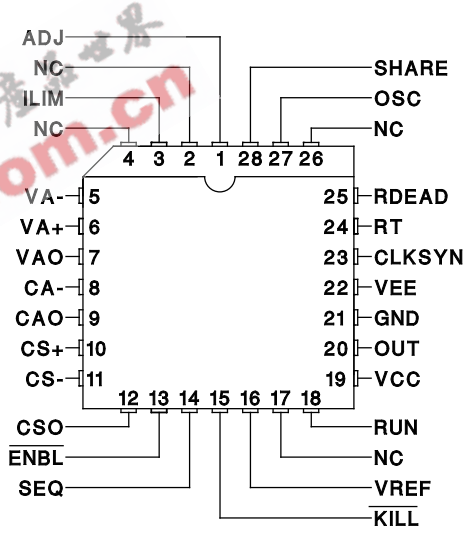
RECOMMENDED OPERATING CONDITIONS

Input Voltage 8V to20V
Sink/Source Output Current 250mA
Timing Resistor (RT) . . . . . .1k to 200k
Timing Capacitor (CT) . . . . . .75pF to 2nF

CONNECTION DIAGRAMS

DIL-24, SOIC-24, TSSOP-24 (Top View)
J or N, DW, PW Packages

PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Ib			0.5	3	µA
Vio	T_A = +25°C			3	mV
	Over Temperature			5	mV
Avo		60	90		dB
GBW (Note 2)	Acl = 1, R_{IN} = 1k, CC = 15pF, f = 200kHz (Note 1)	4.5	7		MHz
Vol	Io = 1mA, Voltage above VEE		0.5		V
Voh	Io = 0mA		3.8		V
	Io = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Current Error Amplifier					
Ib			0.5	3	µA
Vio			3	20	mV

ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Error Amplifier (cont.)					
Avo		60	90		dB
GBW (Note 2)	Acl = 1, R_{IN} = 1k, CC=15pF, f=200kHz (Note 1)	4.5	7		MHz
Vol	I_O = 1mA, Voltage above VEE		0.5		V
Voh	I_O = 0mA		3.8		V
	I_O = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Voltage Error Amplifier					
Ib			0.5	3	µA
Vio			2	5	mV
Avo		60	90		dB
GBW (Note 2)	f = 200kHz	4.5	7		MHz
Vol	I_O = 175µA, Volts above VEE		0.3	0.6	V
Voh	ILIM > 3V	2.85	3	3.15	V
Voh - ILIM	Tested ILIM = 0.5V, 1.0V, 2.0V	–100		100	mV
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
2X Amplifier and Share Amplifier					
V offset (b; y = mx + b)				20	mV
GAIN (m; y = mx + b)	Slope with ΔV_{OUT} = 1V and 2V	1.98		2.02	V
GBW (Note 2)			100		kHZ
R_{SHARE}	VCC = 0, V_{SHARE}/I_{SHARE}		200		k
Total Offset	Negative supply is VEE, GND Open, VAO = GND	–75	0	75	mV
Vol	VAO = Voltage Amplifier Vol, Volts above VEE	0.2	0.45	0.6	V
Voh	I_O = 0mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
	I_O = –1mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
Adjust Amplifier					
Vio		40	60	80	mV
gm	I_{OUT}= –10µA to 10µA, V_{OUT} = 3.5V, C_{ADJ} = 1µF		–1		mS
Vol	I_{OUT} = 0	0.9	1	1.1	V
	I_{OUT} = 50µA	0.85	1	1.15	V
Voh	I_{OUT} = 0, V_{SHARE} = 6.5V	5.7	6	6.3	V
	I_{OUT} = –50µA, V_{SHARE} = 6.5V	5.7	6	6.3	V
Oscillator					
Frequency		450	500	550	kHz
Max Duty Cycle		80	85	90	%
OSC Ramp Amplitude		2	2.5	2.8	V
Clock Driver/SYNC (CLKSYN)					
Vol			0.02	0.2	V
Voh			3.6		V
	R_{CLKSYN} = 200Ω		3.2		V
I_{SOURCE}			25		mA
R_{CLKSYN}	VCC = 0, V_{CLKSYN}/I_{CLKSYN}		10		k
V_{TH}			1.5		V

ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
VREF Comparator					
Turn-on threshold			4.65		V
Hysteresis			0.4		V
VCC Comparator					
Turn-on Threshold		7.9	8.3	8.7	V
Hysteresis			0.4		V
KILL Comparator					
Voltage Threshold			3		V
Sequence Comparator					
Voltage Threshold			2.5		V
SEQ SAT	I_O = 10mA		0.25		V
Enable Comparator					
Voltage Threshold			2.5		V
RUN SAT	I_O = 10mA		0.25		V
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
VREF	VCC = 15V	4.9		5.1	V
Line Regulation	10 < VCC < 20		3	15	mV
Load Regulation	0 < I_O < 10mA		3	15	mV
Short Circuit I	VREF = 0V	30	60	90	mA
Output Stage					
Rise Time	C_L = 100pF		10	20	ns
Fall Time	C_L = 100pF		10	20	ns
Voh	VCC > 11V, I_O = –10mA	8.0	8.4	8.8	V
	I_O = –200mA	7.8			V
Vol	I_O = 200mA			3.0	V
	I_O = 10mA			0.5	V
Virtual Ground					
V_{GND}-VEE	VEE is externally supplied, GND is floating and used as Signal GND.	0.2	0.75		V
Icc					
Icc (run)			21	30	mA

Note 1: If a closed loop gain greater than 1 is used, the possible GBW will increase by a factor of ACL + 10; where ACL is the closed loop gain.

Note 2: Guaranteed by design. Not 100% tested in production.

Note 3: Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

PIN DESCRIPTIONS

ADJ: The output of the transconductance (gm = –1mS) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6V) its control voltage (VA+) until its load current is equal to the master. The 60mV input offset on the gm amplifier guarantees that the unit sensing the highest load current is chosen as the master. The 60mV offset guarantees by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30mV. This pin needs a 1µF capacitor to compensate the amplifier.

CA-: The inverting input to the current error amplifier. This amplifier needs a capacitor between CA- and CAO to set its dominant pole.

PIN DESCRIPTIONS (cont.)

CAO: The output of the current error amplifier which is internally clamped to 4V. It is internally connected to the inverting input of the PWM comparator.

CS-, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier is not internally compensated so the user must compensate externally to attain the highest GBW for the application.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The CLKSYN voltage is 3.6V when the oscillator capacitor (CT) is being discharged, otherwise it is 0V. If the recommended synchronization circuit is not used, a 1k or lower value resistor from CLKSYN to GND may be needed to increase fall time on CLKSYN pin.

CSO: The output of the current sense amplifier which is internally clamped to 4V.

ENBL: The active low input with a 2.5V threshold enables the output to switch. SEQ and RUN are driven low when ENBL is above its 2.5V threshold.

GND: The signal ground used for the voltage sense amplifier, current sense amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

KILL: The active low input with a 3.0V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving KILL above 3.0V and either resetting the power to the chip (VCC) or resetting the ENBL signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0V. A voltage less than 3.0V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp pin which has a capacitor (CT) to ground and a resistor (RDEAD) to the RDEAD pin programs its maximum duty cycle by programming a minimum dead time. The ramp oscillates between 1.2V to 3.4V when an RDEAD resistor is used. The maximum duty cycle can be increased by connecting RDEAD to OSC which changes the oscillator ramp to vary between 0.2V and 3.5V. In order to guarantee zero duty cycle in this configuration VEE should not be connected to GND.

The charge time is approximately $T_{CHARGE} = R_T \cdot C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \cdot RDEAD \cdot C_T$.

(1) $$\text{Frequency} \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}}$$

(2) $$\text{Maximum Duty Cycle} \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}}$$

The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5V. The peak current sink and source are 250mA. All UVLO, SEQ, ENBL, and KILL logic either enable or disable the output driver.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is $2 \cdot RDEAD \cdot C_T$. The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

RT: This pin programs the charge time of the oscillator ramp. The charge current is

$$\frac{VREF}{2 \cdot R_T}$$

The charge time is approximately $T_{CHARGE} \approx R_T \cdot C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} \approx 2 \cdot RDEAD \cdot C_T$.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4V, VREF is greater than 4.65V, SEQ is greater than 2.5V, and KILL lower than 3.0V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND creates a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly DC voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA+, VA-: The inverting and non-inverting inputs to the voltage error amplifier.

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

PIN DESCRIPTIONS (cont.)

VCC: The input voltage of the chip. The chip is operational between 8.4V and 20V.

VEE: The negative supply to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0V.

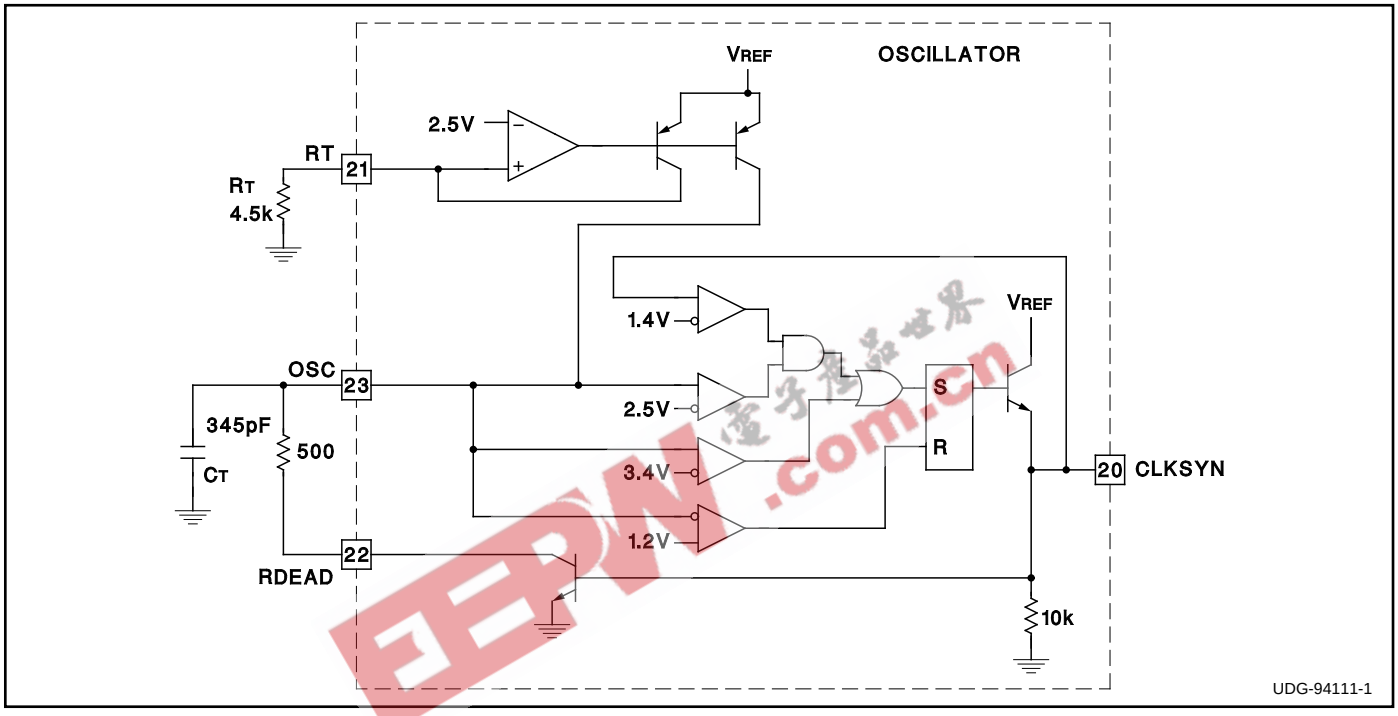


Figure 1. Oscillator Block with External Connections

CIRCUIT BLOCK DESCRIPTION:

PWM Oscillator: The oscillator block diagram with external connections is shown in Figure 1. A resistor (R_T) connected to pin RT sets the linear charge current;

$$I_{RT} \approx \frac{2.5V}{R_T}$$

The timing capacitor (C_T) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4V threshold. After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. This discharge time with the RC time delay of $2 \cdot C_T \cdot$ RDEAD is the minimum output low time. OSC continues to discharge until it reaches a 1.2V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Figure 2. Equations to approximate frequency and maximum duty cycle are listed under the OSC pin description. Figure 3 and 4 graphs show measured variation of frequency and maximum duty cycle with varying RT, CT, and RDEAD component values.

As shown in Figure 5, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the

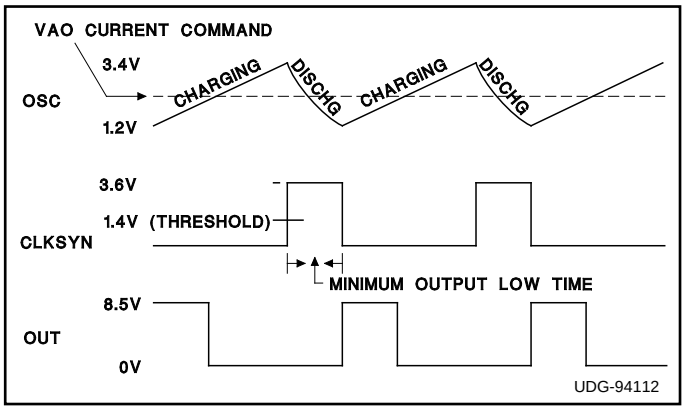


Figure 2. Oscillator and PWM Output Waveform

CIRCUIT BLOCK DESCRIPTION (cont.)

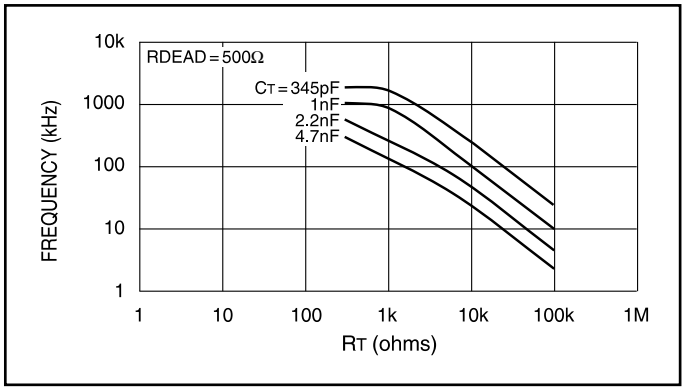


Figure 3. Output Frequency

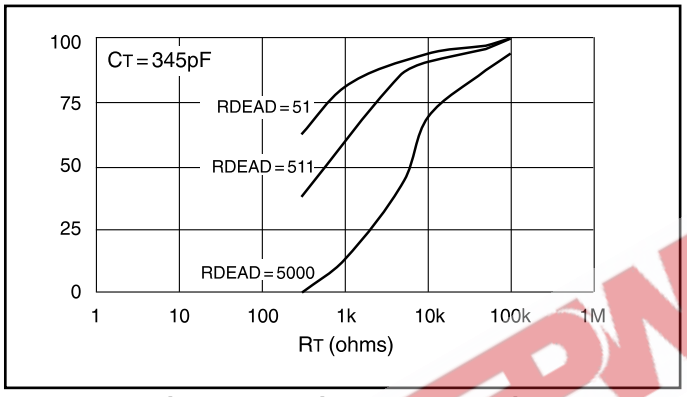


Figure 4. Maximum Duty Cycle

current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to guarantee synchronization.

Grounds, Voltage Sensing and Current Sensing: The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 6, the positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA-), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, RS.

Figure 6 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. The voltage offset on the current sense amplifier is not needed if VEE is separated from GND. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7V below ground. The resistor RADJ is used for load sharing. The unit which is the master will force VADJ to 1.0V. Therefore, the regulated voltage being sensed is actually

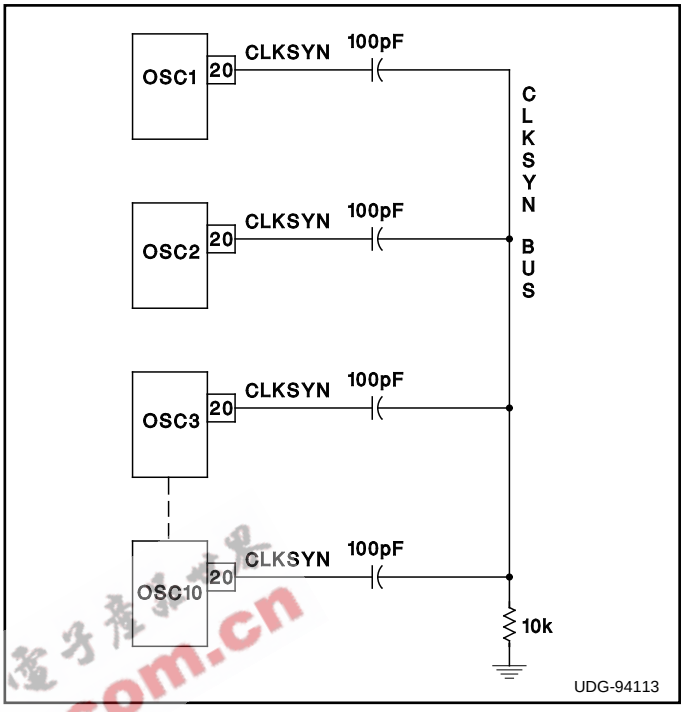


Figure 5. Oscillator Synchronization Connection Diagram

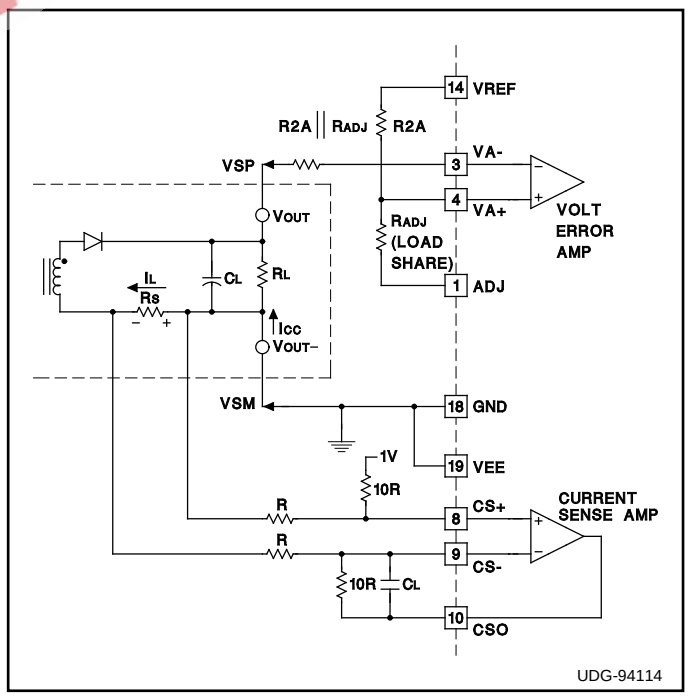


Figure 6. Voltage and Current Sense VEE Tied to GND

$$VSP - VSM = (VREF - V_{ADJ}) \cdot \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + V_{ADJ}$$

VSM = 0V, V_{ADJ} = 1V (master), VREF = 5V

$$VSP = 4 \cdot \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + 1V$$

CIRCUIT BLOCK DESCRIPTION (cont.)

The ADJ pin voltage on the slave chips will increase forcing their load currents to increase to match the master.

The AC frequency response of the voltage error amplifier is shown in Figure 7.

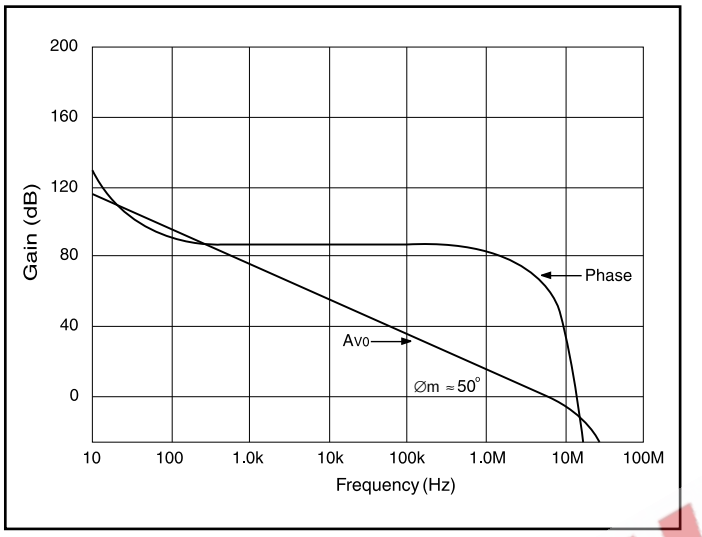


Figure 7. AC Frequency Response of the Voltage Error Amplifier

Startup and Shutdown: Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC1849 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it will command zero load current, guaranteeing a soft start. The undervoltage lockout (UVLO) is a logical AND of ENBL < 2.5V, SEQ > 2.5V, VCC > 8.4V and VREF > 4.65V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the ENBL pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4V. The KILL input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after KILL has been initiated, the chip must be powered down and then back up. A pulse on the ENBL pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing: Load sharing is accomplished similar to the UC1907. The sensed current for the UC1849 has an AC component that is amplified and then averaged. The voltage error amplifier output is the current command signal representing the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The IC with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60mV input offset guarantees that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) ICs to adjust their respective references high in order to balance each IC's load current. The master's ADJ pin will be at its 1.0V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0V.

VREF can be adjusted 150mV to 300mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} will typically be 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1V ±100mV by a factor of 10 to 30, contributing only a 3mV to 10mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop: The current sense amplifier (CSA) is designed specifically for the task of sensing and amplifying the inductor ripple current at frequencies up to 1MHz. The CSA's input offset voltage (VIO) is trimmed to less than 1mV to minimize error of the average current signal. This amplifier is not internally compensated allowing the user to optimally choose the zero crossing bandwidth.

$$(3) \quad \text{Frequency (0dB)} = \frac{1}{2\pi R_{INV} \cdot C_{COMP}}$$

R_{INV} is the input resistance at the inverting terminal CS- C_{COMP} is the capacitance between CS- and CSO.

Although it is only unity gain stable for a GBW of 7MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate at 70MHz with sufficient phase margin. A closed loop gain of 10 attenuates the output by 20.8dB.

$$20.8 = 20\log \cdot \frac{1}{11}$$

to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity

CIRCUIT BLOCK DESCRIPTION (cont.)

at 7MHz, where the phase margin begins to roll off. See Figure 8 for typical Bode plot.

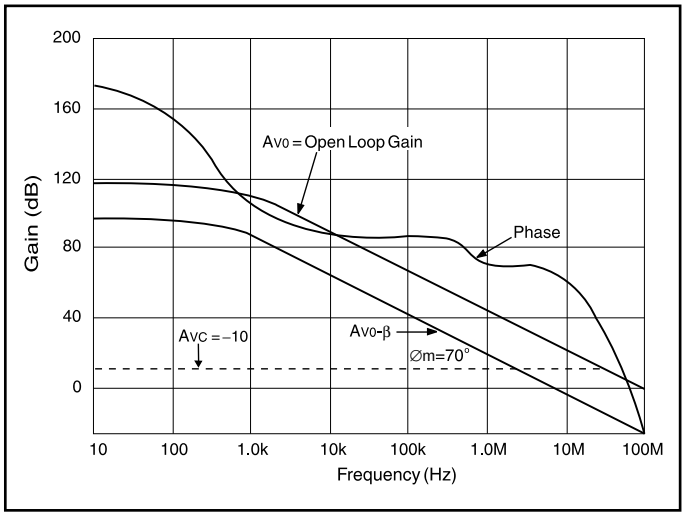


Figure 8. Current Sense Amplifier and Current Error Amplifier Bode Plot

The gain of the differential current sense amplifier (CS_{GAIN}) is calculated by knowing the maximum load current. The maximum voltage across the shunt resistor (R_S) divided by R_S is the maximum load current. By amplifying the voltage across RS, V_{RS}, to be equal to the voltage error amplifier Voh, the current control loop keeps the load from exceeding its current limit. Voh is set at 3.0V if ILIM is connected to VREF. The maximum current limit clamp can be reduced by reducing the voltage at ILIM to less than 3.0V as described in the ILIM pin description.

$$(4) \quad R_S = \frac{V_{RS}}{\text{Max } I_{LOAD}}$$

$$(5) \quad CS_{GAIN} = \frac{V_{ILIM}}{V_{RS}}$$

The current error amplifier (CEA) also needs its loop compensated by the user with the same criteria as the current sense amplifier. This amplifier is essentially the same wide bandwidth amplifier without the input offset voltage trim. The zero crossing can also be approximately calculated with Equation 3. The gain bandwidth of the current loop is optimized by matching the inductor downslope (Vo/L) to the oscillator ramp slope (Vs ▪ fs). Subharmonic oscillation problems are avoided by keeping the amplified inductor downslope less than the oscillator ramp slope.

The following equation determines the current error amplifier gain (GCA):

$$(6) \quad GCA = \frac{Vs \cdot fs}{(Vo/L) \cdot R_S \cdot CS_{GAIN}};$$

where CS_{GAIN} and R_S are defined by equations 4 and 5,
Vs is the oscillator peak to peak voltage,
fs is the oscillator frequency,
Vo is the output voltage,
and L is the inductance.

Additional Information about average current mode control can be found in Unitrode Application Note U-140.

Design Example: Figure 9 is an open loop test that lets the user test the circuit blocks discussed without having to build an entire control loop. The pulse width can be varied by either the V_{ADJ} or the V_{ISENSE} inputs. Figure 10 shows an isolated power supply using the UC1849 secondary side average current mode controller.

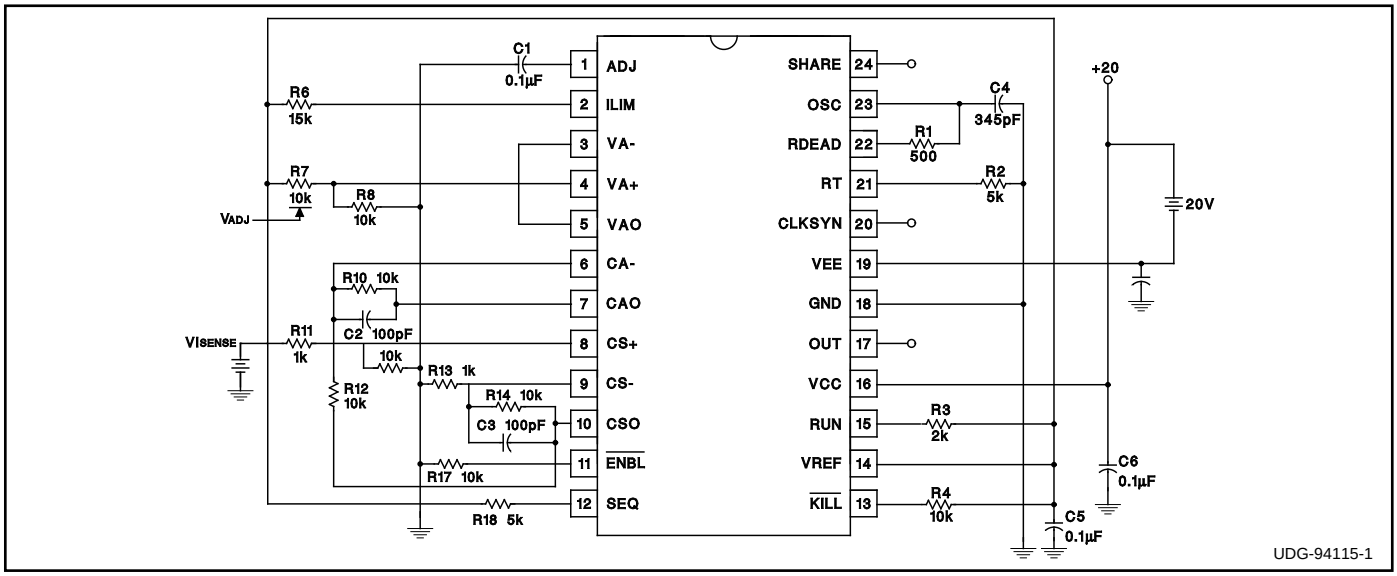


Figure 9. Open Loop Circuit

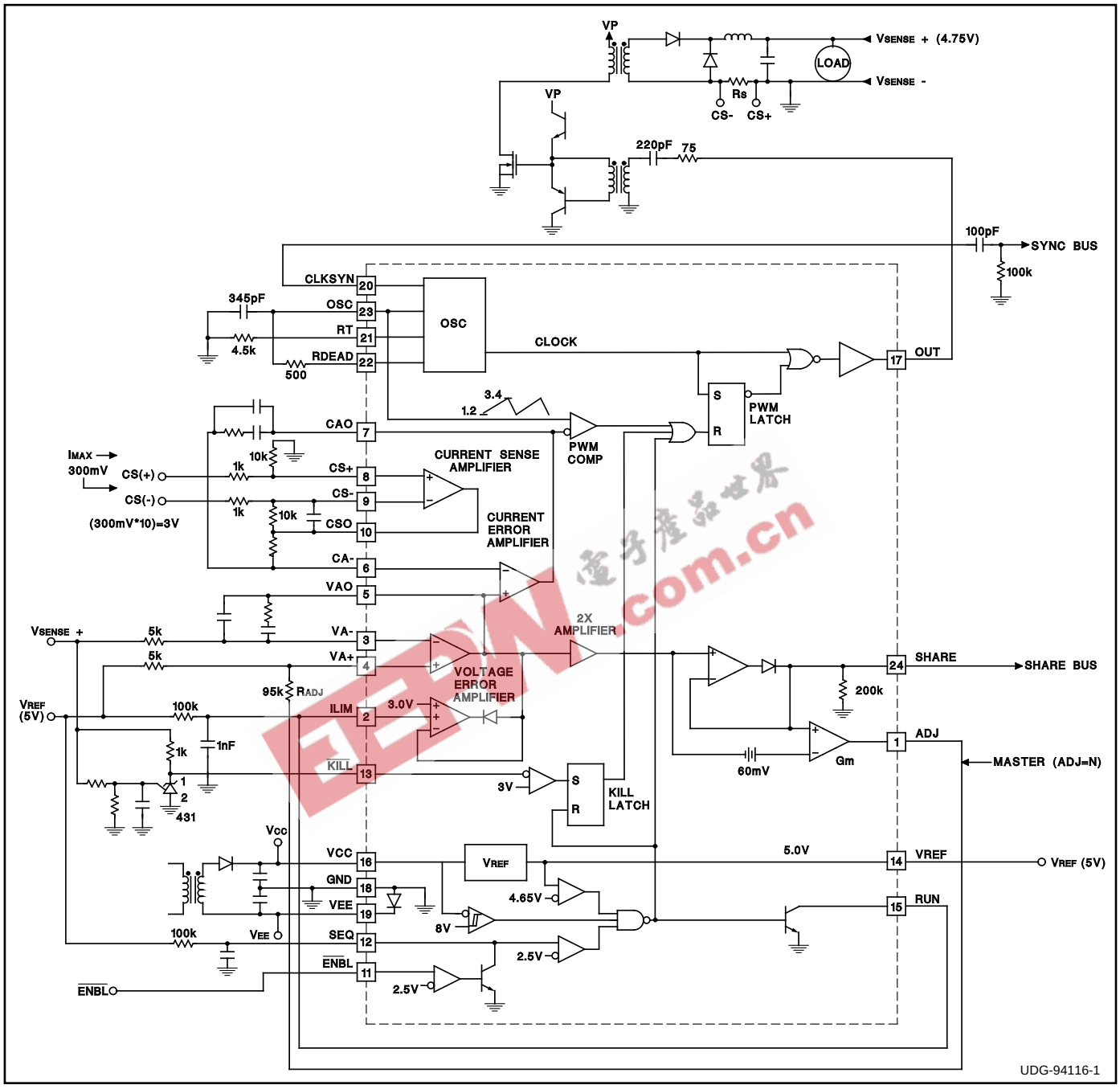


Figure 10. UC1849 Application Diagram

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.