

HIGH-SPEED PWM CONTROLLER

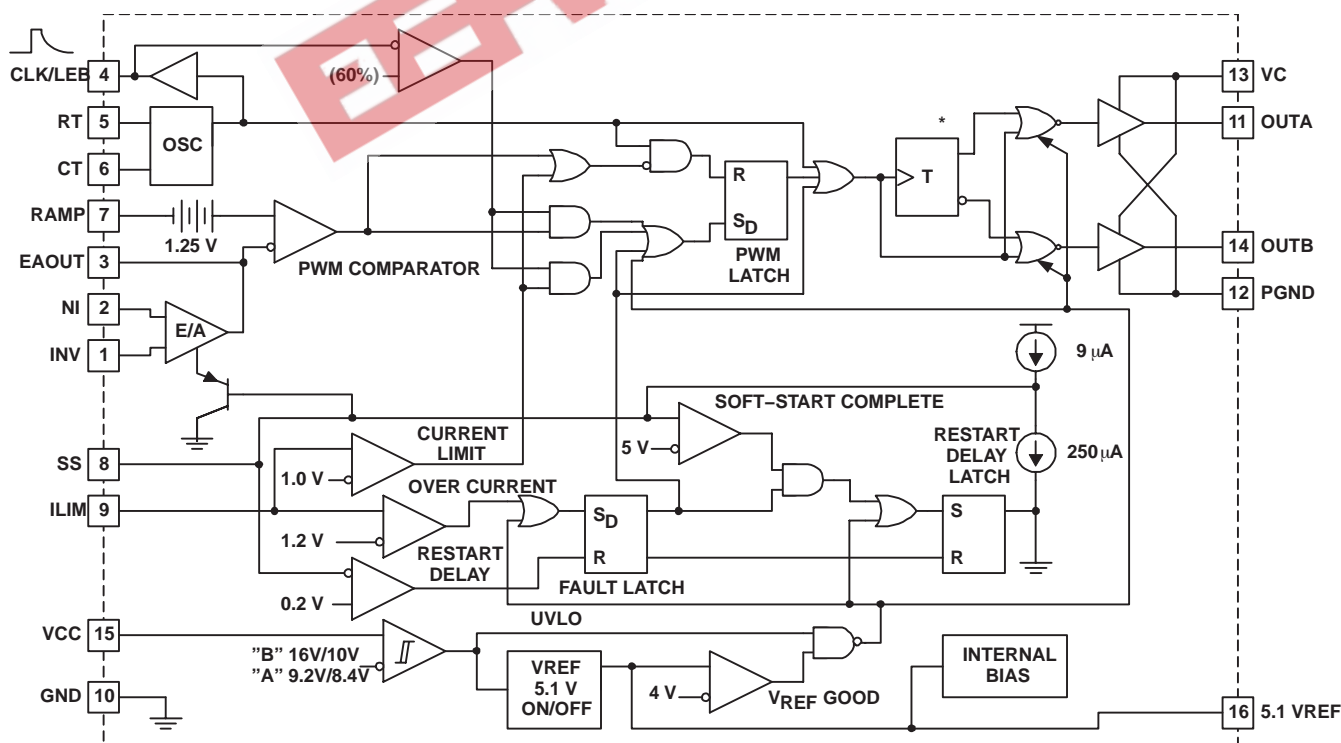
FEATURES

- Improved Versions of the UC3823/UC3825 PWMs
- Compatible with Voltage-Mode or Current-Mode Control Methods
- Practical Operation at Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High-Current Dual Totem Pole Outputs (2-A Peak)
- Trimmed Oscillator Discharge Current
- Low 100- μ A Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

DESCRIPTION

The UC3823A and UC3823B and the UC3825A and UC3825B family of PWM controllers are improved versions of the standard UC3823 and UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 μ A, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

BLOCK DIAGRAM



* On the UC1823A version, toggles Q and \bar{Q} are always low.

UDG-02091



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UC1823A, UC2823A, UC2823B, UC3823A, UC3823B, UC1825A, UC2825A, UC2825B, UC3825A, UC3825B

SLUS334C – AUGUST 1995 – REVISED AUGUST 2004



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A and UC3825B have dual alternating outputs and the same pin configuration of the UC3825. The UC3823A and UC3823B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A and UC3823B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823 and UC3825. The "B" versions have UVLO thresholds of 16 V and 10 V, intended for ease of use in off-line applications.

Consult the application note, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, (SLUA125) for detailed technical and applications information.

ORDERING INFORMATION

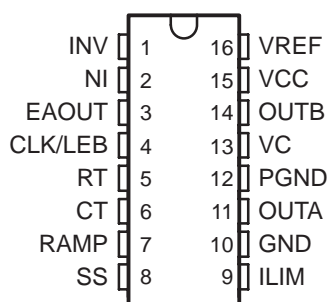
| T _A | MAXIMUM DUTY CYCLE | UVLO | | | | | |
|----------------|--------------------|--------------------------------|----------------|-------------------------------|-----------------|----------------|-------------------------------|
| | | 9.2 V / 8.4 V | | | 16 V / 10 V | | |
| | | SOIC-16 ⁽¹⁾ (DW) | PDIP-16 (N) | PLCC-20 ⁽¹⁾ (Q) | SOIC-16 (DW) | PDIP-16 (N) | PLCC-20 ⁽¹⁾ (Q) |
| -40°C to 85°C | < 100% | UC2823ADW | UC2823AN | UC2823AQ | UC2823BDW | UC2823BN | - |
| | < 50% | UC2825ADW | UC2825AN | UC2825AQ | UC2825BDW | UC2825BN | - |
| -0°C to 70°C | < 100% | UC3823ADW | UC3823AN | UC3823AQ | UC3823BDW | UC3823BN | - |
| | < 50% | UC3825ADW | UC3825AN | UC3825AQ | UC3825BDW | UC3825BN | UC3825BQ |

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

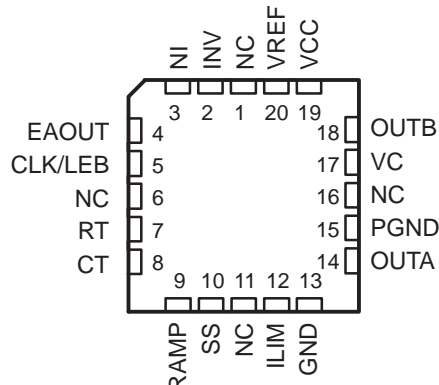
| T _A | MAXIMUM DUTY CYCLE | UVLO | |
|----------------|--------------------|--------------------------------------|--------------------------------------|
| | | 9.2 V / 8.4 V | |
| | | CDIP-16 (J) | LCCC-20 (L) |
| -55°C to 125°C | < 100% | UC1823AJ, UC1823AJ883B, UC1823AJQMLV | UC1823AL, UC1823AL883B |
| | < 50% | UC1825AJ, UC1825AJ883B, UC1825AJQMLV | UC1825AL, UC1825AL883B, UC1825ALQMLV |

PIN ASSIGNMENTS

DW, J, OR N PACKAGES
(TOP VIEW)



Q OR L PACKAGES
(TOP VIEW)



NC = no connection

TERMINAL FUNCTIONS

| NAME | TERMINAL NO. | | I/O | DESCRIPTION |
|---------|--------------|--------|-----|---|
| | J or DW | Q or L | | |
| CLK/LEB | 4 | 5 | O | Output of the internal oscillator |
| CT | 6 | 8 | I | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length. |
| EAOUT | 3 | 4 | O | Output of the error amplifier for compensation |
| GND | 10 | 13 | – | Analog ground return pin |
| ILIM | 9 | 12 | I | Input to the current limit comparator |
| INV | 1 | 2 | I | Inverting input to the error amplifier |
| NI | 2 | 3 | I | Non-inverting input to the error amplifier |
| OUTA | 11 | 14 | O | High current totem pole output A of the on-chip drive stage. |
| OUTB | 14 | 18 | O | High current totem pole output B of the on-chip drive stage. |
| PGND | 12 | 15 | – | Ground return pin for the output driver stage |
| RAMP | 7 | 9 | I | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| RT | 5 | 7 | I | Timing resistor connection pin for oscillator frequency programming |
| SS | 8 | 10 | I | Soft-start input pin which also doubles as the maximum duty cycle clamp. |
| VC | 13 | 17 | – | Power supply pin for the output stage. This pin should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor with minimal trace lengths. |
| VCC | 15 | 19 | – | Power supply pin for the device. This pin should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor with minimal trace lengths. |
| VREF | 16 | 20 | O | 5.1-V reference. For stability, the reference should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor and minimal trace length to the ground plane. |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | UNIT | |
|--------------------|---|---------------|----------------|
| V _{IN} | Supply voltage, | VC, VCC | 22 V |
| I _O | Source or sink current, DC | OUTA, OUTB | 0.5 A |
| I _O | Source or sink current, pulse (0.5 μ s) | OUTA, OUTB | 2.2 A |
| | Analog inputs | INV, NI, RAMP | –0.3 V to 7 V |
| | | ILIM, SS | –0.3 V to 6 V |
| | Power ground | PGND | \pm 0.2 V |
| I _{CLK} | Clock output current | CLK/LEB | –5 mA |
| I _{O(EA)} | Error amplifier output current | EAOUT | 5 mA |
| I _{SS} | Soft-start sink current | SS | 20 mA |
| I _{OSC} | Oscillator charging current | RT | –5 mA |
| T _J | Operating virtual junction temperature range | | –55°C to 150°C |
| T _{stg} | Storage temperature | | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | –55°C to 150°C |
| t _{STG} | Storage temperature | | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds | | 300°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**UC1823A, UC2823A, UC2823B,
UC3823A, UC3823B, UC1825A,
UC2825A, UC2825B, UC3825A, UC3825B**

SLUS334C – AUGUST 1995 – REVISED AUGUST 2004

ELECTRICAL CHARACTERISTICS

$T_A = -55^\circ\text{C}$ to 125°C for the UC1823A/UC1825A, $T_A = -40^\circ\text{C}$ to 85°C for the UC2823x/UC2825x, $T_A = 0^\circ\text{C}$ to 70°C for the UC3823x/UC3825x, $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 12\text{ V}$, $T_A = T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|---|------|------|------|----------------------------|
| REFERENCE, V_{REF} | | | | | | |
| V_O | Output voltage range | $T_J = 25^\circ\text{C}$, $I_O = 1\text{ mA}$ | 5.05 | 5.1 | 5.15 | V |
| | Line regulation | $12\text{ V} \leq V_{CC} \leq 20\text{ V}$ | | 2 | 15 | mV |
| | Load regulation | $1\text{ mA} \leq I_O \leq 10\text{ mA}$ | | 5 | 20 | |
| | Total output variation | Line, load, temperature | 5.03 | | 5.17 | V |
| | Temperature stability ⁽¹⁾ | $T_{(\text{min})} < T_A < T_{(\text{max})}$ | | 0.2 | 0.4 | mV/ $^\circ\text{C}$ |
| | Output noise voltage ⁽¹⁾ | $10\text{ Hz} < f < 10\text{ kHz}$ | | 50 | | μV_{RMS} |
| | Long term stability ⁽¹⁾ | $T_J = 125^\circ\text{C}$, 1000 hours | | 5 | 25 | mV |
| | Short circuit current | $V_{REF} = 0\text{ V}$ | 30 | 60 | 90 | mA |
| OSCILLATOR | | | | | | |
| f_{OSC} | Initial accuracy ⁽¹⁾ | $T_J = 25^\circ\text{C}$ | 375 | 400 | 425 | kHz |
| | | $R_T = 6.6\text{ k}\Omega$, $C_T = 220\text{ pF}$, $T_A = 25^\circ\text{C}$ | 0.9 | 1 | 1.1 | MHz |
| | Total variation ⁽¹⁾ | Line, temperature | | | 450 | kHz |
| | | $R_T = 6.6\text{ k}\Omega$, $C_T = 220\text{ pF}$ | 0.85 | | 1.15 | MHz |
| | Voltage stability | $12\text{ V} < V_{CC} < 20\text{ V}$ | | | 1% | |
| | Temperature stability ⁽¹⁾ | $T_{(\text{min})} < T_A < T_{(\text{max})}$ | +/- | 5% | | |
| | High-level output voltage, clock | | 3.7 | 4 | | V |
| | Low-level output voltage, clock | | | 0 | 0.2 | |
| | Ramp peak | | 2.6 | 2.8 | 3 | |
| | Ramp valley | | 0.7 | 1 | 1.25 | |
| | Ramp valley-to-peak | | 1.6 | 1.8 | 2 | |
| I_{OSC} | Oscillator discharge current | $R_T = \text{OPEN}$, $V_{CT} = 2\text{ V}$ | 9 | 10 | 11 | |
| ERROR AMPLIFIER | | | | | | |
| | Input offset voltage | | | 2 | 10 | mV |
| | Input bias current | | | 0.6 | 3 | μA |
| | Input offset current | | | 0.1 | 1 | |
| | Open loop gain | $1\text{ V} < V_O < 4\text{ V}$ | 60 | 95 | | dB |
| CMRR | Common mode rejection ratio | $1.5\text{ V} < V_{CM} < 5.5\text{ V}$ | 75 | 95 | | |
| PSRR | Power supply rejection ratio | $12\text{ V} < V_{CC} < 20\text{ V}$ | 85 | 110 | | |
| $I_{O(\text{sink})}$ | Output sink current | $V_{EAOUT} = 1\text{ V}$ | 1 | 2.5 | | mA |
| $I_{O(\text{src})}$ | Output source current | $V_{EAOUT} = 4\text{ V}$ | -0.5 | -1.3 | | |
| | High-level output voltage | $I_{EAOUT} = -0.5\text{ mA}$ | 4.5 | 4.7 | 5 | V |
| | Low-level output voltage | $I_{EAOUT} = -1\text{ mA}$ | 0 | 0.5 | 1 | |
| | Gain bandwidth product | $f = 200\text{ kHz}$ | 6 | 12 | | Mhz |
| | Slew rate ⁽¹⁾ | | 6 | 9 | | V/ μs |

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

$T_A = -55^\circ\text{C}$ to 125°C for the UC1823A/UC1825A, $T_A = -40^\circ\text{C}$ to 85°C for the UC2823x/UC2825x, $T_A = 0^\circ\text{C}$ to 70°C for the UC3823x/UC3825x,
 $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 12\text{ V}$, $T_A = T_J$ (unless otherwise noted)

| PWM COMPARATOR | | | | | |
|--|---|---|------|------|---------------|
| I _{BIAS} | Bias current, RAMP | $V_{RAMP} = 0\text{ V}$ | -1 | -8 | μA |
| | Minimum duty cycle | | | 0% | |
| | Maximum duty cycle | | 85% | | |
| t _{LEB} | Leading edge blanking time | $R_{LEB} = 2\text{ k}\Omega$, $C_{LEB} = 470\text{ pF}$ | 300 | 375 | 450 |
| R _{LEB} | Leading edge blanking resistance | $V_{CLK/LEB} = 3\text{ V}$ | 8.5 | 10.0 | 11.5 |
| V _{ZDC} | Zero dc threshold voltage, EAOUT | $V_{RAMP} = 0\text{ V}$ | 1.10 | 1.25 | 1.4 |
| t _{DELAY} | Delay-to-output time | $V_{EAOUT} = 2.1\text{ V}$, $V_{ILIM} = 0\text{ V}$ to 2 V step | | 50 | 80 |
| CURRENT LIMIT / START SEQUENCE / FAULT | | | | | |
| I _{SS} | Soft-start charge current | $V_{SS} = 2.5\text{ V}$ | 8 | 14 | 20 |
| V _{SS} | Full soft-start threshold voltage | | 4.3 | 5 | |
| I _{DSCH} | Restart discharge current | $V_{SS} = 2.5\text{ V}$ | 100 | 250 | 350 |
| I _{SS} | Restart threshold voltage | | 0.3 | 0.5 | |
| I _{BIAS} | ILIM bias current | $V_{ILIM} = 0\text{ V}$ to 2 V step | | | 15 |
| I _{CL} | Current limit threshold voltage | | 0.95 | 1 | 1.05 |
| | Overcurrent threshold voltage | | 1.14 | 1.2 | 1.26 |
| t _d | Delay-to-output time, ILIM ⁽¹⁾ | $V_{ILIM} = 0\text{ V}$ to 2 V step | | 50 | 80 |
| OUTPUT | | | | | |
| | Low-level output saturation voltage | I _{OUT} = 20 mA | | 0.25 | 0.4 |
| | | I _{OUT} = 200 mA | | 1.2 | 2.2 |
| | High-level output saturation voltage | I _{OUT} = 20 mA | | 1.9 | 2.9 |
| | | I _{OUT} = 200 mA | | 2 | 3 |
| t _r , t _f | Rise/fall time ⁽¹⁾ | $C_L = 1\text{ nF}$ | | 20 | 45 |
| UNDERVOLTAGE LOCKOUT (UVLO) | | | | | |
| | Start threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | | 16 | 17 |
| | | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | | 8.4 | 9.2 |
| | Stop threshold voltage | UC2823B, UC2825B, UC3825B, UC3825B | | 9 | 10 |
| | OVLO hysteresis | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A | | 0.4 | 0.8 |
| | | UC2823B, UC2825B, UC3825B, UC3825B | | 5 | 6 |
| SUPPLY CURRENT | | | | | |
| I _{su} | Startup current | $V_C = V_{CC} = V_{TH} = -0.5\text{ V}$ | | 100 | 300 |
| I _{CC} | Input current | | | 28 | 36 |

(1) Ensured by design. Not production tested.

APPLICATION INFORMATION

The oscillator of the UC3823A, UC3823B, UC3825A, and UC3825B is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and D_{MAX}. The design equations are:

$$R_T = \frac{3\text{ V}}{(10\text{ mA}) \times (1 - D_{MAX})} \quad C_T = \frac{(1.6 \times D_{MAX})}{(R_T \times f)} \quad (1)$$

Recommended values for R_T range from 1 kΩ to 100 kΩ. Control of D_{MAX} less than 70% is not recommended.

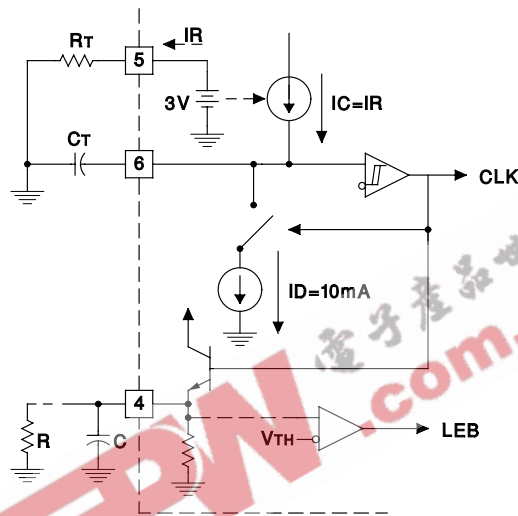


Figure 1. Oscillator

UDG-95102

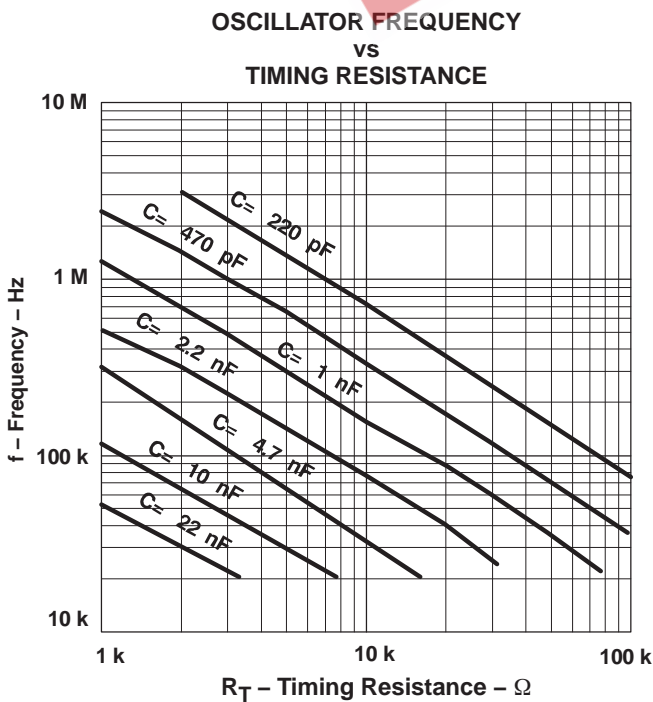


Figure 2

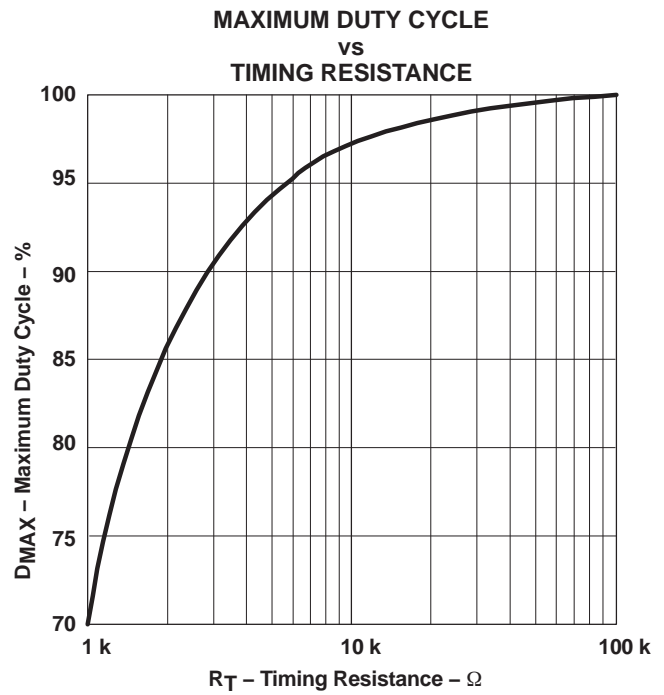


Figure 3

LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

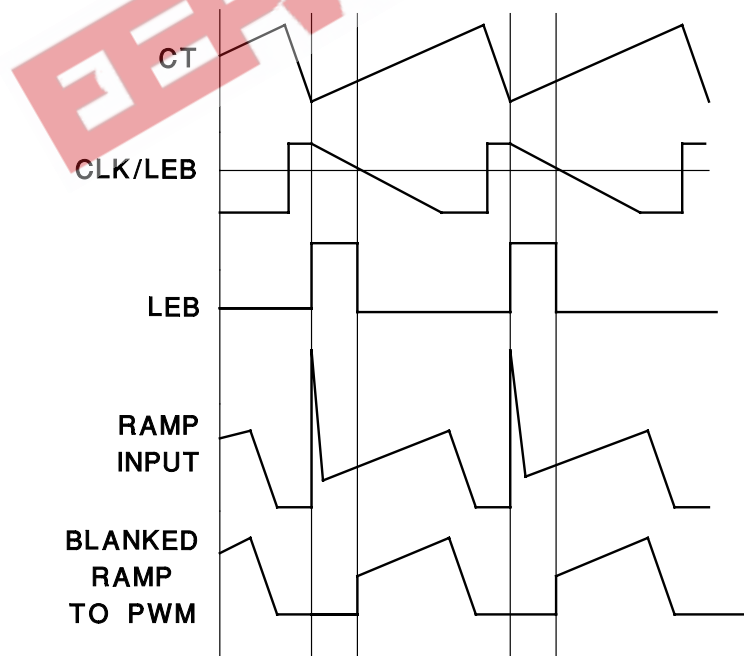
Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10 \text{ k}\Omega) \times C \quad (2)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.



UDG-95105

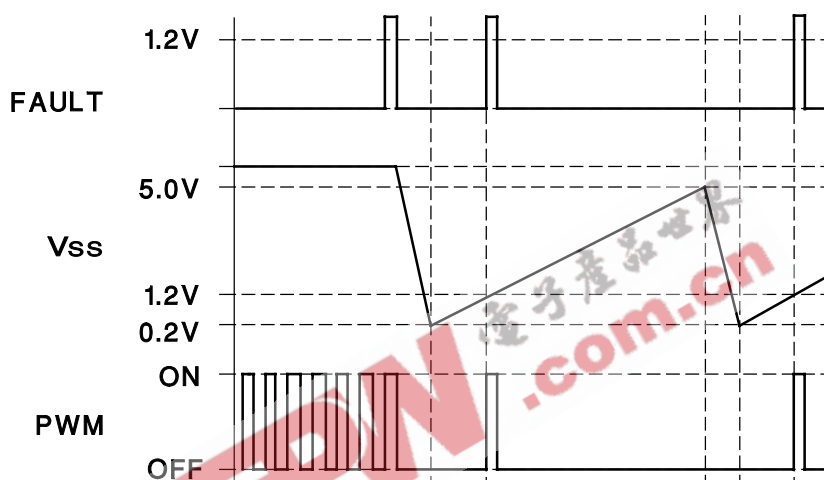
Figure 4. Leading Edge Blanking Operational Waveforms

UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9- μ A source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250- μ A current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

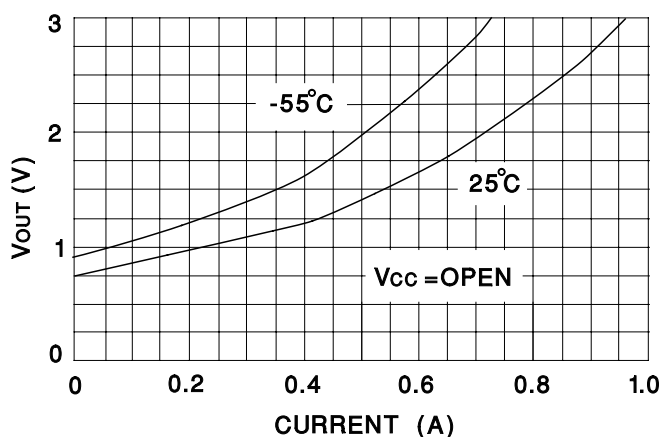


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Figure 5. Soft-Start and Fault Waveforms

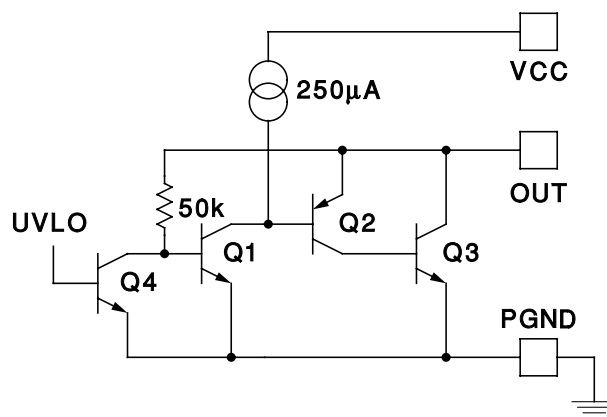
ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.



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Figure 6. Output Voltage vs Output Current



UDG-95106

Figure 7. Output V and I During UVLO

CONTROL METHODS

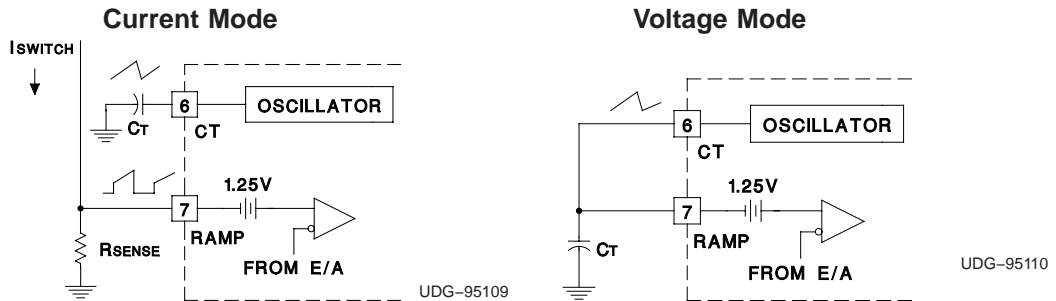


Figure 8. Control Methods

SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

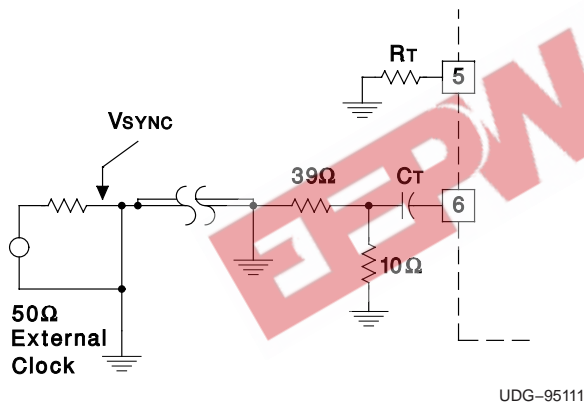


Figure 9. General Oscillator Synchronization

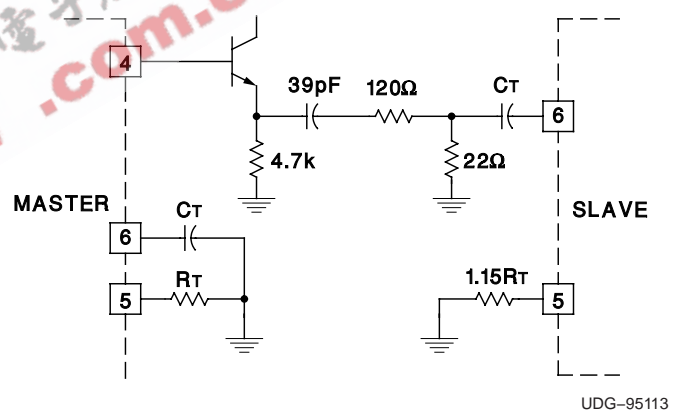
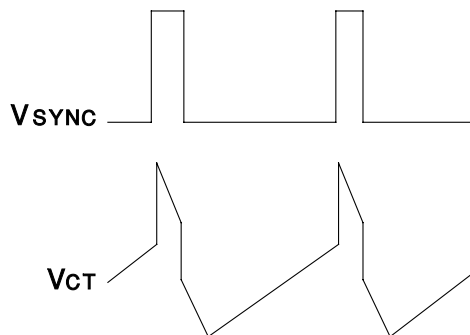


Figure 10. Two Unit Interface



UDG-95112

Figure 11. Operational Waveforms

HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A and UC3823AB, UC3825A, and UC3825B can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 13 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.

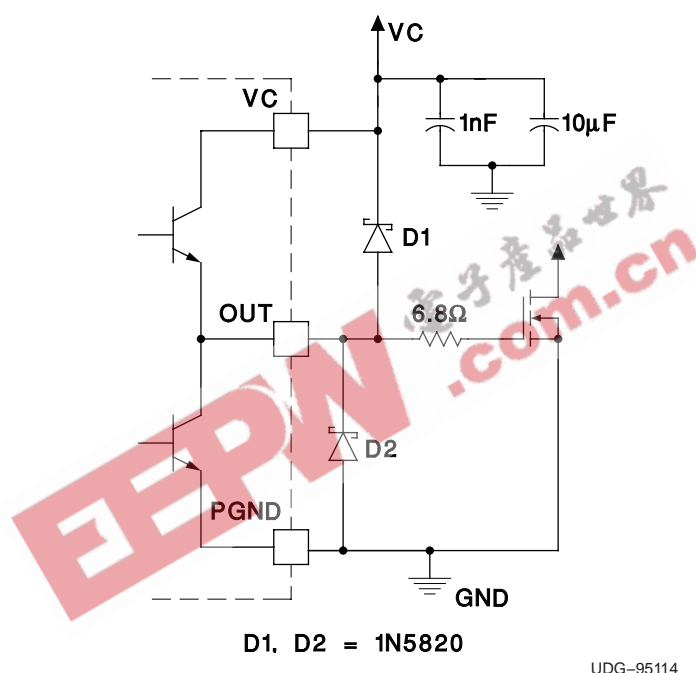
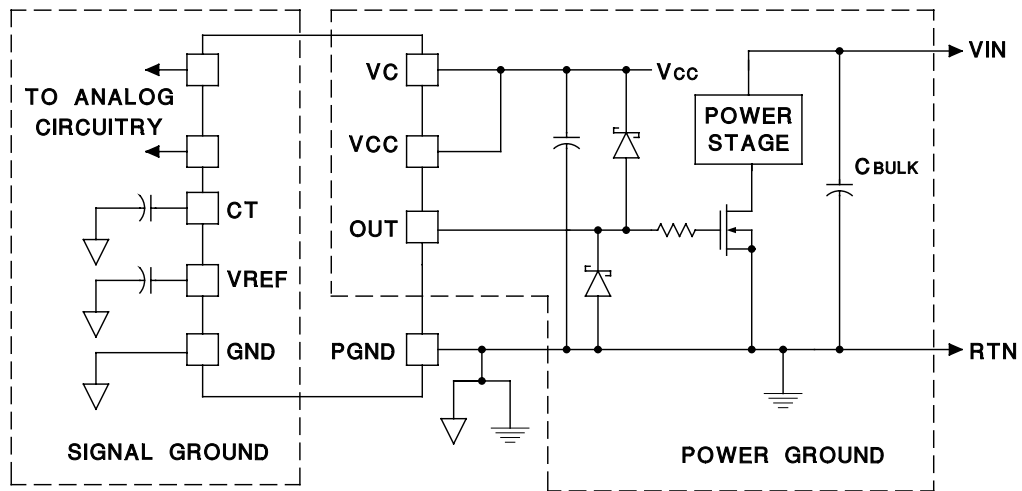


Figure 12. Power MOSFET Drive Circuit

GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

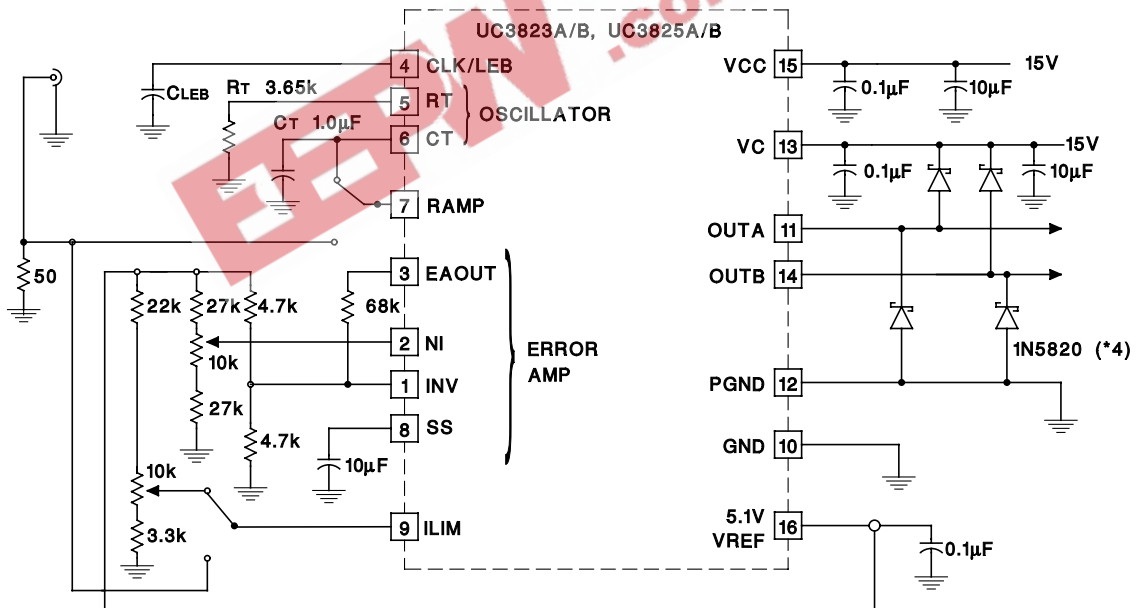


UDG-95115

Figure 13. Ground Planes Diagram

OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



UDG-95116

Figure 14. Open Loop Test Circuit Schematic

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-87681022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| 5962-8768102EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| 5962-8768102V2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-8768102VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-8768102XA | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | Call TI |
| 5962-8768103XA | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | Call TI |
| 5962-89905022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| 5962-8990502EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| 5962-8990502VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| UC1823AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| UC1823AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| UC1823AJQMLV | ACTIVE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| UC1823AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| UC1823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1823BL | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1823BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| UC1825AJ883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| UC1825AJQMLV | ACTIVE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825AL | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| UC1825AL883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | Level-NC-NC-NC |
| UC1825ALP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | Call TI |
| UC1825ALQMLV | ACTIVE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BJ883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC1825BL/81047 | OBSOLETE | TO/SOT | L | 20 | | TBD | Call TI | Call TI |
| UC1825BL883B | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UC1825BLP883B | OBSOLETE | TO-92 | LP | 28 | | TBD | Call TI | Call TI |
| UC2823ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | Level-NC-NC-NC |
| UC2823AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2823ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2823AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2823BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| UC2823BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2823BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC2823BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2823BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2825ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2825ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2825AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC2825BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC2825BJ | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| UC2825BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC2825BNG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC3823ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC3823ANG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC3823BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3823BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| UC3825ADW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |
| UC3825AQ | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825AQTR | ACTIVE | PLCC | FN | 20 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR |
| UC3825BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3825BN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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