Unitrode Products
from Texas Instruments

application INFO available

UC1846/7
UC2846/7
UC3846/7

Current Mode PWM Controller

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- ±1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHZ Operation

DESCRIPTION

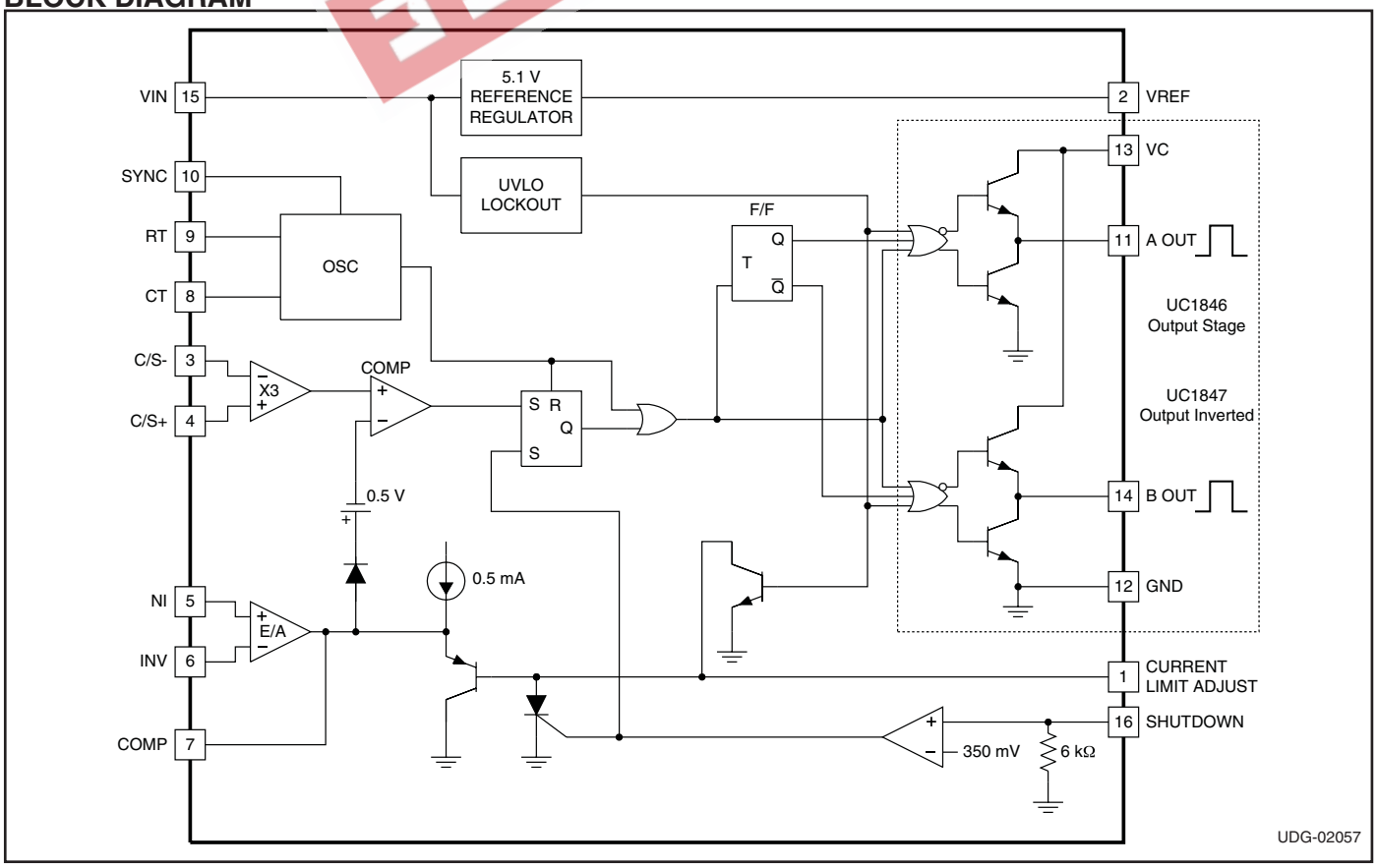
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



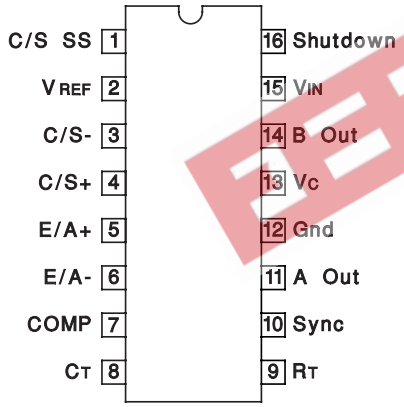
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) . . . . . +40V
Collector Supply Voltage (Pin 13) . . . . . +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16). . . . . -0.3V to +V_{IN}
Reference Output Current (Pin 2) . . . . . -30mA
Sync Output Current (Pin 10). . . . . -5mA
Error Amplifier Output Current (Pin 7) . . . . . -5mA
Soft Start Sink Current (Pin 1). 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=25°C 2000mW
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

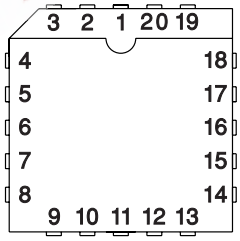
Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the speficied terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
V_{REF}	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
C_T	10
N/C	11
R_T	12
Sync	13
A Out	14
Gnd	15
N/C	16
V_C	17
B Out	18
V_{IN}	19
Shutdown	20

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J=25°C, I_O=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN}=8V to 40V		5	20		5	20	mV
Load Regulation	I_L=1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤10kHz, T_J=25°C (Note 2)		100			100		µV
Long Term Stability	T_J=125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	T_J=25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	ΔV_O=1.2 to 3V, V_{CM}=2V	80	105		80	105		dB
Unity Gain Bandwidth	T_J=25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		75	100		dB
PSRR	V_{IN}=8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		2	6		mA
Output Source Current	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM}=1V to 12V	60	83		60	83		dB
PSRR	V_{IN}=8V to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

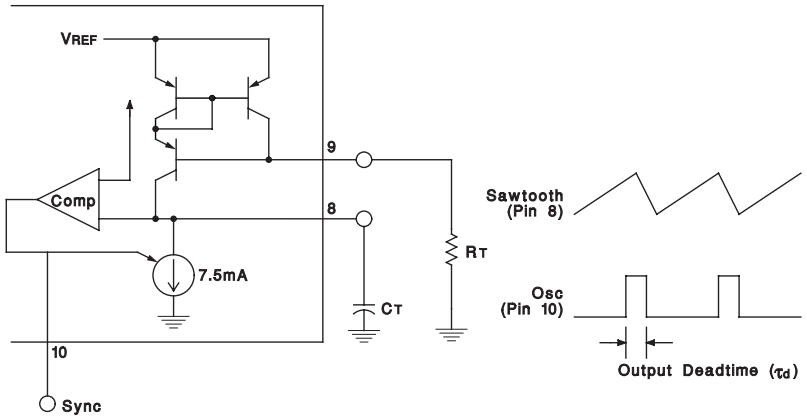
(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J=25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C=40V (Note 5)			200			200	µA
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=100mA	12	13.5		12	13.5		V
Rise Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with VPIN 5 = VREF, VPIN 6 = 0V.
Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$; V_{PIN4} = 0 to 1.0V
Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau d\ (\mu s) = 145CT\ (\mu f) \left(\frac{ID}{ID - \frac{3.6}{RT\ (k\Omega)}} \right)$.

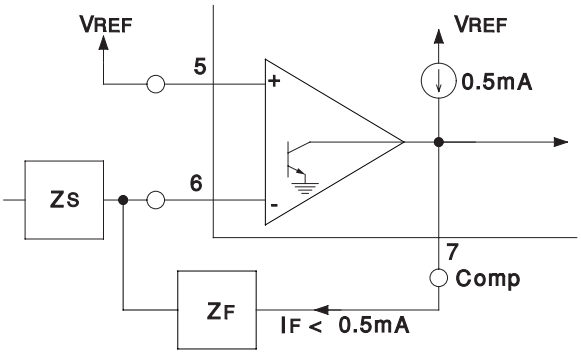
I_D = Oscillator discharge current at 25°C is typically 7.5.

For large values of R_T: $\tau d\ (\mu s) \approx 145CT\ (\mu f)$.

Oscillator frequency is approximated by the formula: $fT\ (kHz) \approx \frac{2.2}{RT\ (k\Omega) \bullet CT\ (\mu f)}$.

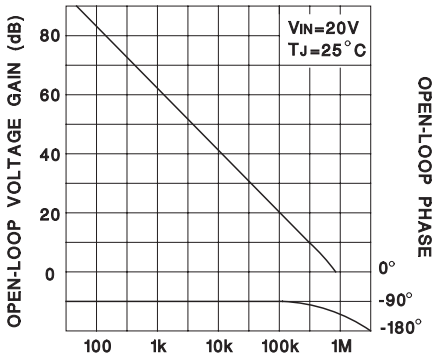
APPLICATIONS DATA (cont.)

Error Amp Output Configuration

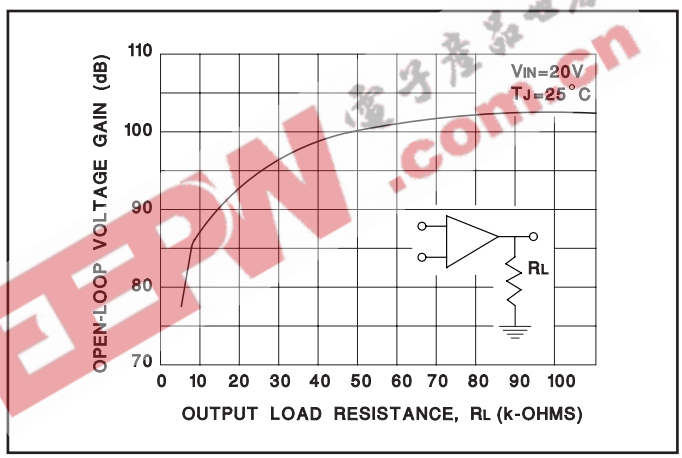


Error Amplifier can source up to 0.5mA.

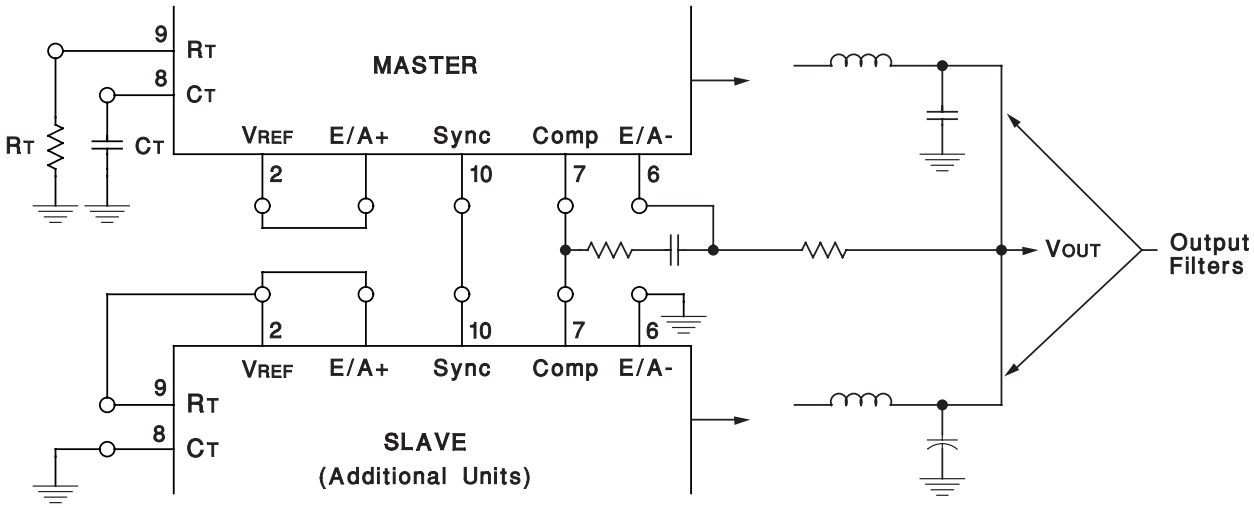
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance



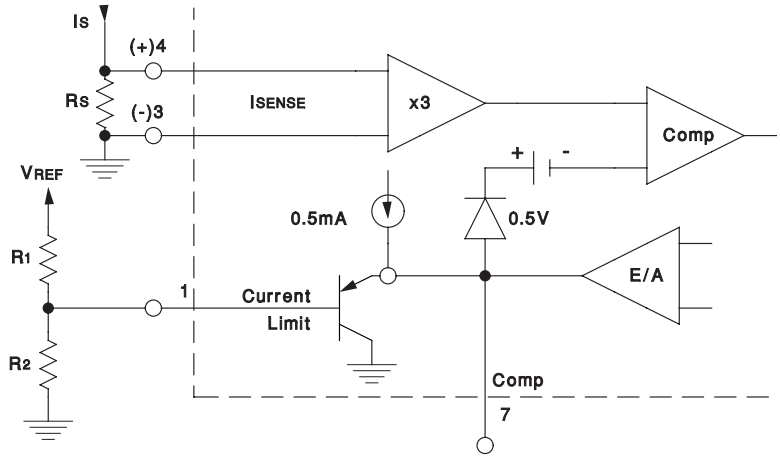
Parallel Operation



Slaving allows parallel operation of two or more units with equal current sharing.

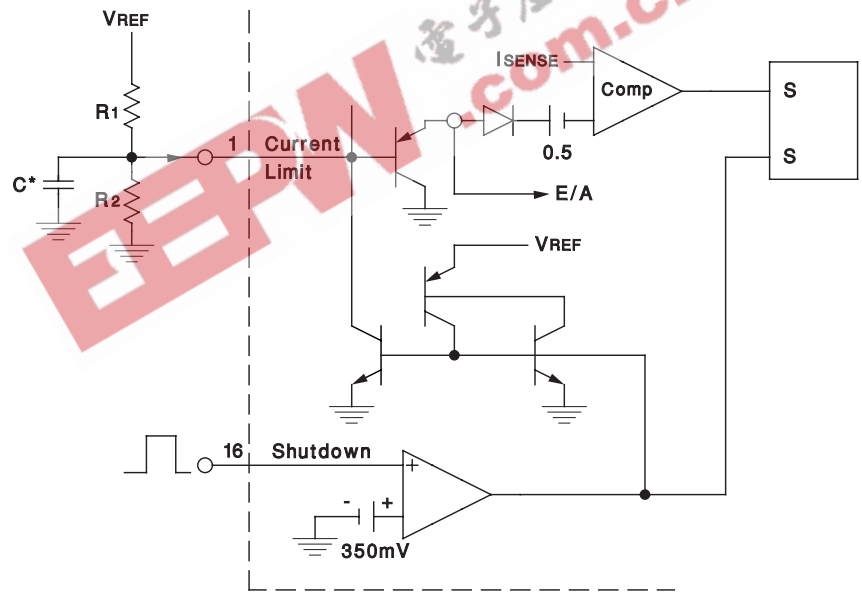
APPLICATIONS DATA (cont.)

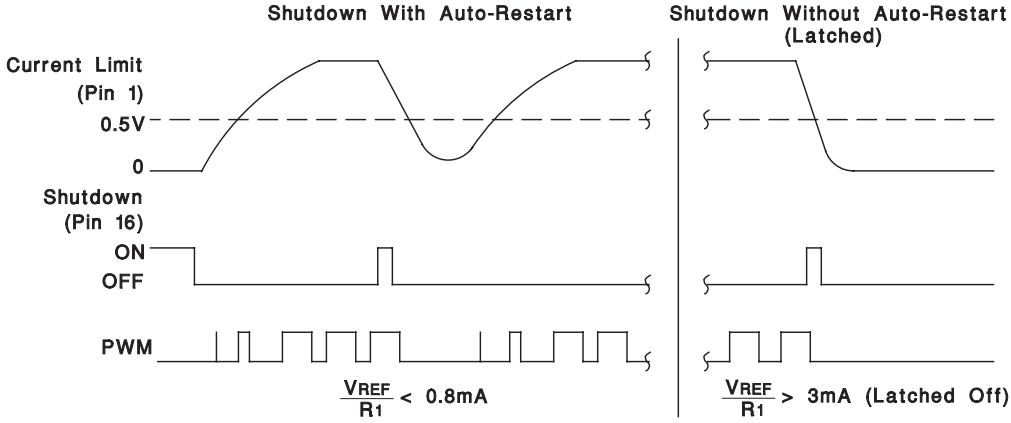
Pulse by Pulse Current Limiting



Peak Current (Is) is determined by the formula: $IS = \dfrac{\dfrac{R2\,VREF}{R1 + R2} - 0.5}{3RS}$

Soft Start and Shutdown /Restart Functions



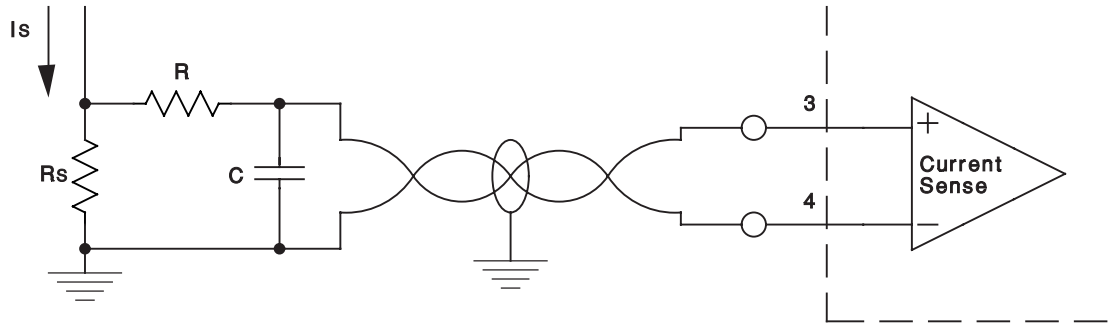


If $\frac{VREF}{R1}$ < 0.8mA, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{VREF}{R1}$ > 3mA, the device will latch off until power is recycled.

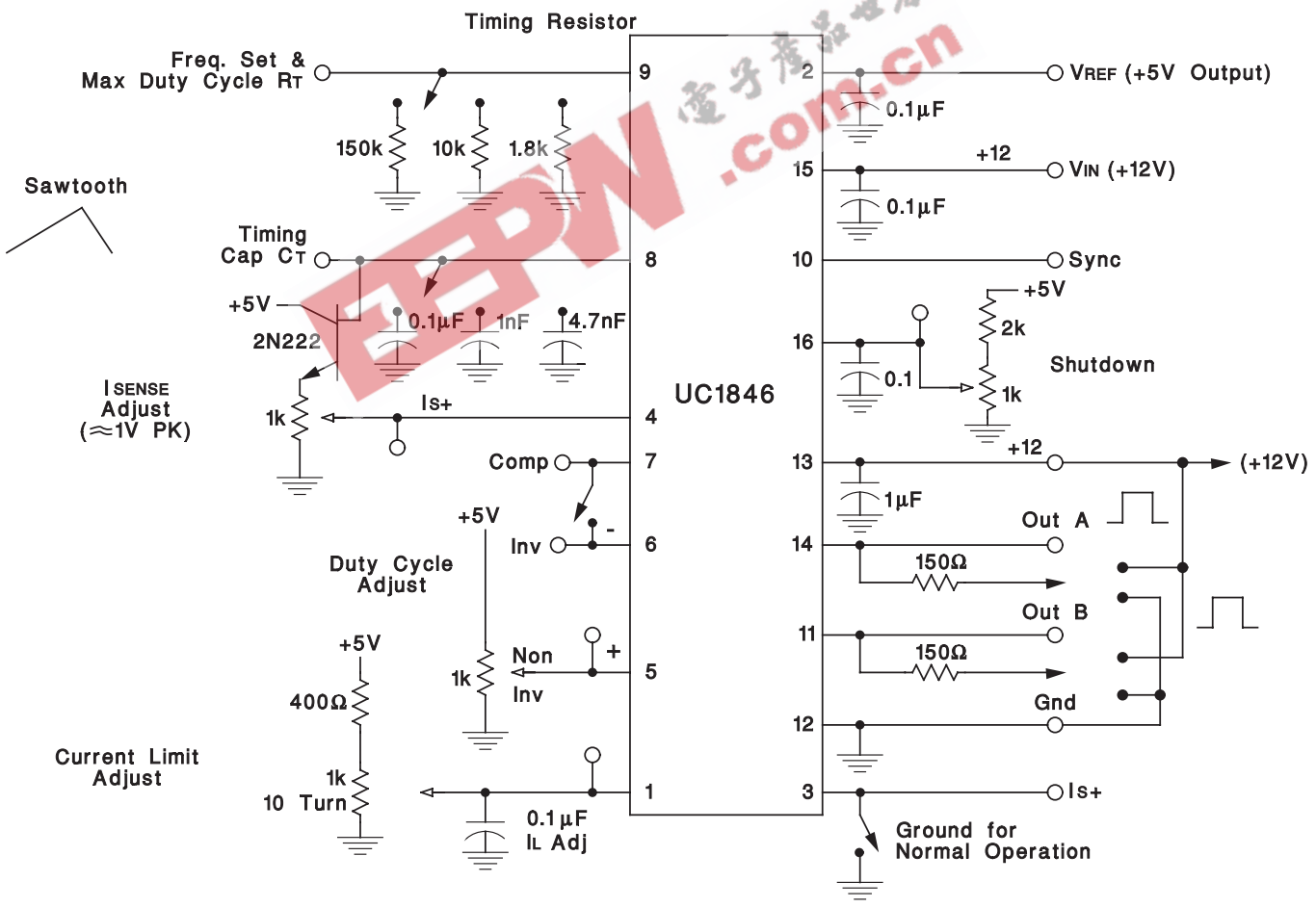
APPLICATIONS DATA (cont.)

Current Sense Amp Connection



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

UC1846 Open Loop Test Circuit



-Bypass Caps Should Be Low ESR & ESL Type
-Short Pins 6 & 7 for Unity Gain Testing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-86806012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8680601EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-8680601V2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8680601VEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
UC1846J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1846J/80257	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1846J/80364	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1846J/80619	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1846J883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1846JQMLV	ACTIVE	CDIP	J	16		TBD	Call TI	Call TI
UC1846L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1846LQMLV	ACTIVE	LCCC	FK	20		TBD	Call TI	Call TI
UC1847J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1847J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1847L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC1847L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC2846DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2846DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2846J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2846N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC2846Q	ACTIVE	PLCC	FN	20	46	TBD	Call TI	Level-2-220C-1 YEAR
UC2846QTR	ACTIVE	PLCC	FN	20	1000	TBD	Call TI	Level-2-220C-1 YEAR
UC2847DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2847DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2847N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3846DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3846DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3846J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3846N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3846Q	ACTIVE	PLCC	FN	20	46	TBD	Call TI	Level-2-220C-1 YEAR
UC3846QTR	ACTIVE	PLCC	FN	20	1000	TBD	Call TI	Level-2-220C-1 YEAR
UC3847DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3847DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3847J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC3847N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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