THESE HIGH-VOLTAGE, HIGH-CURRENT

Darlington arrays are comprised of seven silicon NPN darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

ULN2003 has a 2.7 kΩ series base resistor for each darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs particularly those beyond the capabilities of standard logic buffers.

ULN2004 has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V.

ULN2003/ULN2004 is the original high-voltage, high-current darlington array. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the off state. Output may be paralle-led for higher load-current capability.

ULN2003/ULN2004 darlington arrays are furnished in a 16-Pin dual in-line plastic package. These can also be supplyed in a hermetic dual in-line package for use in military and aerospace applications.

DEVICE NUMBER DESIGNATION

VCE(MAX)	50V
IC(MAX)	500mA

Logic	Type Number
5V TTL, CMOS	ULN2003
6-15V CMOS,PMOS	ULN2004
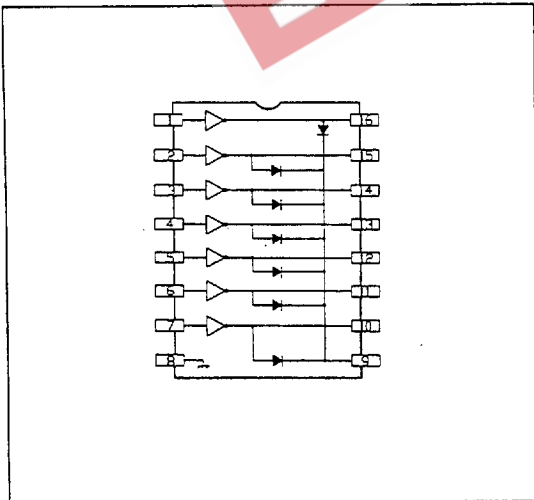
ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE
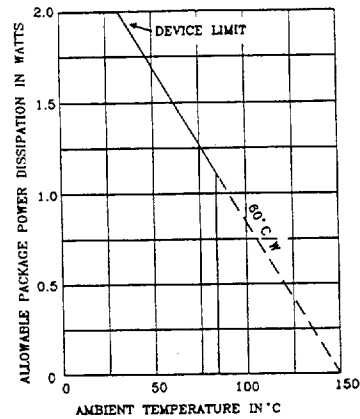
ABSOLUTE MAXIMUM RATINGS

at +25 ℃ Free – Air Temperature
(unless otherwise noted)

Input Voltage, V_{IN} (ULN2003, ULN2004) · 30 V

Continuous Input Current, I_{IN} · 25 mA

Power Dissipation, P_D (one Darlington pair) · 1.0 W

(total package) · 2.0 W*

Operating Ambient Temperature Range, T_A · – 20℃ to + 85℃

Storage Temperature Range, T_S · – 55℃ to + 150℃

* Debate at the rate of 16.67 mW/℃ above + 25℃ .

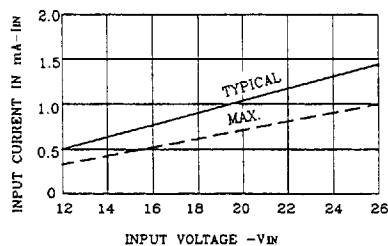Under normal operating conditions, these devices will sustain 350 mA per output with

$V_{CE(STA)}$ = 1.6 V at +70℃ with a pulse width of 20 ms and a duty cycle of 34%.
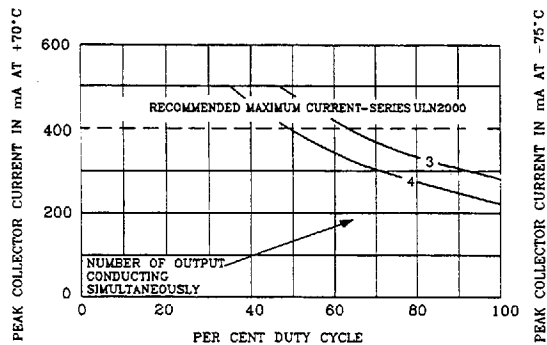
PARTIAL SCHEMATICS

Series ULN2003
(each driver)
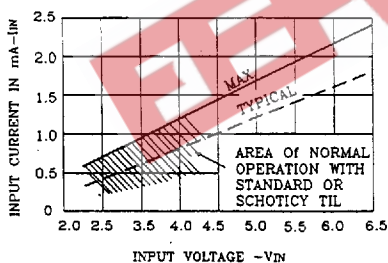
Series ULN2004
(each driver)

**PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE**

ELECTRICAL CHARACTERISTICS AT +25℃ (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	V_{CE}=50V, T_A=25℃	–	–	50	μA
				V_{CE}=50V, T_A=70℃	–	–	100	μA
		1B	ULN2004	V_{CE}=50V, T_A=70℃, V_{IN}=1.0V	–	–	500	μA
Collector - Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C=100mA, I_S=250μA	–	0.9	1.1	V
				I_C=200mA, I_S=350μA	–	1.1	1.3	V
				I_C=350mA, I_S=500μA	–	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN2003	V_{IN}=3.85V	–	0.93	1.35	mA
			ULN2004	V_{IN}=5.0V	–	0.35	0.5	mA
				V_{IN}=12V	–	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C=500μA, T_A=70℃	50	65	–	μA
Input Voltage	$V_{IN(ON)}$	5	ULN2003	V_{CE}=2.0V, I_C=200mA	–	–	2.4	V
				V_{CE}=2.0V, I_C=250mA	–	–	2.7	V
				V_{CE}=2.0V, I_C=300mA	–	–	3.0	V
			ULN2004	V_{CE}=2.0V, I_C=125mA	–	–	5.0	V
				V_{CE}=2.0V, I_C=200mA	–	–	6.0	V
				V_{CE}=2.0V, I_C=275mA	–	–	7.0	V
				V_{CE}=2.0V, I_C=350mA	–	–	8.0	V
Input Capacitance	C_{IN}	–	All		–	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	–	0.25	1.0	μS
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	–	0.25	1.0	μS
Clamp Diode Leakage Current	I_R	6	All	V_R=50V, T_A=25℃	–	–	50	μA
				V_R=50V, T_A=70℃	–	–	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F=350mA	–	1.7	2.0	V

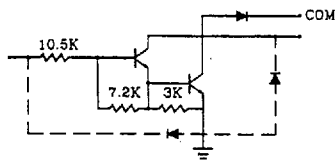**COLLECTOR CURRENT AS A FUNCTION OF SATRATION VOLTAGE**
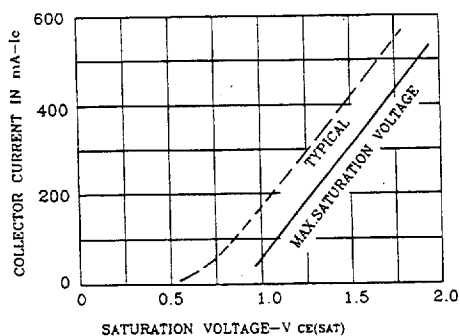
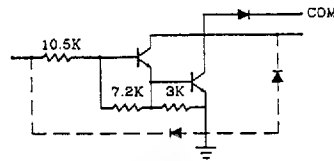**COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT**
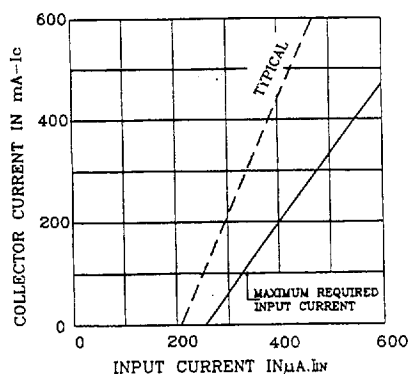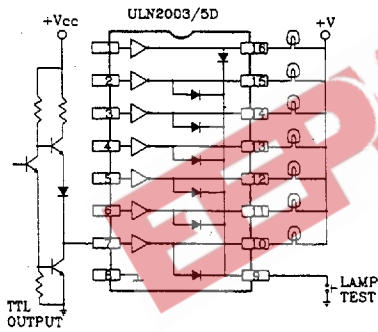
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE
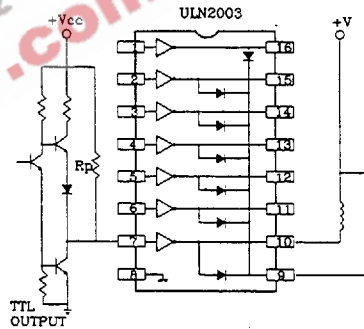
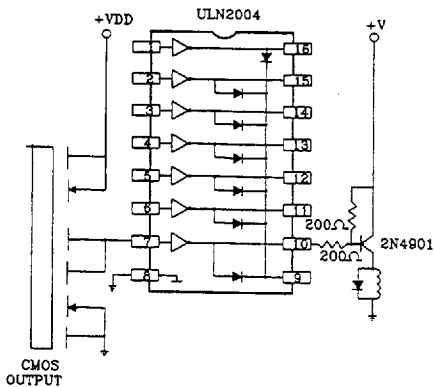**SERIES ULN2003**

SERIES ULN2004

TTL TO LOAD

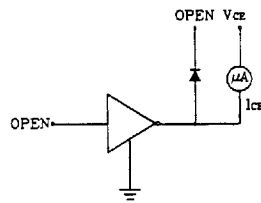**USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT**

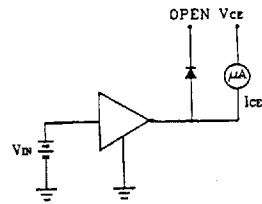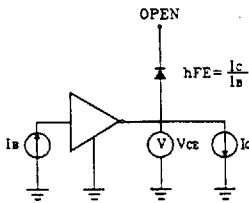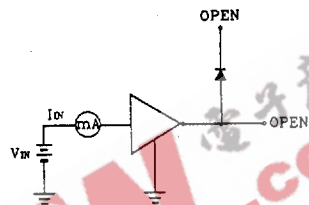**BUFFER FOR HIGH-CURRENT LOAD**

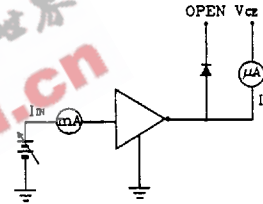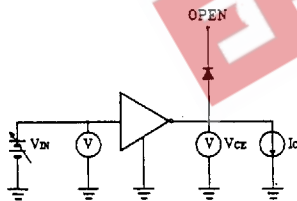**TEST FIGURES**

FIGURE 1A

FIGURE 1B

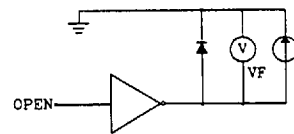FIGURE 2

$hFE = \dfrac{I_C}{I_B}$

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

FIGURE 7