0.45-Ω QUAD SPDT ANALOG SWITCH
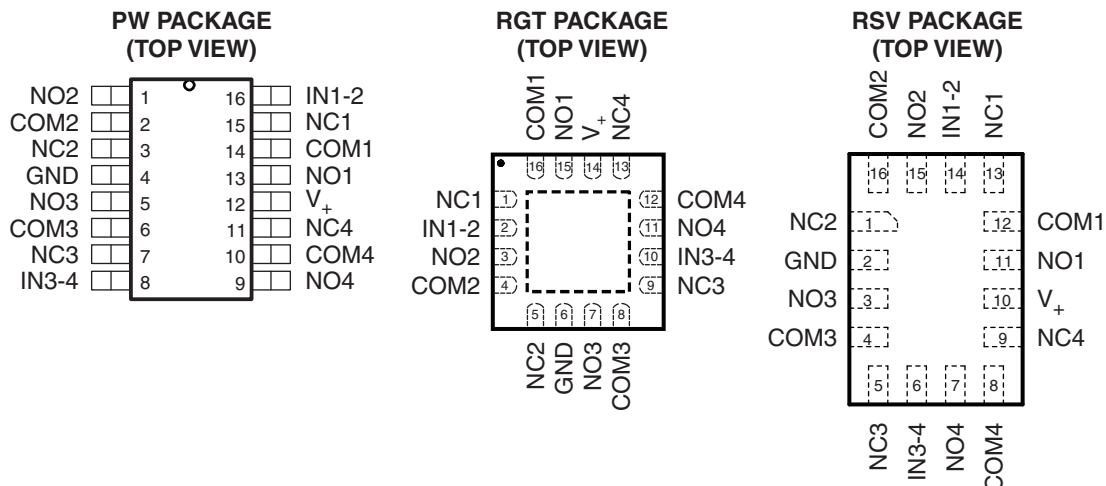# QUAD-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER WITH TWO CONTROLS

FEATURES

- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (<0.5 Ω)**
- **Control Inputs Are 1.8-V Logic Compatible**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 4.3-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio and Video Signal Routing**
- **Low-Voltage Data-Acquisition Systems**
- **Communication Circuits**
- **Modems**
- **Hard Drives**
- **Computer Peripherals**
- **Wireless Terminals and Peripherals**

PW PACKAGE (TOP VIEW)

NO2	1	16	IN1-2
COM2	2	15	NC1
NC2	3	14	COM1
GND	4	13	NO1
NO3	5	12	V_+
COM3	6	11	NC4
NC3	7	10	COM4
IN3-4	8	9	NO4

RGT PACKAGE (TOP VIEW)

Top pins: COM1, NO1, V_+, NC4

NC1	1	12 COM4
IN1-2	2	11 NO4
NO2	3	10 IN3-4
COM2	4	9 NC3

Bottom pins: NC2, GND, NO3, COM3

RSV PACKAGE (TOP VIEW)

Top pins: COM2, NO2, IN1-2, NC1

NC2	1	12 COM1
GND	2	11 NO1
NO3	3	10 V_+
COM3	4	9 NC4

Bottom pins: NC3, IN3-4, NO4, COM4

DESCRIPTION/ORDERING INFORMATION

The TS3A44159 is a quad single-pole double-throw (SPDT) analog switch with two control inputs, which is designed to operate from 1.65 V to 4.3 V. This device is also known as a dual double-pole double-throw (DPDT) configuration. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS3A44159

ORDERING INFORMATION

T_A	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	RGT – QFN	Tape and reel	TS3A44159RGTR	ZWH
	RSV – QFN	Tape and reel	TS3A44159RSVR	ZWH
	PW – TSSOP	Tape and reel	TS3A44159PWR	YC4159

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
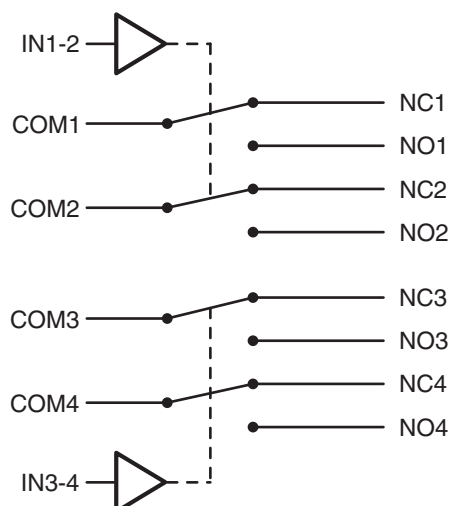
SUMMARY OF CHARACTERISTICS[1]

Configuration	Quad 2:1 Multiplexer/Demultiplexer (4 × SPDT or 2 × DPDT)
Number of channels	4
ON-state resistance (r_{on})	0.45 Ω (max)
ON-state resistance match (Δr_{on})	0.07 Ω (max)
ON-state resistance flatness ($r_{ON(flat)}$)	0.1 Ω (max)
Turn-on/turn-off time (t_{ON}/t_{OFF})	23 ns/32 ns
Break-before-make time (t_{BBM})	30 ns
Charge injection (Q_C)	139 pC
Bandwidth (BW)	35 MHz
OFF isolation (O_{ISO})	−71 dB
Crosstalk (X_{TALK})	−73 dB
Total harmonic distortion (THD)	0.003%
Power-supply current (I_+)	0.4 µA
Package option	16-pin QFN

(1) V_+ = 4.3 V, T_A = 25°C

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

LOGIC DIAGRAM

Copyright © 2007–2008, Texas Instruments Incorporated

Product Folder Link(s): TS3A44159

ABSOLUTE MAXIMUM RATINGS[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[3]		−0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[3][4][5]		−0.5	$V_+ + 0.5$	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	−50		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	−200	200	mA
	ON-state peak switch current[6]		−400	400	
V_I	Digital input voltage range		−0.5	4.6	V
I_{IK}	Digital input clamp current[3][4]	V_I < 0	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
θ_{JA}	Package thermal impedance[7]	PW package		108	°C/W
		RGT package		TBD	
		RSV package		TBD	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 4.6 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

TS3A44159

ELECTRICAL CHARACTERISTICS FOR 4.3-V SUPPLY[1]

$T_A = -40°C$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.3	0.45	Ω
				Full				0.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.05	0.07	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	4.3 V		0.02	0.1	Ω
				Full				0.1	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 3.0 V, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = 0.3 V,	See Figure 17	25°C	4.3 V	−20	5	20	nA
				Full		−90		90	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = Open,	See Figure 18	25°C	4.3 V	−20	5	20	nA
				Full		−90		90	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 3.0 V,	See Figure 18	25°C	4.3 V	−20	5	20	nA
				Full		−90		90	
Digital Control Inputs (IN1-2, IN3-4)[2]									
Input logic high	V_{IH}			Full	4.3 V	1.5		4.3	V
Input logic low	V_{IL}			Full	4.3 V	0		1	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 3.6 V or 0		25°C	4.3 V		0.5	10	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Link(s): *TS3A44159*

ELECTRICAL CHARACTERISTICS FOR 4.3-V SUPPLY (continued)

T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF	25°C	4.3 V		17	23	ns
				Full				25	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF	25°C	4.3 V		12	32	ns
				Full				35	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF	25°C	4.3 V	2	9	30	ns
				Full		1		35	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1$ nF	25°C	4.3 V		139		pC
NC, NO off capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	4.3 V		50		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	4.3 V		160		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 19	25°C	4.3 V		160		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND		25°C	4.3 V		2.5		pF
Bandwidth	BW	$R_L = 50\ \Omega$,	Switch ON	25°C	4.3 V		35		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 100$ kHz,	Switch OFF	25°C	4.3 V		−71		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 100$ kHz,	Switch ON	25°C	4.3 V		−73		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50$ pF,	$f = 20$ Hz to 20 kHz	25°C	4.3 V		0.003		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	4.3 V		0.15	0.4	µA
				Full				1.2	

Submit Documentation Feedback   5

Product Folder Link(s): *TS3A44159*

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY[1]

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.0 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	3 V		0.37	0.55	Ω
				Full				0.6	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.0 V, 0.8 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	3 V		0.06	0.07	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} or V_{NC} = 2.0 V, 0.8 V I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	3 V		0.05	0.1	Ω
				Full				0.1	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 3.0 V, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = 0.3 V,	See Figure 17	25°C	3.6 V	−15	5	15	nA
				Full		−50		50	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3.0 V, V_{COM} = Open,	See Figure 18	25°C	3.6 V	−15	5	15	nA
				Full		−50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 3.0 V,	See Figure 18	25°C	3.6 V	−15	5	15	nA
				Full		−50		50	
Digital Control Inputs (IN1-2, IN3-4)[2]									
Input logic high	V_{IH}			Full		1.25		4.3	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 3.6 V or 0		25°C	3.6 V		0.5	10	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS			T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic										
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,		C_L = 35 pF	25°C	3 V		20	38	ns
					Full	3 V to 3.6 V			40	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,		C_L = 35 pF	25°C	3 V		14	34	ns
					Full	3 V to 3.6 V			35	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,		C_L = 35 pF	25°C	3 V	3	11	35	ns
					Full	3 V to 3.6 V	2		55	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,		C_L = 1 nF	25°C	3 V		109		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,		See Figure 19	25°C	3 V		51		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,		See Figure 19	25°C	3 V		162		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,		See Figure 19	25°C	3 V		162		pF
Digital input capacitance	C_I	V_I = V_+ or GND			25°C	3 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω,		Switch ON	25°C	3 V		35		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 100 kHz,		Switch OFF	25°C	3 V		–71		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 100 kHz,		Switch ON	25°C	3 V		–73		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,		f = 20 Hz to 20 kHz	25°C	3 V		0.003		%
Supply										
Positive supply current	I_+	V_I = V_+ or GND,		Switch ON or OFF	25°C	3.6 V		0.015	0.2	µA
					Full				0.7	

TS3A44159

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY[1]

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.45	0.6	Ω
				Full				0.7	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.045	0.07	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} or V_{NC} = 1.8 V, 0.8 V I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.06	0.15	Ω
				Full				0.2	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 2.3 V, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = 0.3V,	See Figure 17	25°C	2.7 V	−10	0.5	10	nA
				Full		−20		20	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = Open,	See Figure 18	25°C	2.7 V	−10	0.1	10	nA
				Full		−20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 2.3 V,	See Figure 18	25°C	2.7 V	−10	0.1	10	nA
				Full		−20		20	
Digital Control Inputs (IN1-2, IN3-4)[2]									
Input logic high	V_{IH}			Full		1.2		4.3	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 3.6 V or 0		25°C	2.7 V		0.5	10	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Link(s): TS3A44159

TS3A44159

www.ti.com   SCDS225A−MARCH 2007−REVISED JUNE 2008

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V		2.6	47	ns
				Full	2.3 V to 2.7 V			50	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V		16.5	34	ns
				Full	2.3 V to 2.7 V			35	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	2.5 V	4	15	35	ns
				Full	2.3 V to 2.7 V	3		35	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF	25°C	2.5 V		84		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	2.5 V		52		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	2.5 V		163		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND,	See Figure 19	25°C	2.5 V		163		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND		25°C	2.5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON	25°C	2.5 V		35		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	2.5 V		−71		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	2.5 V		−73		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz	25°C	2.5 V		0.009		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.5 V		0.004	0.1	µA
				Full				0.5	

Copyright © 2007–2008, Texas Instruments Incorporated   Submit Documentation Feedback   9

Product Folder Link(s): TS3A44159

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY[1]

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.5	0.7	Ω
				Full				0.8	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.5 V, 0.6 V I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.05	0.07	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} or V_{NC} = 1.5 V, 0.6 V 1.5 V, 2.5 V, I_{COM} = −100 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.5	0.7	Ω
				Full				0.8	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = 0.3 V,	See Figure 17	25°C	1.95 V	−10	0.5	10	nA
				Full		−20		20	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = Open,	See Figure 18	25°C	1.95 V	−10	0.1	10	nA
				Full		−20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.3V, or V_{NO} or V_{NC} = Open, V_{COM} = 1.65 V,	See Figure 18	25°C	1.95 V	−10	0.1	10	nA
				Full		−20		20	
Digital Control Inputs (IN1-2, IN3-4)[2]									
Input logic high	V_{IH}			Full		1		4.3	V
Input logic low	V_{IL}			Full		0		0.4	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 3.6 V or 0		25°C	1.95 V		0.5	10	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V		40	70	ns
				Full	1.65 V to 1.95 V			75	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V		22	45	ns
				Full	1.65 V to 1.95 V			50	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF	25°C	1.8 V	5	25	70	ns
				Full	1.65 V to 1.95 V	4		75	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	C_L = 1 nF	25°C	1.8 V		64		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	1.8 V		52		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 19	25°C	1.8 V		164		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 19	25°C	1.8 V		164		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND		25°C	1.8 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON	25°C	1.8 V		35		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 100 kHz,	Switch OFF	25°C	1.8 V		−71		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 100 kHz,	Switch ON	25°C	1.8 V		−73		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz	25°C	1.8 V		0.1		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.05	µA
				Full				0.15	

Product Folder Link(s): TS3A44159

TYPICAL PERFORMANCE
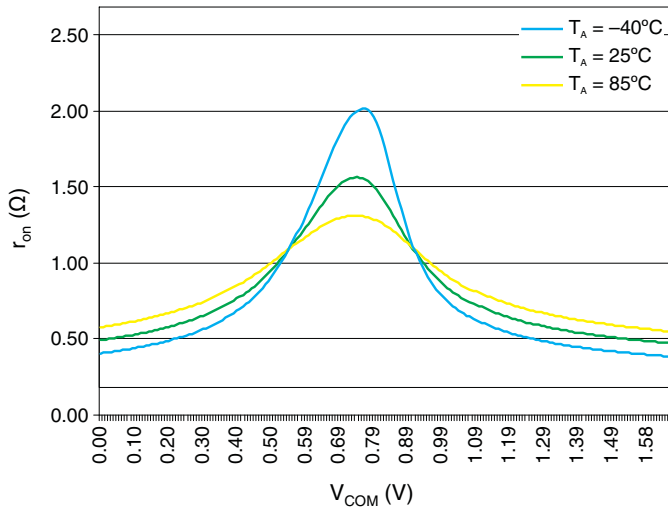
Figure 1. r_on vs V_COM
(V_+ = 1.65 V)
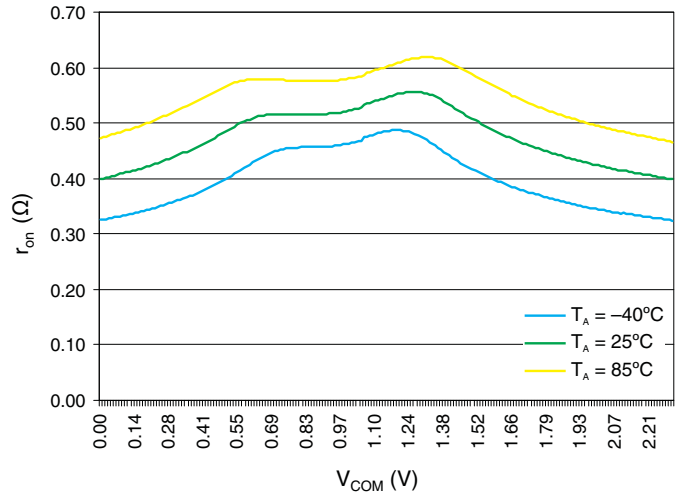
Figure 2. r_on vs V_COM
(V_+ = 2.3 V)
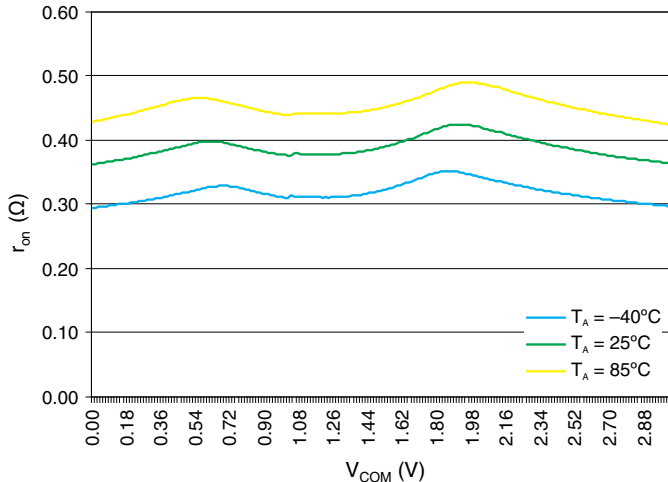
Figure 3. r_on vs V_COM
(V_+ = 3 V)
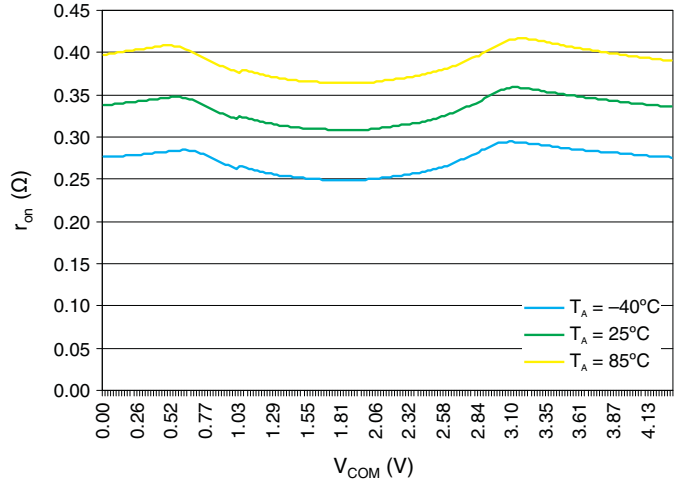
Figure 4. r_on vs V_COM
(V_+ = 4.3 V)
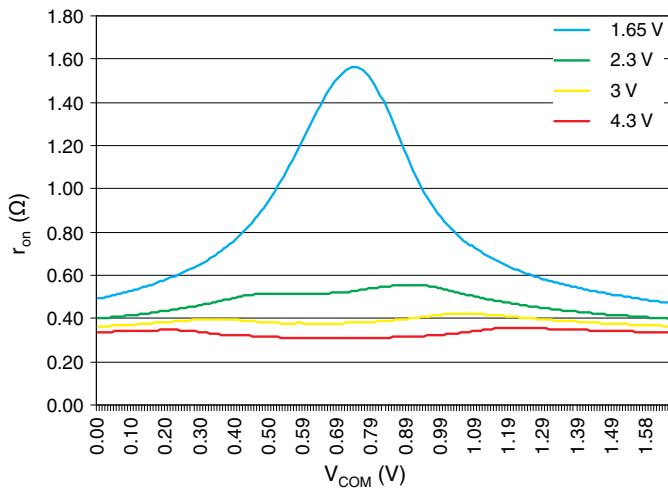
Figure 5. r_on vs V_COM
(All Voltages)
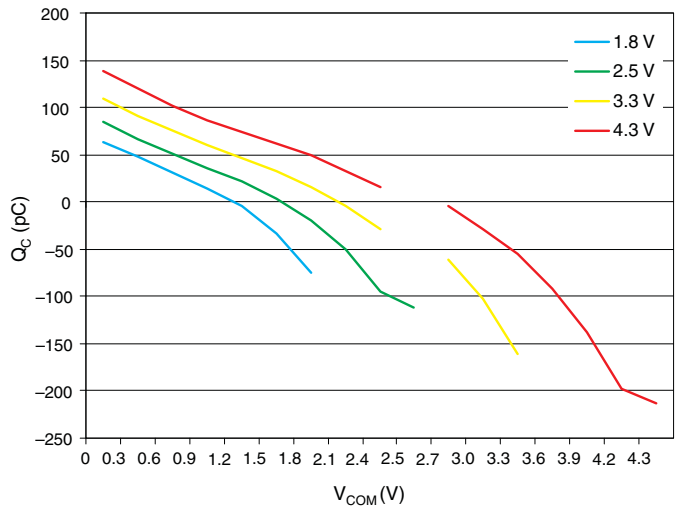
Figure 6. Charge Injection (Q_C) vs V_COM
(T_A = 25°C)

Submit Documentation Feedback

Product Folder Link(s): *TS3A44159*

TYPICAL PERFORMANCE (continued)
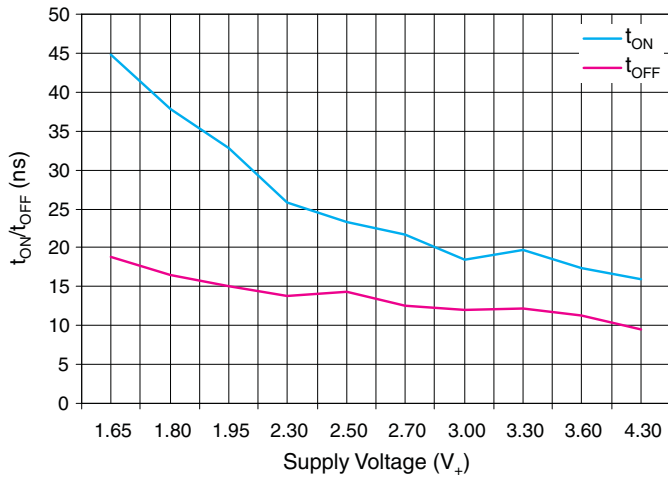
Figure 7. t_ON and t_OFF vs Supply Voltage (T_A = 25°C)
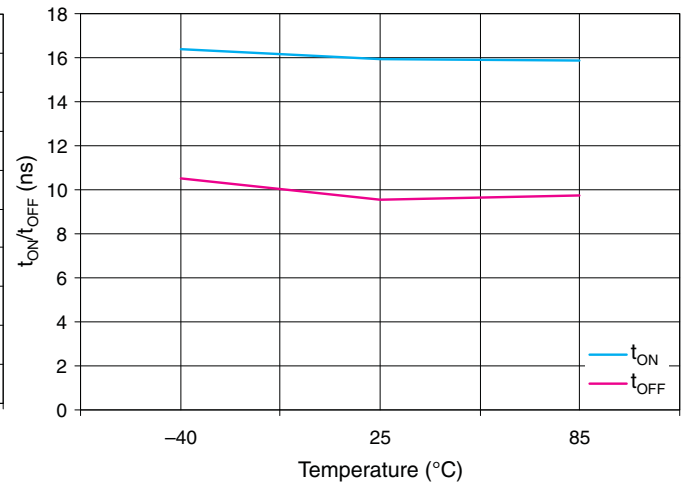
Figure 8. t_ON and t_OFF vs Temperature (V_+ = 4.3 V)
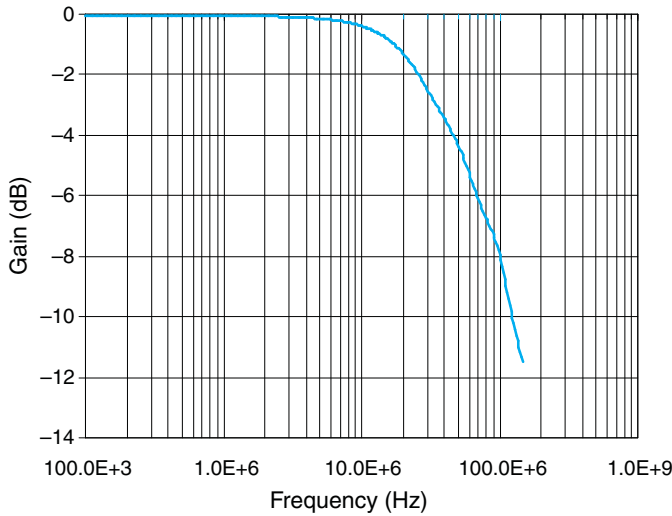
Figure 9. Bandwidth
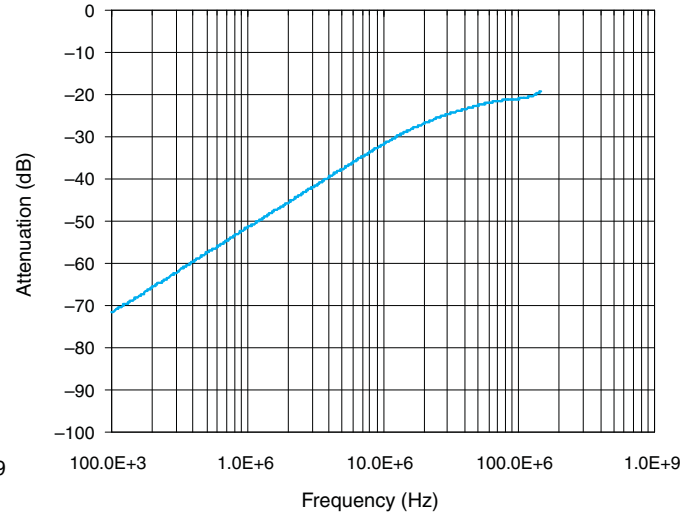
Figure 10. OFF Isolation
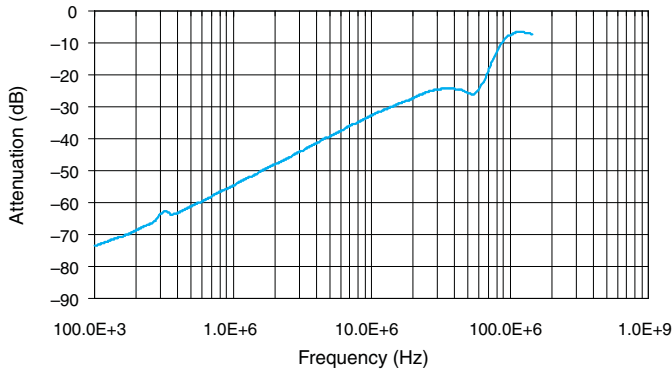
Figure 11. Crosstalk
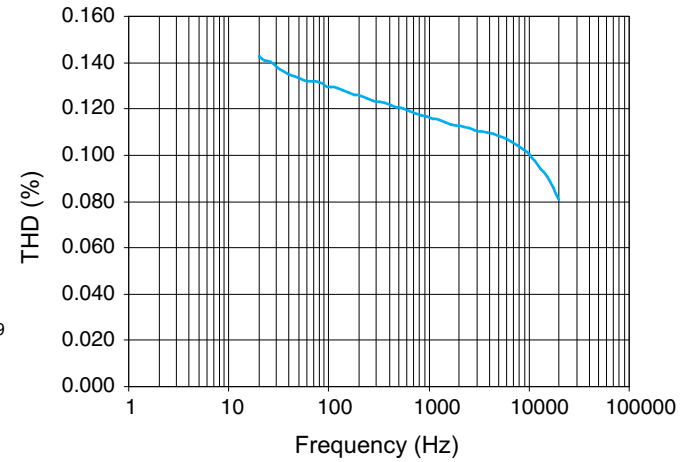
Figure 12. Total Harmonic Distortion vs Frequency (V_+ = 1.8 V)

Product Folder Link(s): TS3A44159

TYPICAL PERFORMANCE (continued)
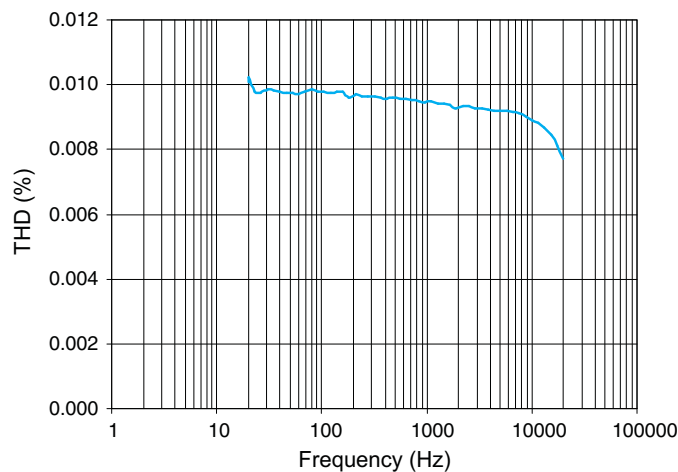
Figure 13. Total Harmonic Distortion vs Frequency
(V$_+$ = 2.5 V)
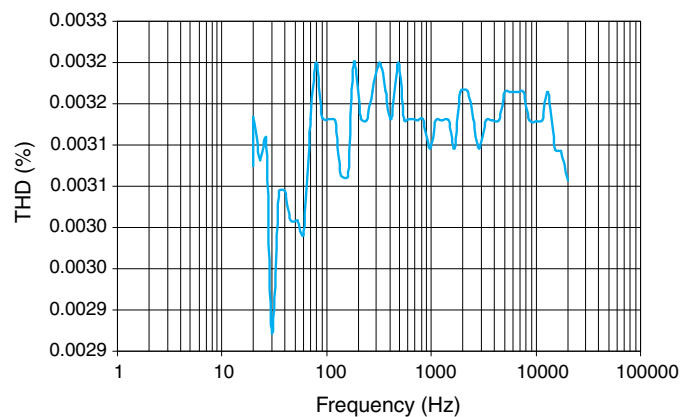
Figure 14. Total Harmonic Distortion vs Frequency
(V$_+$ = 3.3 V)
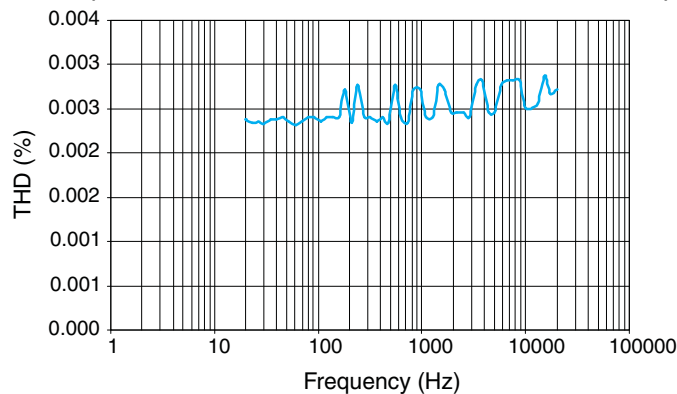
Figure 15. Total Harmonic Distortion vs Frequency
(V$_+$ = 4.3 V)

Product Folder Link(s): *TS3A44159*

PARAMETER MEASUREMENT INFORMATION
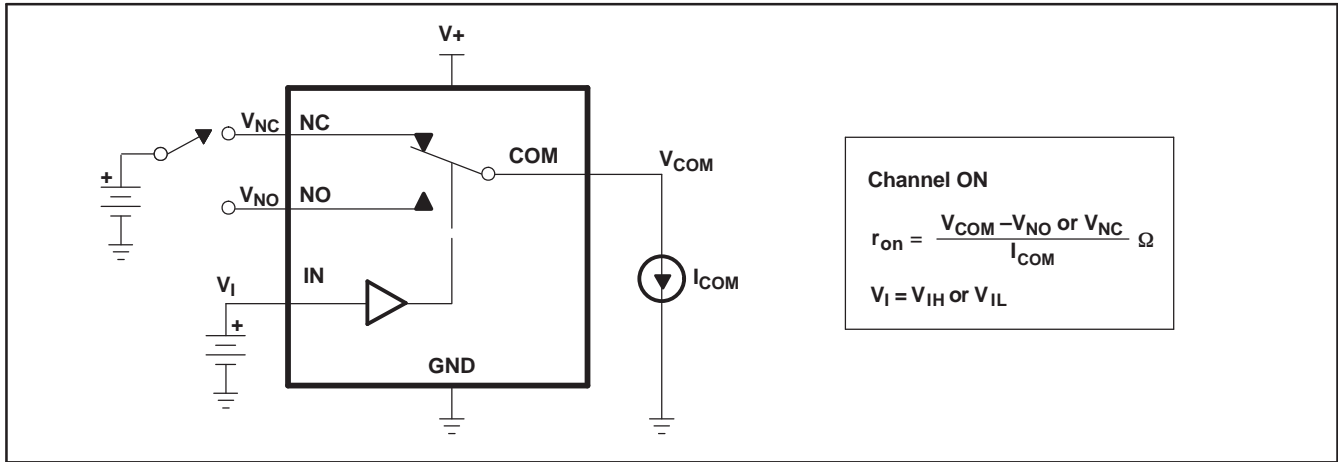
Figure 16. ON-state Resistance (r$_{ON}$)

Channel ON

$$r_{on} = \frac{V_{COM} - V_{NO} \text{ or } V_{NC}}{I_{COM}} \, \Omega$$

$V_I = V_{IH} \text{ or } V_{IL}$
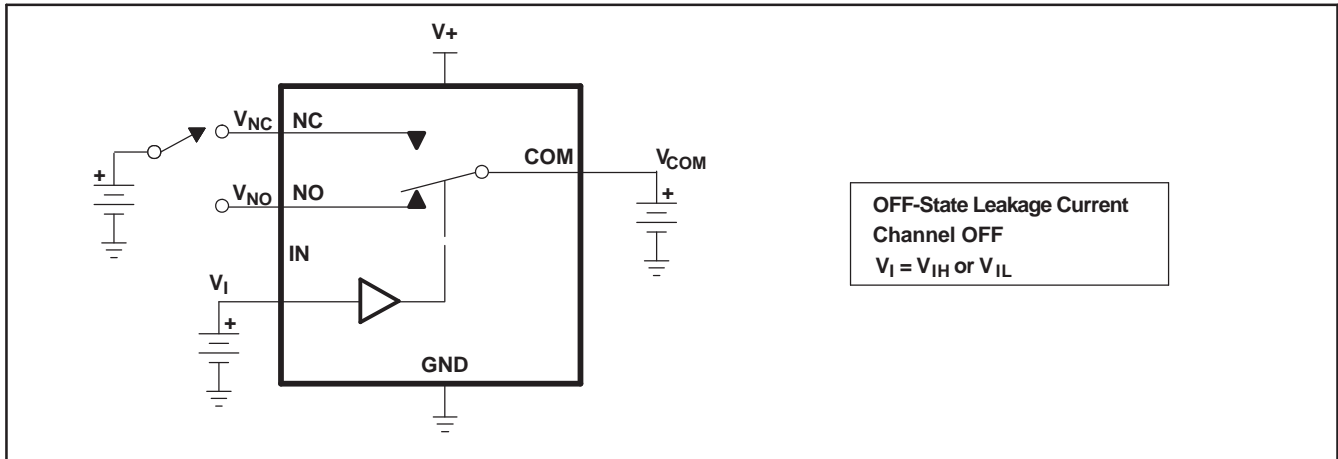
Figure 17. OFF-State Leakage Current
($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

OFF-State Leakage Current
Channel OFF
$V_I = V_{IH} \text{ or } V_{IL}$

PARAMETER MEASUREMENT INFORMATION (continued)
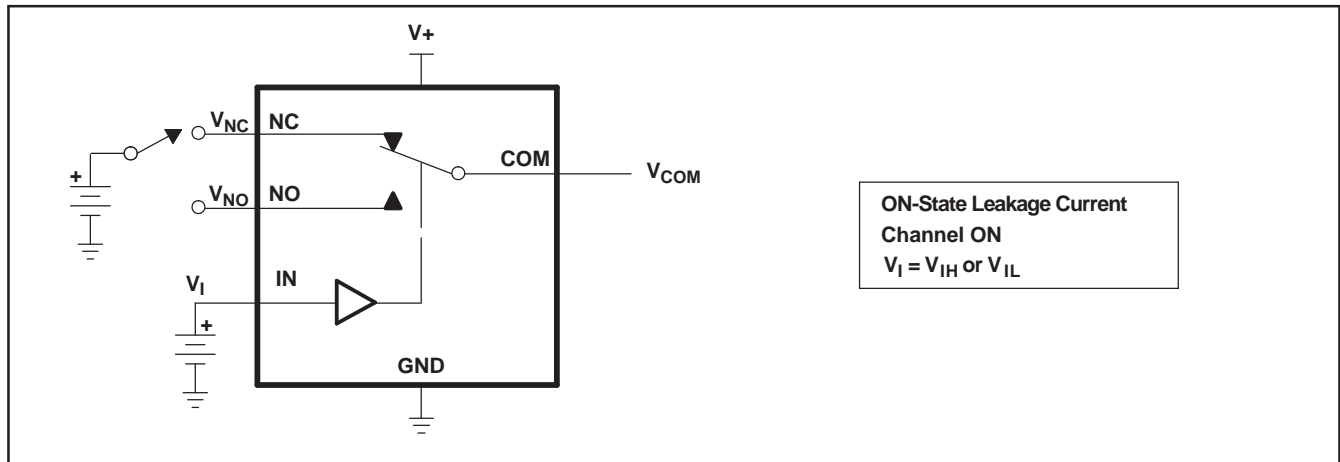
Figure 18. ON-State Leakage Current
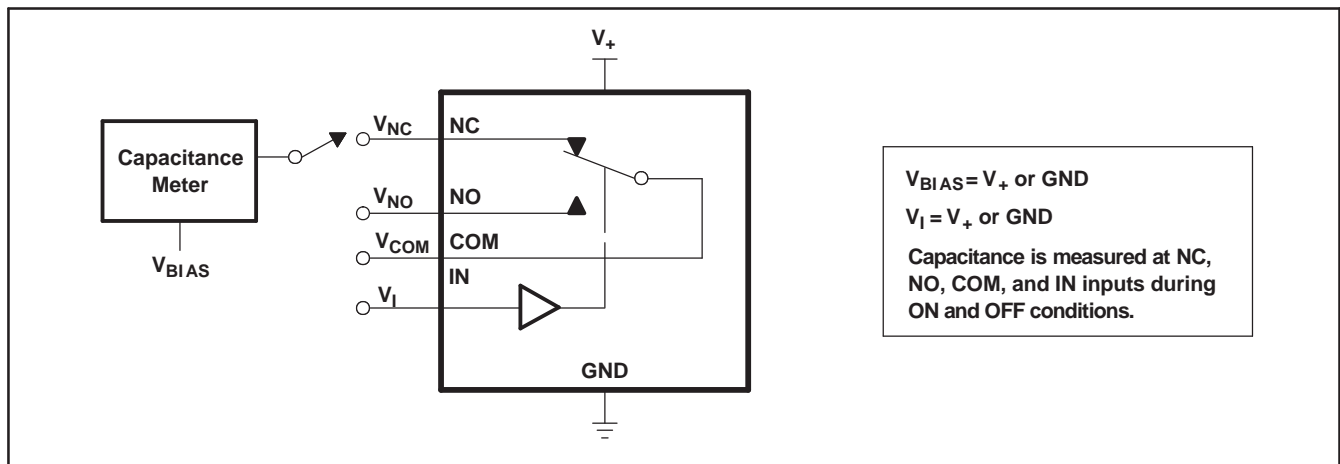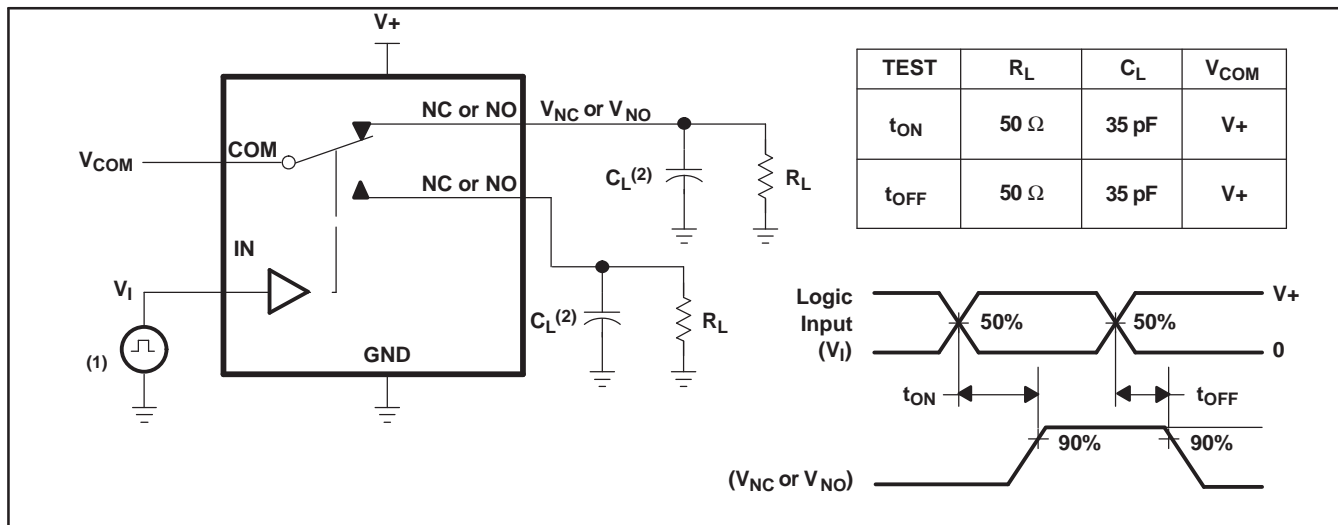**($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)**

Figure 19. Capacitance
(C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Product Folder Link(s): *TS3A44159*

PARAMETER MEASUREMENT INFORMATION (continued)

TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V+
t_{OFF}	50 Ω	35 pF	V+

A.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 20. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

V_{NC} or V_{NO} = V+
R_L = 50 Ω
C_L = 35 pF
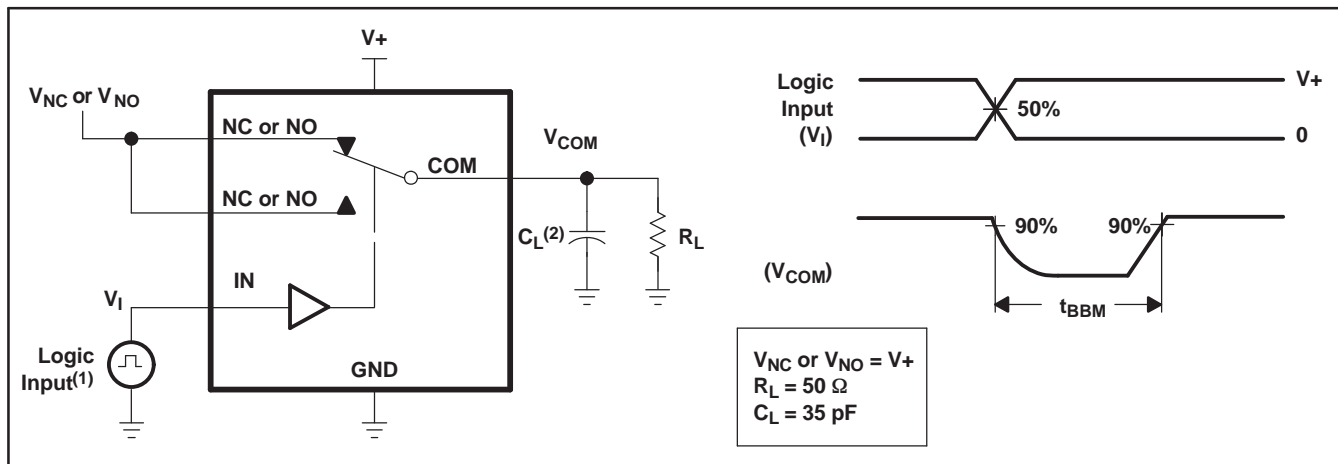
A. C_L includes probe and jig capacitance.

B.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 21. Break-Before-Make Time (t_{BBM})

Product Folder Link(s): *TS3A44159*
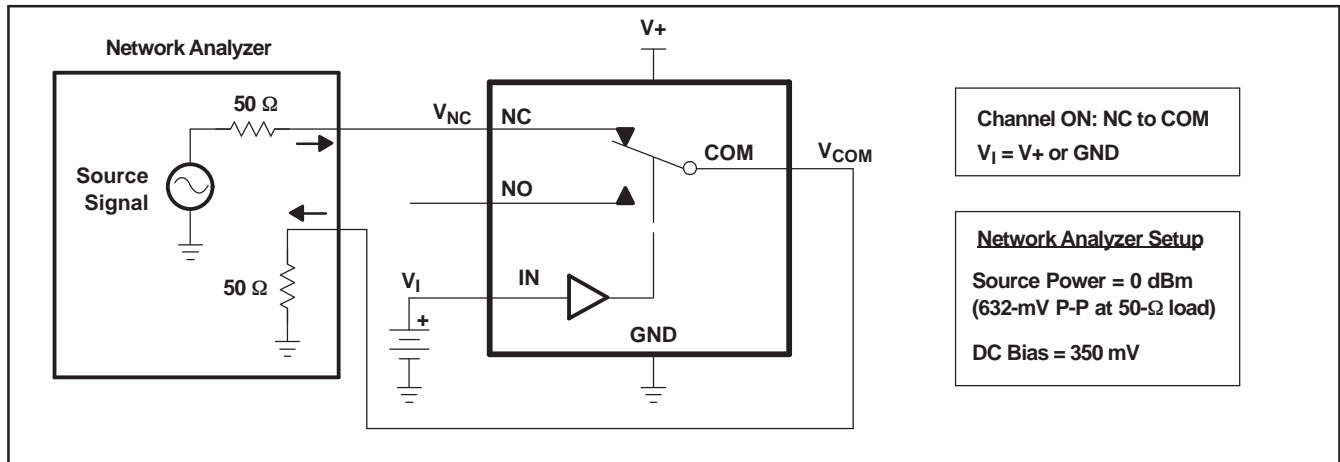
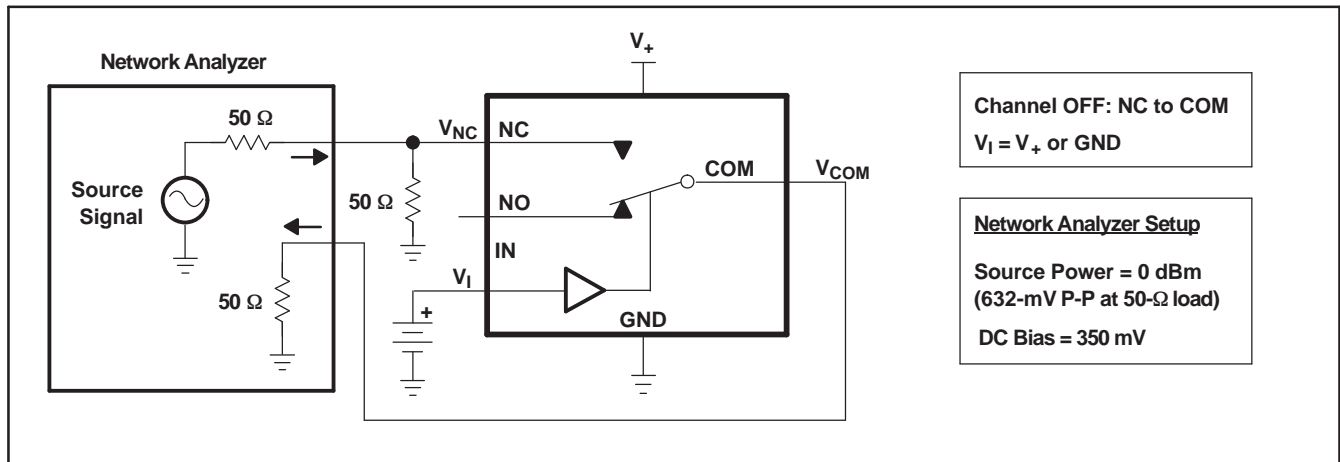## PARAMETER MEASUREMENT INFORMATION (continued)

Figure 22. Bandwidth (BW)

Figure 23. OFF Isolation (O$_{ISO}$)

Figure 24. Crosstalk (X$_{TALK}$)

Product Folder Link(s): *TS3A44159*

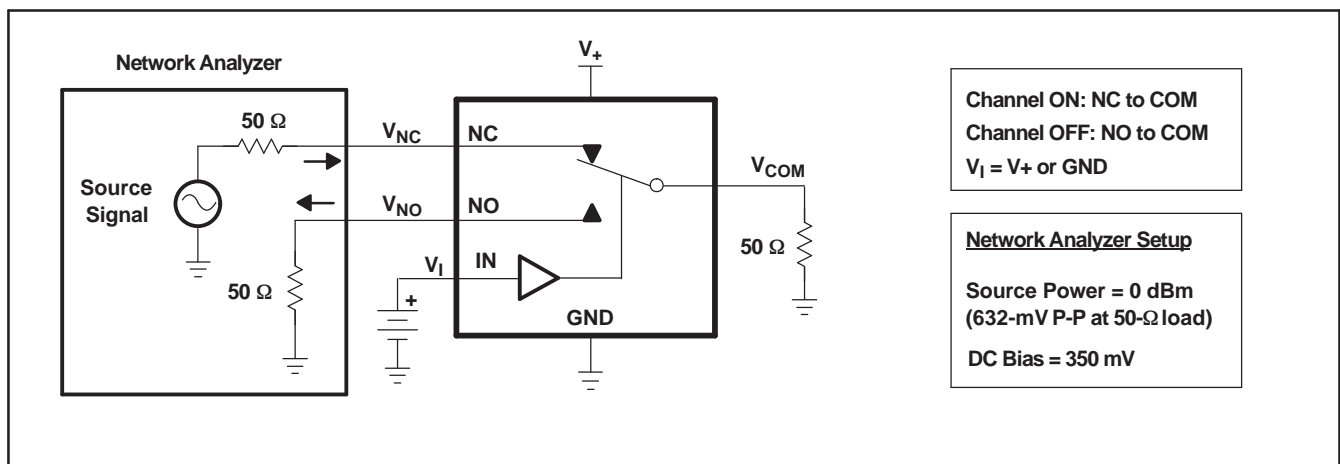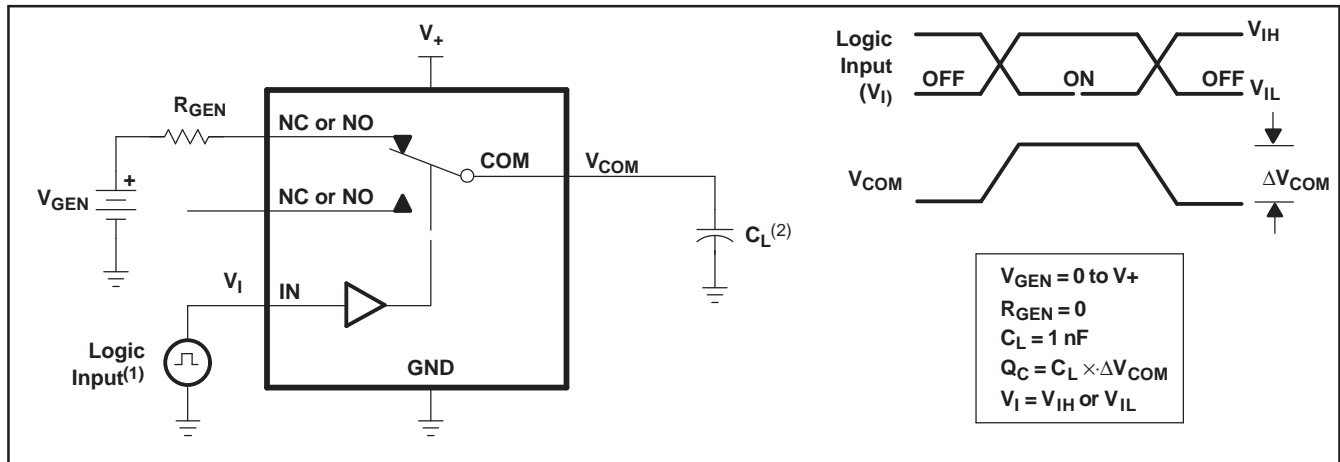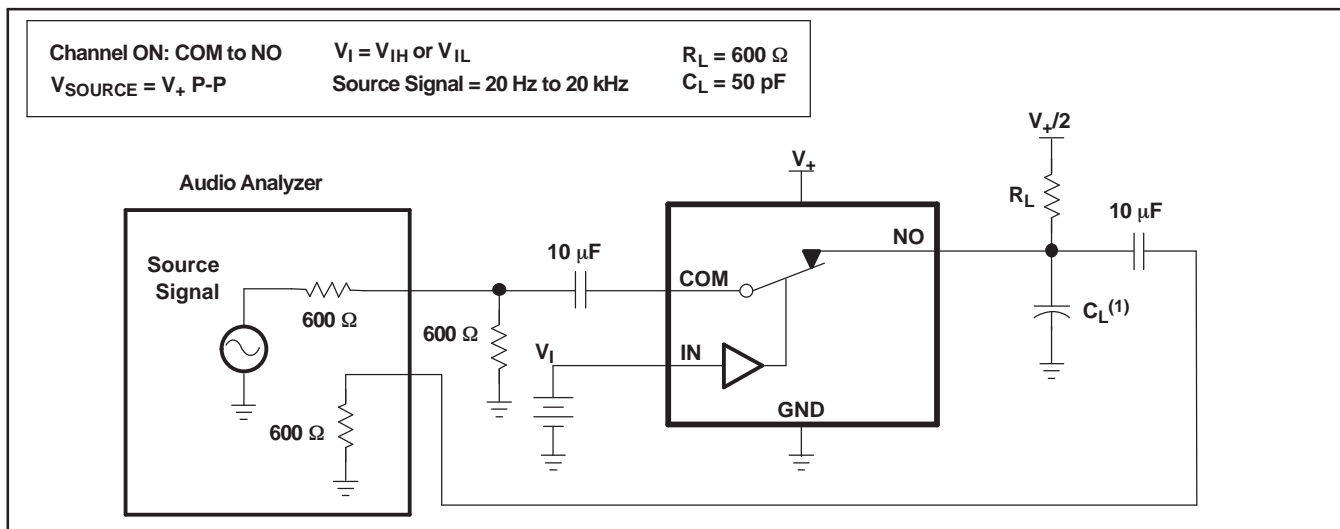## PARAMETER MEASUREMENT INFORMATION (continued)

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

B. C_L includes probe and jig capacitance.

Figure 25. Charge Injection (Q_C)

A. C_L includes probe and jig capacitance.

Figure 26. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TS3A44159PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TS3A44159PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TS3A44159RGTR	ACTIVE	QFN	RGT	16	3000	TBD	Call TI	Call TI	Request Free Samples
TS3A44159RGTRG4	ACTIVE	QFN	RGT	16	3000	TBD	Call TI	Call TI	Request Free Samples
TS3A44159RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TS3A44159RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

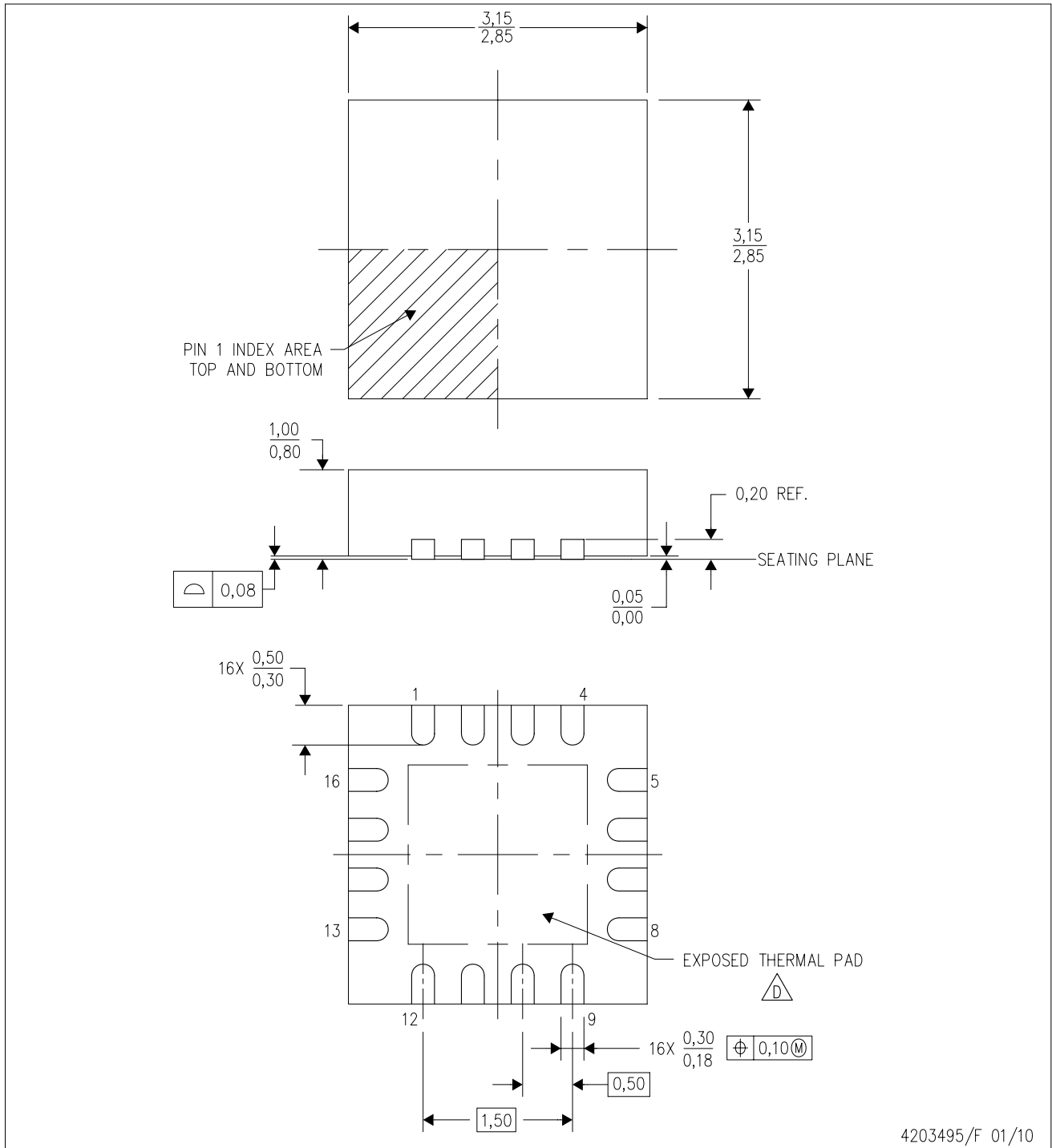| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A44159PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A44159RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A44159PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TS3A44159RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{3,15}{2,85}$

$\frac{3,15}{2,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

⌐ 0,08

$\frac{0,05}{0,00}$

16X $\frac{0,50}{0,30}$

1   4

16   5

13   8

EXPOSED THERMAL PAD

/D\

12   9

16X $\frac{0,30}{0,18}$ ⊕ 0,10 Ⓜ

0,50

1,50

4203495/F 01/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Quad Flatpack, No−leads (QFN) package configuration.
    /D\ The package thermal pad must be soldered to the board for thermal and mechanical performance.
         See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
        E. Falls within JEDEC MO−220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

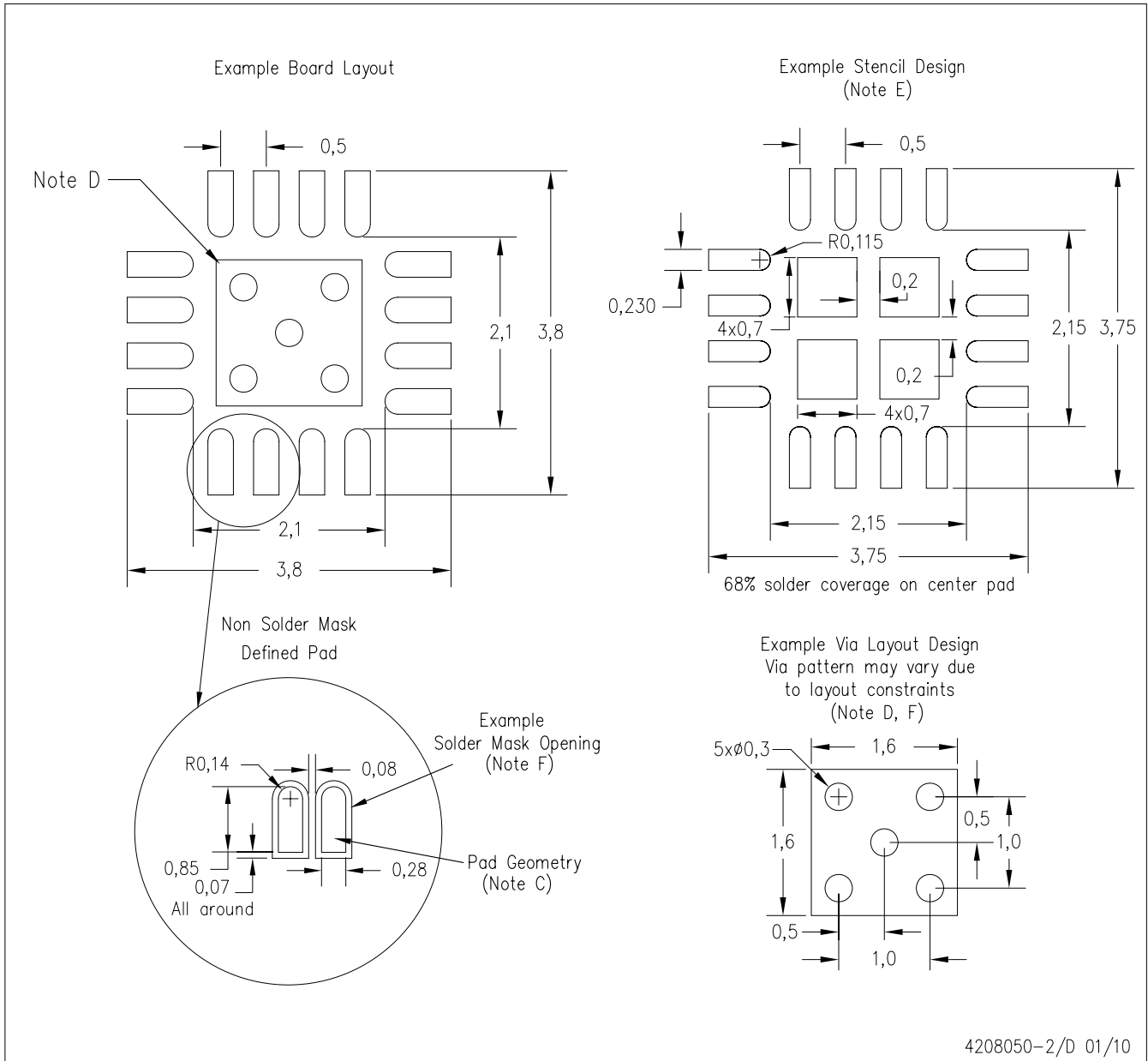The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

1,60 ±0,10

1,60±0,10
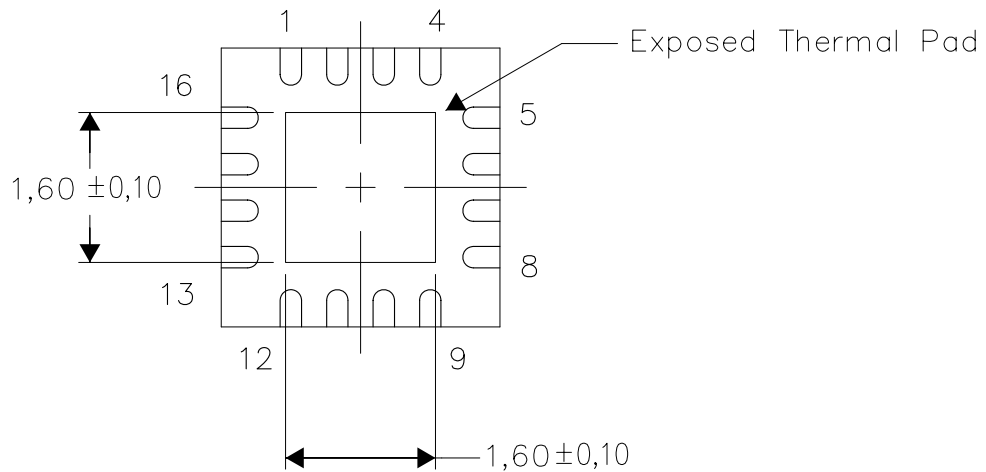
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206349−3/M 12/09

RGT (S−PVQFN−N16)

Example Board Layout

Note D

0,5

2,1   3,8

2,1

3,8

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

R0,14   0,08

0,85

0,07   0,28
All around

Pad Geometry
(Note C)

Example Stencil Design
(Note E)

0,5

0,230

R0,115

4x0,7   0,2

0,2

4x0,7

2,15 3,75

2,15

3,75

68% solder coverage on center pad

Example Via Layout Design
Via pattern may vary due
to layout constraints
(Note D, F)

5xØ0,3   1,6

1,6   0,5

1,0

0,5   1,0

4208050−2/D 01/10
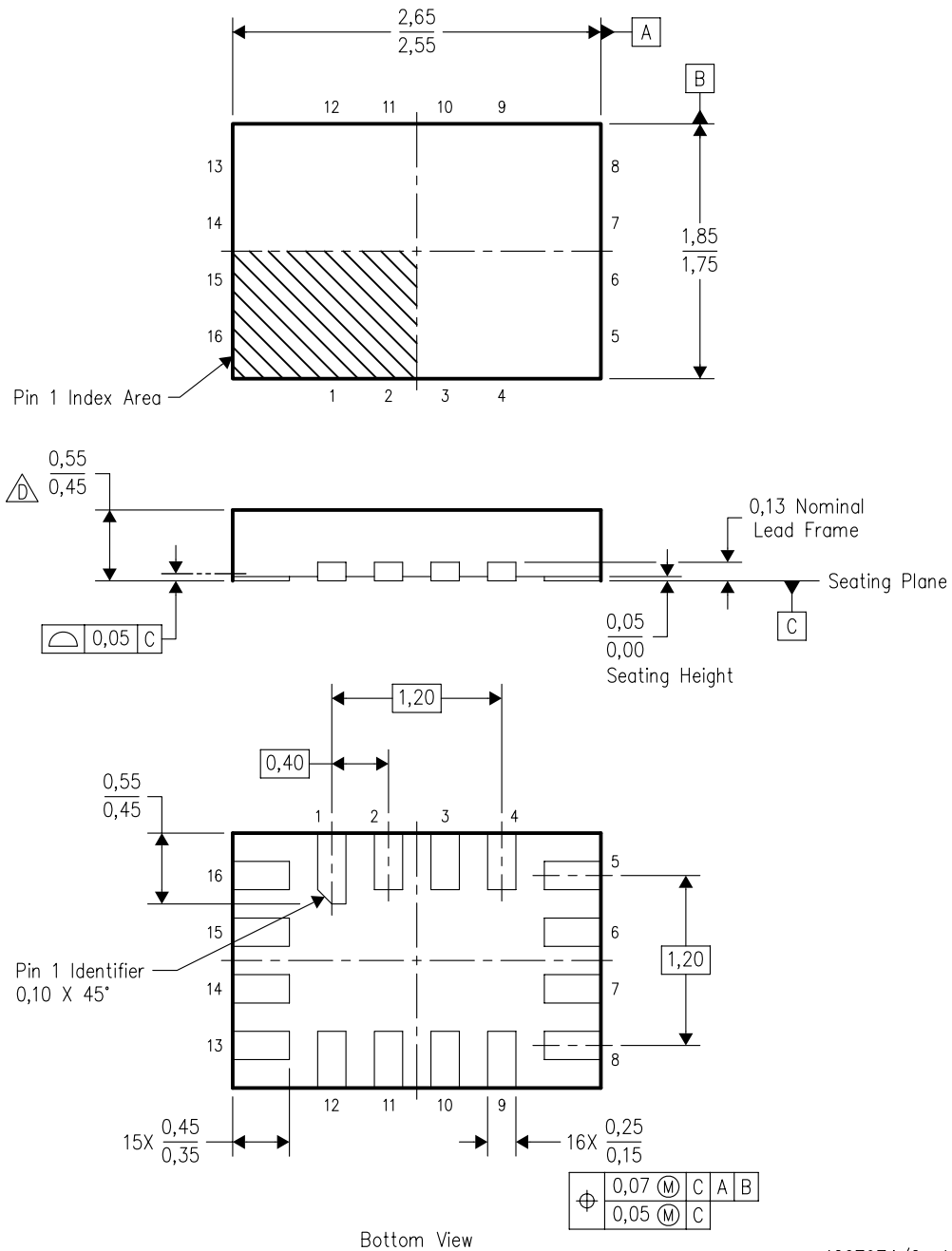
NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
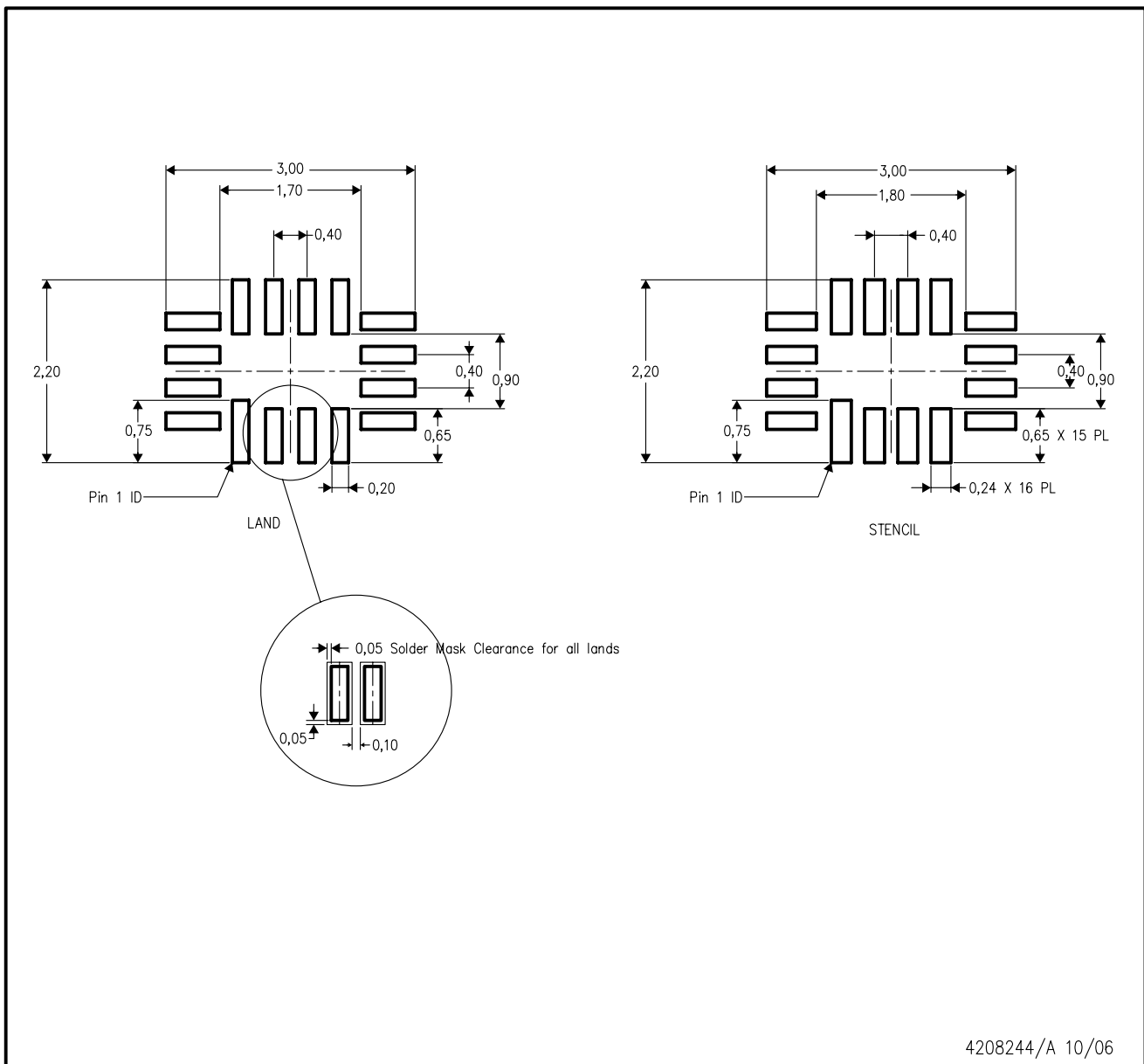
RSV (R–PQFP–N16) **PLASTIC QUAD FLATPACK**

2,65 / 2,55 [A]

[B]

1,85 / 1,75

Pin 1 Index Area

0,55 / 0,45 [D]

0,13 Nominal Lead Frame

Seating Plane

[C]

0,05 / 0,00 Seating Height

0,05 C

1,20

0,40

0,55 / 0,45

Pin 1 Identifier
0,10 X 45°

1,20

15X 0,45 / 0,35

16X 0,25 / 0,15

⊕ 0,07 M C A B
0,05 M C

Bottom View

4207974/C 10/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R−PQFP−N16)

LAND

3,00
1,70
0,40
2,20
0,40 0,90
0,75
0,65
Pin 1 ID
0,20

STENCIL

3,00
1,80
0,40
2,20
0,40 0,90
0,75
0,65 X 15 PL
Pin 1 ID
0,24 X 16 PL

0,05 Solder Mask Clearance for all lands
0,05
0,10

4208244/A 10/06

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
        E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
            if stencil manufacturing process allows for sufficient release at smaller opening.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps