ACE24C32/64
Two-wire Serial EEPROM

Description

The ACE24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

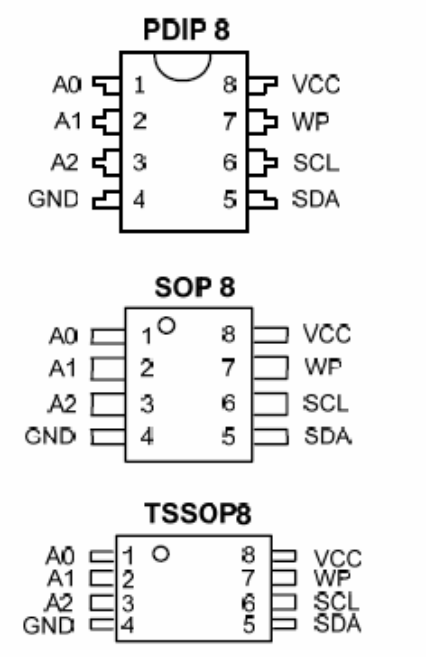
- Low Operation Voltage: Vcc = 1.7V to 5.5V
- Internally Organized: 4096 x 8,8192 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1MHz (2.5V~5.5V) and 400 kHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-byte Page Write Modes (Partial Page Writes are Allowed)
- Self-timed Write Cycle (5 ms max)
- High-reliability - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- PDIP-8,SOP-8,TSSOP-8 ROHS compliant Packages
- Wafer Sales: available in inked wafer Form

Absolute Maximum Ratings

Operating Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type



Pin Configurations

Pin Name	Function
A0~A2	Device Address Inputs
SDA	Serial Data Input / Output
SCL	Serial Clock Input
WP	Write Protect
VCC	Power Supply
GND	Ground

Block Diagram

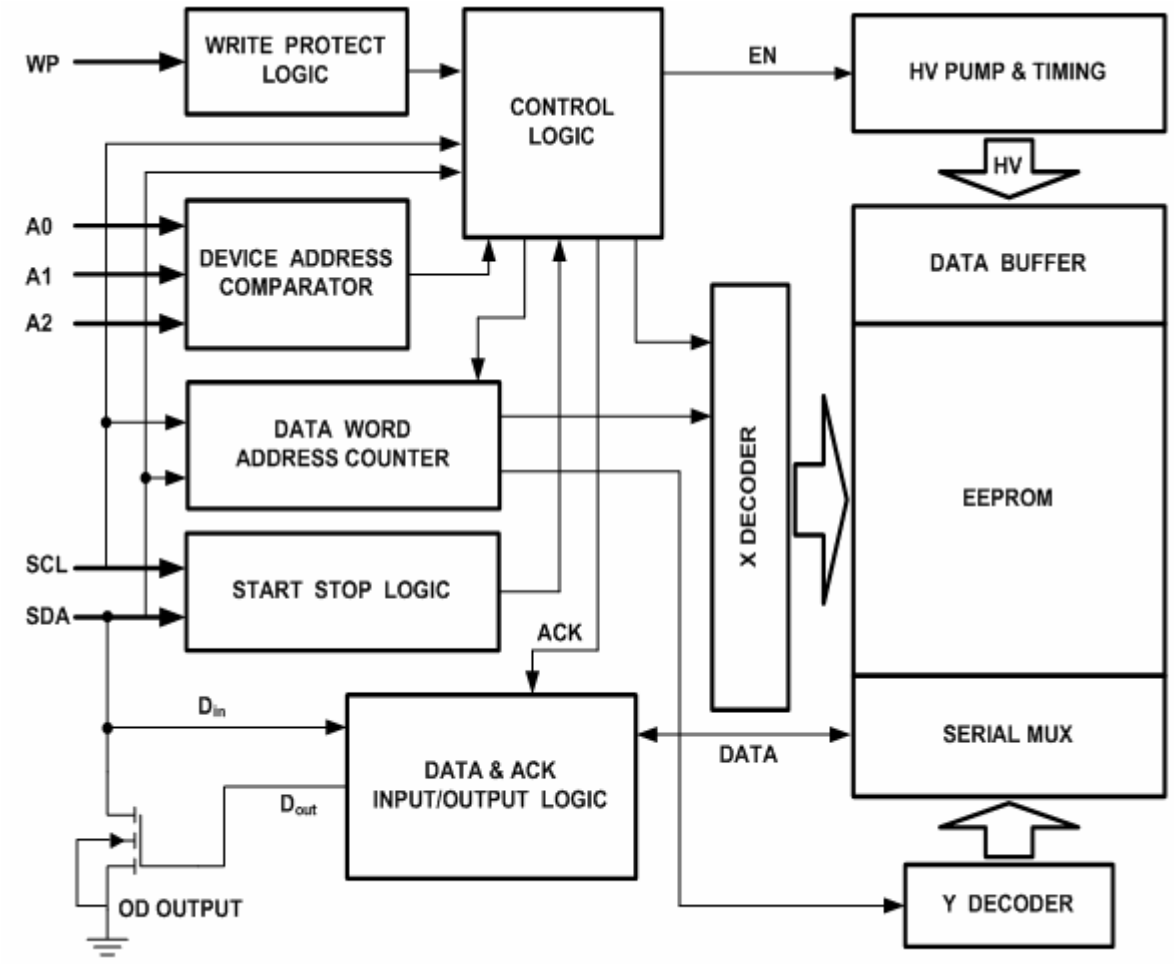
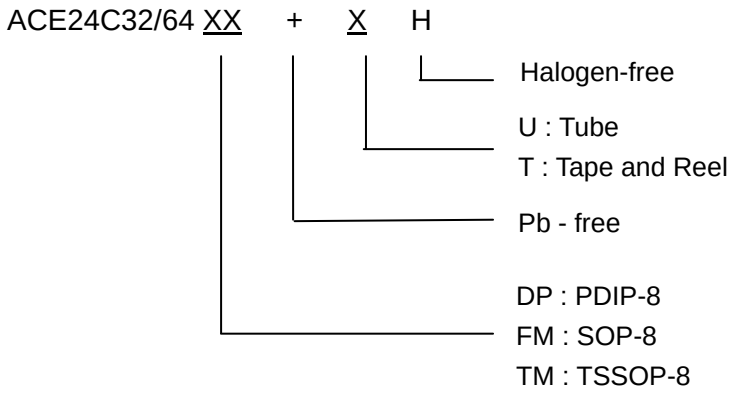


Figure 1

Ordering information

Selection Guide



Serial Clock (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA):

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device/Page Addresses (A2, A1, A0):

The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other ACE24CXX/ACE24CXX devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is < 3pF, if coupling is > 3pF recommends connecting the address pins to GND.

Write Protect (WP):

The ACE24C32/64 has a Write Provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to Vcc. All write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled is < 3pF , if coupling is > 3pF, recommends connecting the pins to GND. Switching WP to Vcc prior to a write operation creates a software write protected function.

Write Protect Description

WP Pin Status	Part of the Array Protected	
	ACE24C32	ACE24C64
WP=V_{CC}	Full (32K) Memory	Full (64K) Memory
WP=GND	Normal Read/Write Operations	

Memory Organization

ACE24C32, 32K Serial EEPROM:

Internally organized with 128 pages of 32 bytes each, the 32K requires a 12-bit data word address for random word addressing.

ACE24C64, 64K Serial EEPROM:

Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

Pin Capacitance(1)

Applicable over recommended operating range from: T_A = 25℃, f = 1.0 MHz, V_{CC} = +1.7V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$[1]	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5V, Read at 400KHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5V, Write at 400KHz		2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC}/ V_{SS}			1.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.5V, V_{IN} = V_{CC}/ V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/ V_{SS}		0.05	3.0	µA
V_{IL}[1]	Input Low Level		-0.6		V_{CC}x0.3	V
V_{IH}[1]	Input High Level		V_{CC}x0.7		V_{CC}+0.5	V
V_{OL2}	Output Low Level 2	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level 1	V_{CC} = 1.7V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from:

T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7-volt		2.5-volt		5.5-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000		1000	kHz
T_{LOW}	Clock Pulse Width Low	1.3		0.45		0.4		μs
T_{HIGH}	Clock Pulse Width High	0.6		0.45		0.4		μs
t_I[1]			100		50		50	
T_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	0.05	0.55	μs
T_{BUF}[1]	Time the bus must be free before a new transmission can Start	1.3		0.5		0.5		μs
$T_{HD.STA}$	Start Hold Time	0.6		0.25		0.25		μs
$T_{SU.STA}$	Start Setup Time	0.6		0.25		0.25		μs
$T_{HD.DAT}$	Data In Hold Time	0		0		0		μs
$T_{SU.DAT}$	Data In Setup Time	100		100		100		ns
T_R	Inputs Rise Time		0.3		0.3		0.3	μs
T_F	Inputs Fall Time		300		100		100	ns
$T_{SU.STO}$	Stop Setup Time	0.6		0.25		0.25		μs
T_{DH}	Data Out Hold Time	50		50		50		ns
T_{WR}	Write Cycle Time		5		5		5	ms
Endurance (1)	3.6V, 25℃, Page Mode	1,000,000						Write Cycles

Notes:1. This parameter is characterized and not 100% tested.

2.AC measurement conditions:

RL (connects to Vcc): 1.3kΩ

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: ≦50 ns

Input and output timing reference voltages: 0.5Vcc

Device Operation

Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

Stop Condition:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

Acknowledge:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Standby Mode :

The ACE24C32/64 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory Reset :

After an interruption in protocol power loss or system reset, any two-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition as SDA is high.

Bus Timing

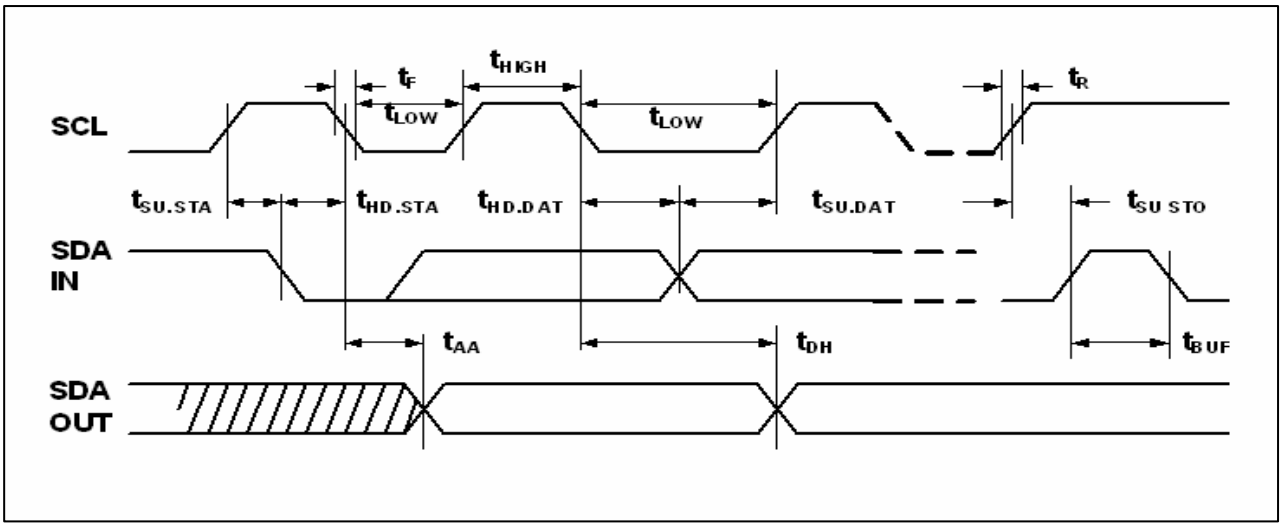


Figure 2 · SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

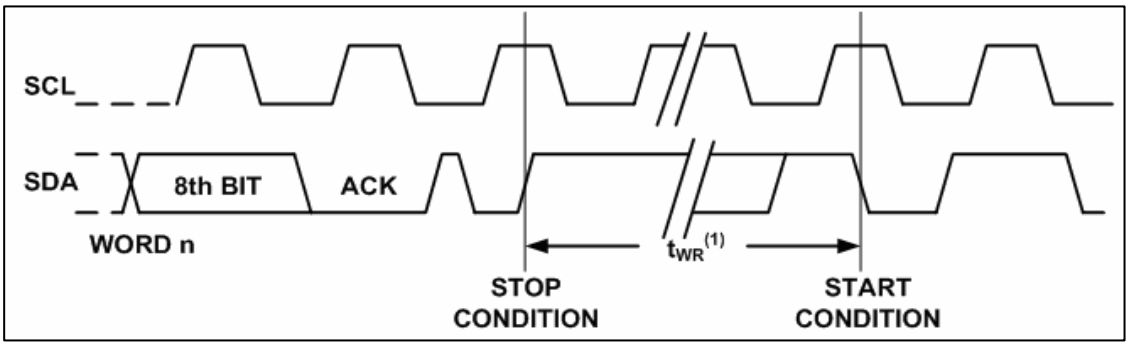


Figure 3. SCL: Serial Clock, SDA: Serial Data I/O

Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

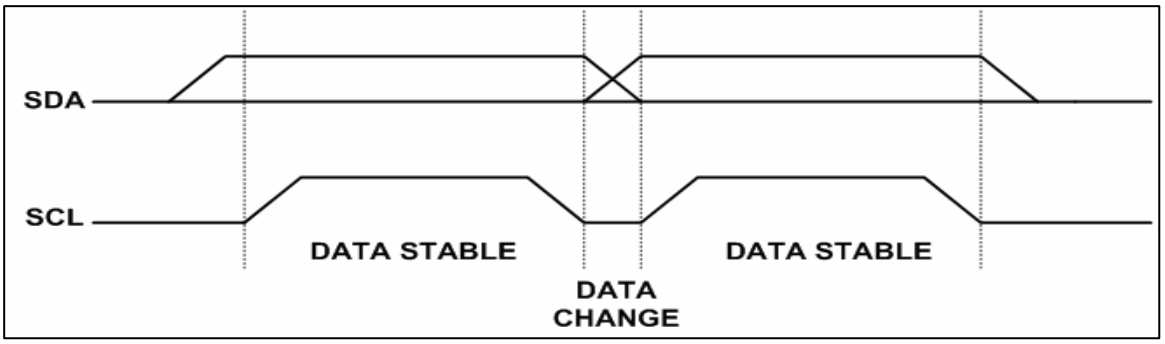


Figure 4 · Data Validity

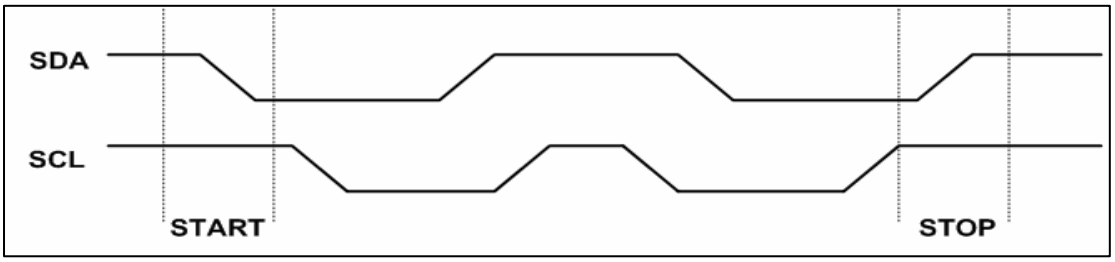


Figure 5 · Start and Stop Definition

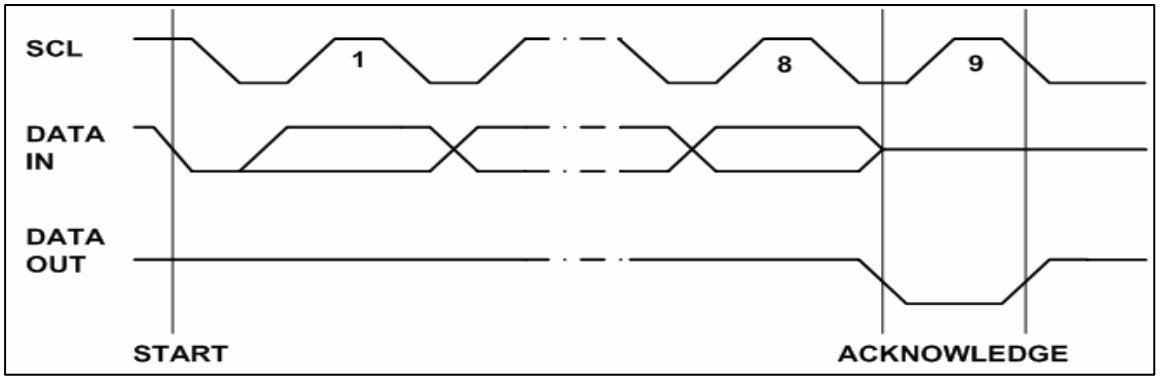


Figure 6 · Output Acknowledge

Device Addressing

The 32K, 64K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 7).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The 32/64K EEPROM use the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard-wired input pins. The A2,A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eight bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

Noise protection:

Special internal circuitry place on the SDA and SCL pins prevent small noise spikes from activating the device.

Date Security:

The ACE24C32/64 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at Vcc.

Write Operations

Byte Write:

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 8).

Page Write:

The 32K/64K EEPROM is capable of an 32-byte page write.A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 9).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

Acknowledge Polling:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

Current Address Read:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 10).

Random Read:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

Sequential Read:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit (64K) is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 12).

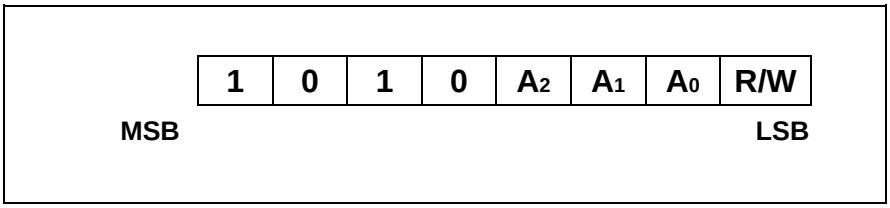


Figure 7 · Device Address

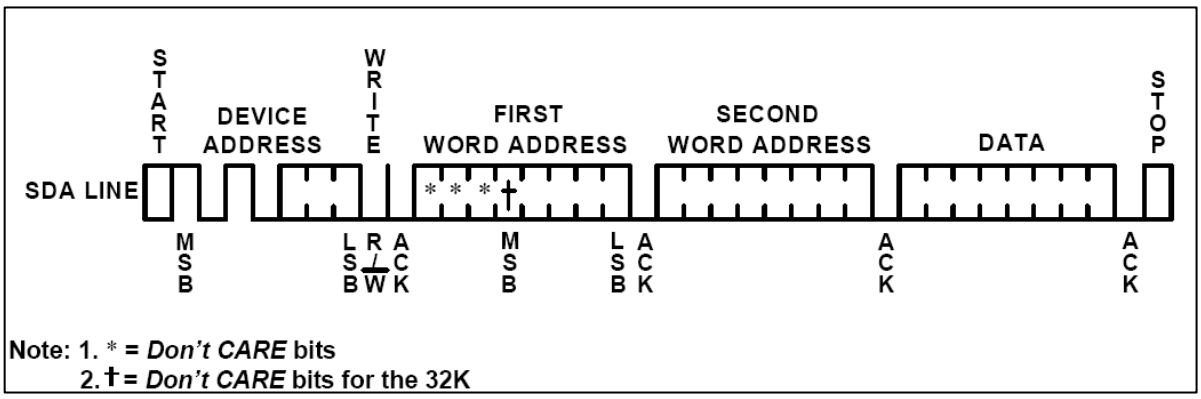


Figure 8 · Byte Write

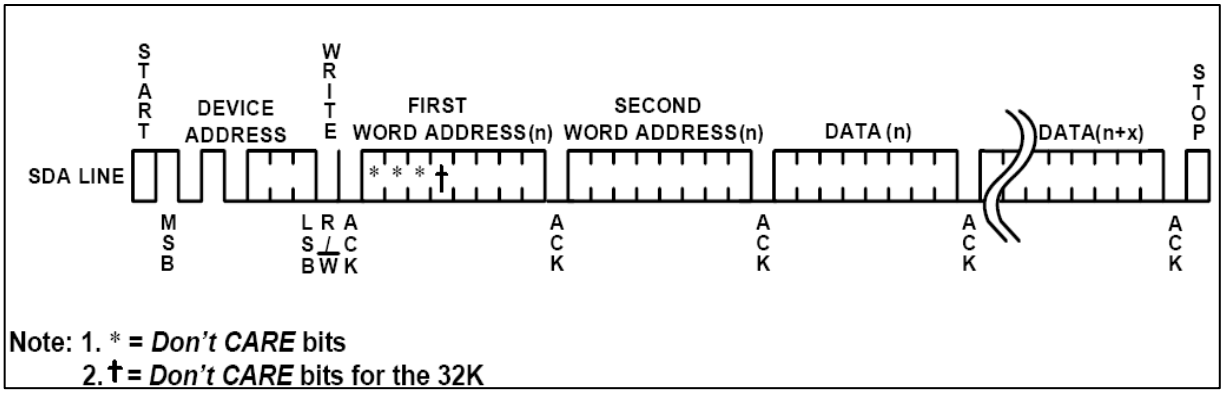


Figure 9 · Page Write

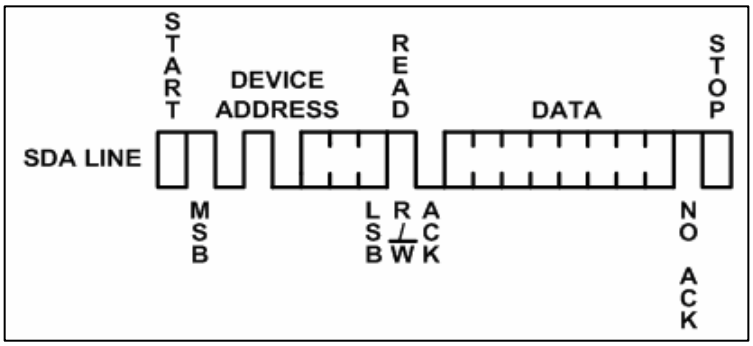


Figure 10 · Current Address Read

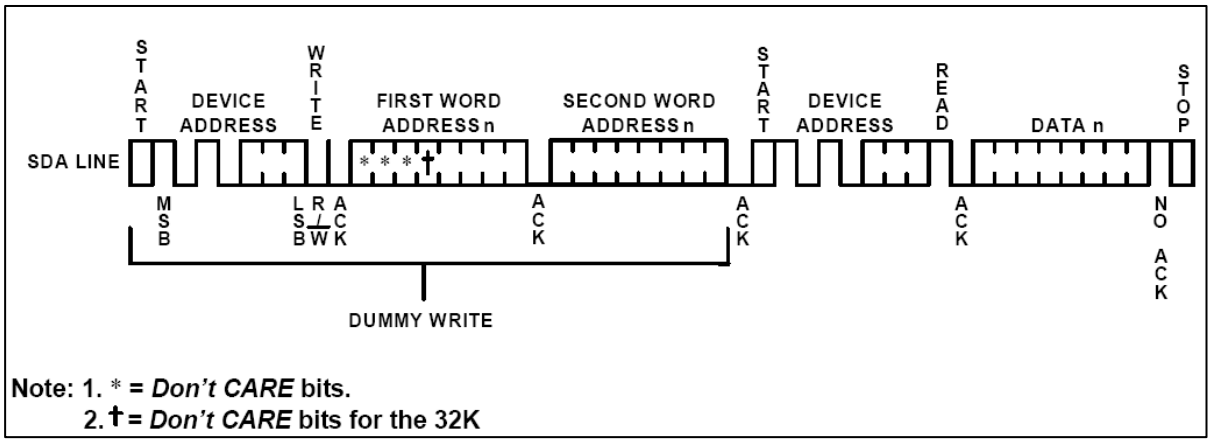


Figure 11 · Random Read

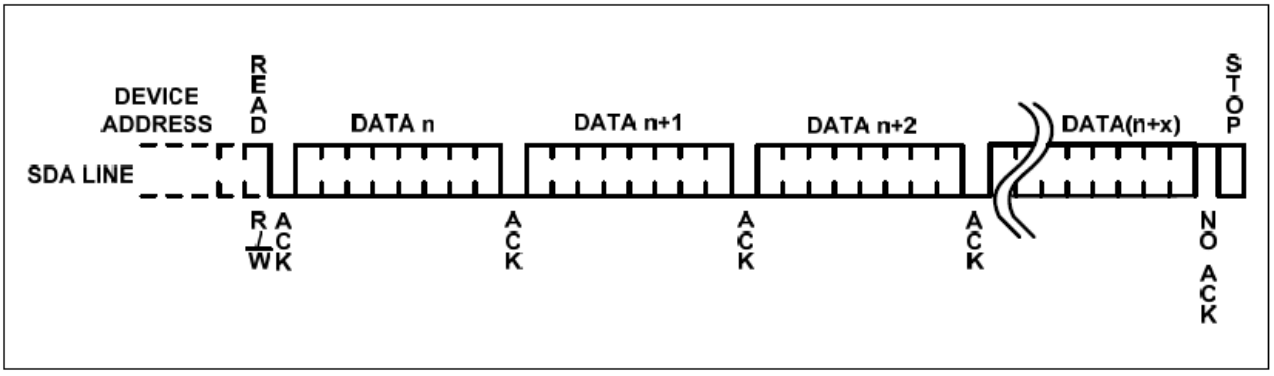
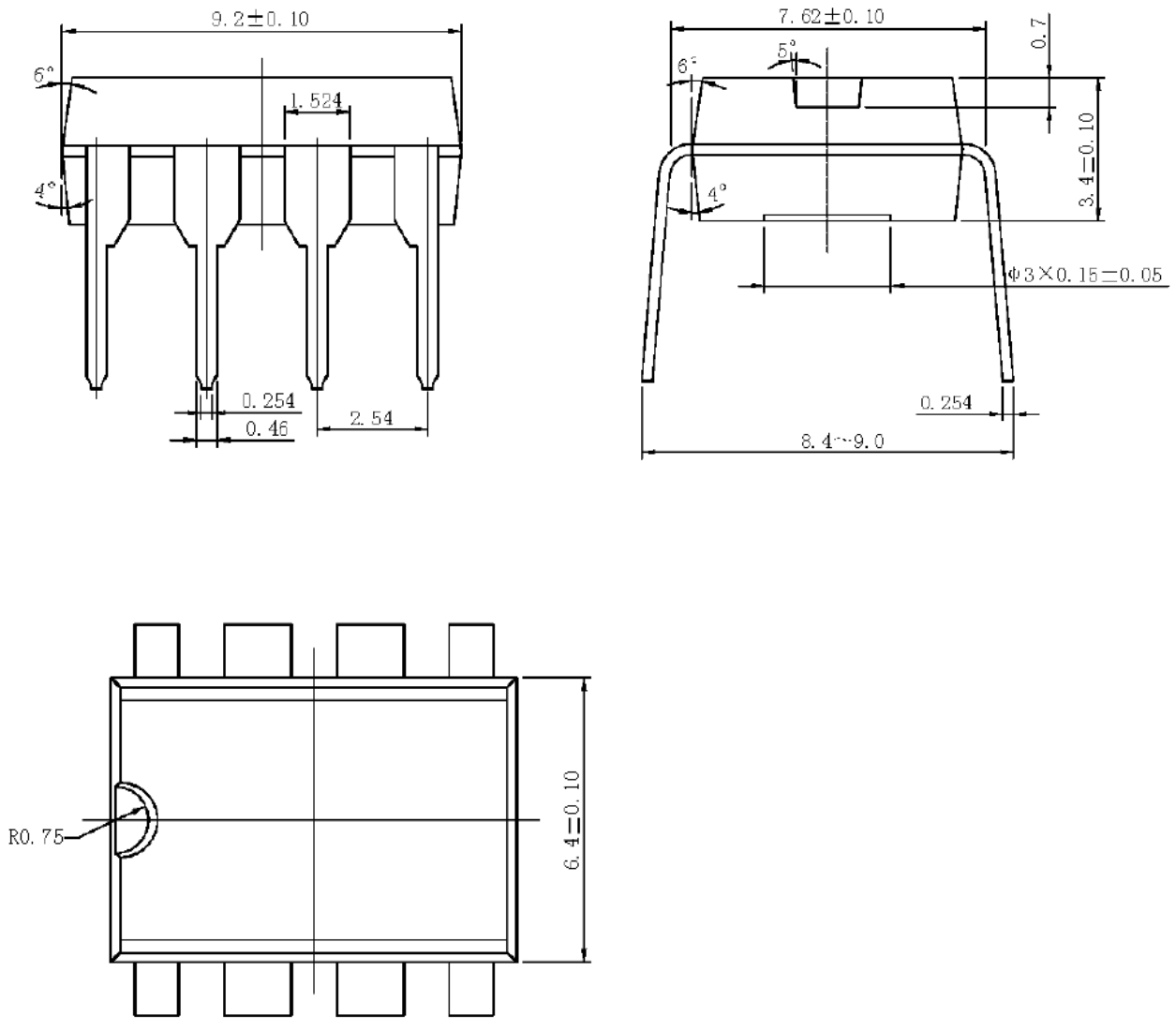


Figure 12 · Sequential Read

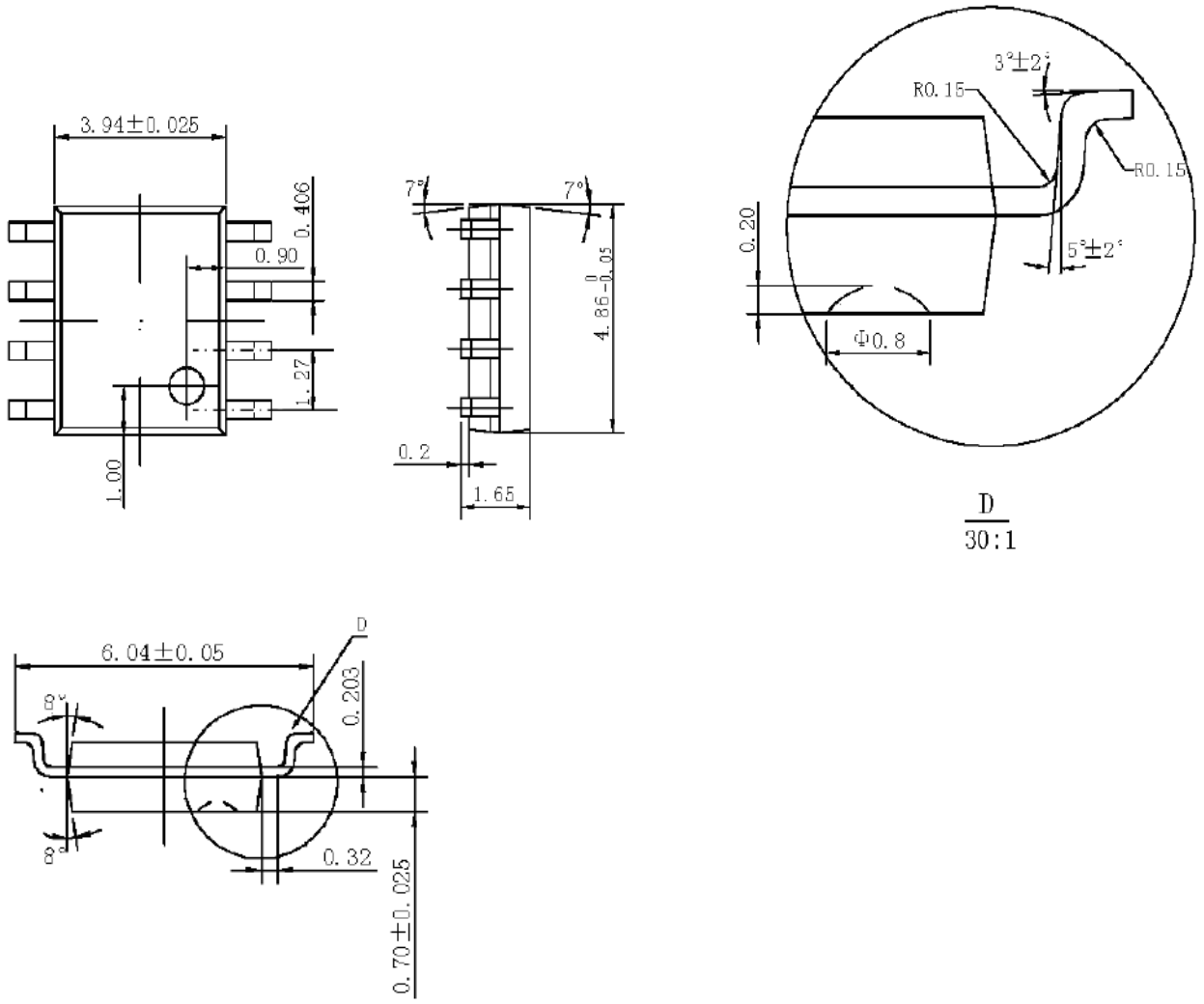
Packaging information

PDIP-8



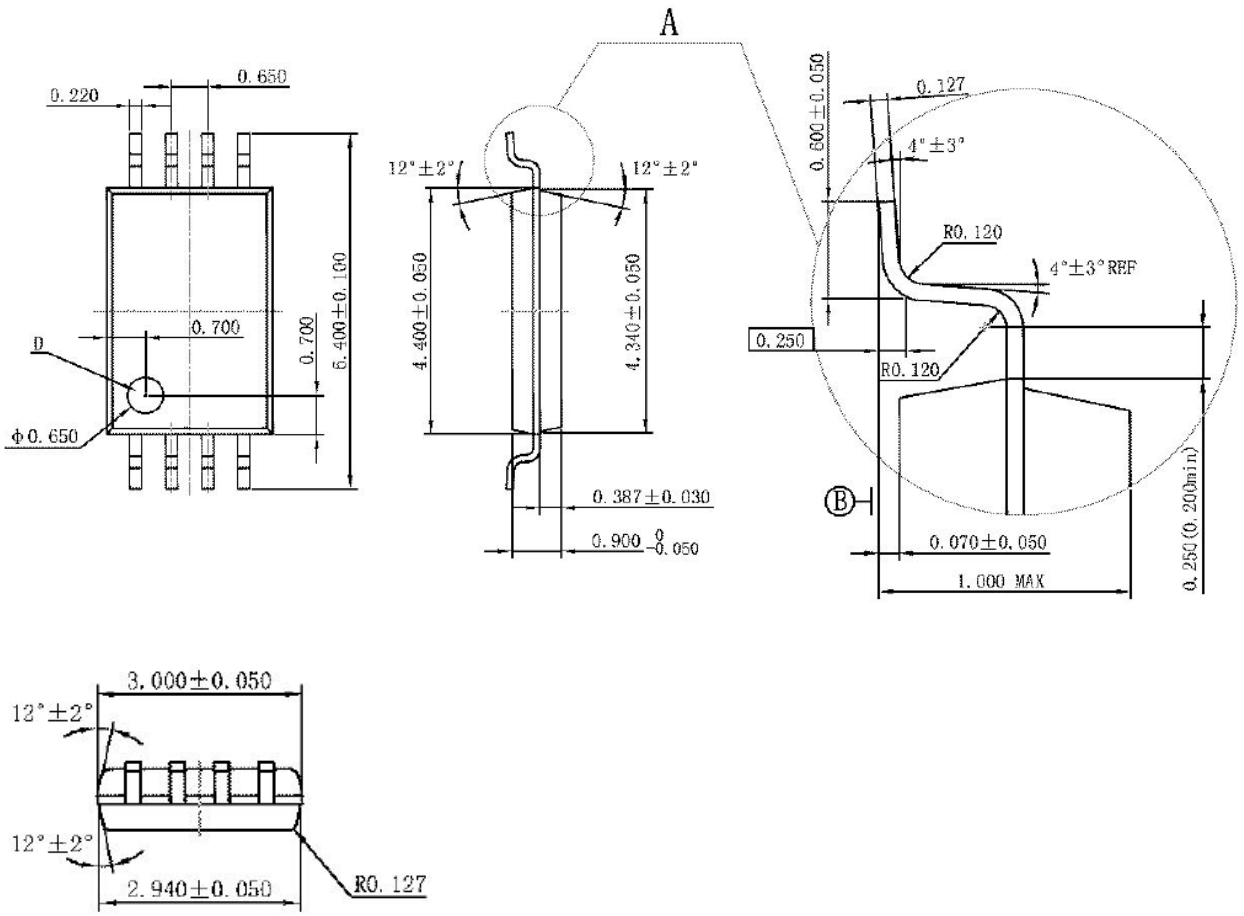
Note: Dimensions in Millimeters.

SOP-8



Note: Dimensions in Millimeters.

TSSOP-8



Note: Dimensions in Millimeters.

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ACE Technology Co., LTD.
http://www.ace-ele.com/