Intel® 41210 Serial to Parallel PCI Bridge

Datasheet

Product Features

- *PCI Express Specification*, Revision 1.0a
- Support for single x8, single x4 or single x1 PCI Express operation.
- 64-bit addressing support
- 32-bit CRC (cyclic redundancy checking) covering all transmitted data packets.
- 16-bit CRC on all link message information.
- Raw bit-rate on the data pins of 2.5 Gbit/s, resulting in a raw bandwidth per pin of 250 MB/s.
- Maximum realized bandwidth on PCI Express interface is 2 GB/s (in x8 mode) in each direction simultaneously, for an aggregate of 4 GB/s.
- *PCI Local Bus Specification*, Revision 2.3.
- *PCI-to-PCI Bridge Specification*, Revision 1.1.
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b
- 64-bit 66 MHz, 3.3 V, NOT 5 V tolerant.
- On Die Termination (ODT) with 8.3KOhm pull-up to 3.3V for PCI signals.
- Six external REQ/GNT Pairs for internal arbiter on segment A and B respectively.
- Programmable bus parking on either the last agent or always on the 41210 Bridge
- 2-level programmable round-robin internal arbiter with Multi-Transaction Timer (MTT)
- External PCI clock-feed support for asynchronous primary and secondary domain operation.
- 64-bit addressing for upstream and downstream transactions
- Downstream LOCK# support.
- No upstream LOCK# support.
- PCI fast Back-to-Back capable as target.
- Up to four active and four pending upstream memory read transactions
- Up to two downstream delayed (memory read, I/O read/write and configuration read/write) transaction.
- Tunable inbound read prefetch algorithm for PCI MRM/MRL commands
- Device hiding support for secondary PCI devices.
- Secondary bus Private Memory support via Opaque memory region
- Local initialization via SMBus
- Secondary side initialization via Type 0 configuration cycles.
- Full peer-to-peer read/write capability between the two secondary PCI segments.

Order Number: 278875-005US
May 2005

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Revision History

Date	Revision	Description
May 2005	005	Revised Table 1, Table 9, and Section 3.8
April 2005	004	Revised Table 26 “PCI and PCI-X Clock Timings” on page 33 CLK Cycle Time parameters
September 2004	003	Revised first page PCI Express operation description; updated information in Table 2.
June 2004	002	Added Chapter 2. Removed original Sections 3.6 and 3.7. Updated VCC information to VCC15.
September 2003	001	Initial release

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Introduction 1

1.1 About This Document

This document provides information on the Intel® 41210 Serial to Parallel PCI Bridge, including a functional overview, signal descriptions, mechanical data, package signal location and bus functional waveforms.

1.2 Product Overview

The Intel® 41210 Serial to Parallel PCI Bridge (also called the 41210 Bridge) integrates two PCI Express-to-PCI/PCI-X bridges. Each bridge follows the PCI-to-PCI Bridge programming model. The PCI Express port is compatible with the *PCI Express Specification*, Revision 1.0a. The two PCI bus interfaces are compatible with the *PCI Local Bus Specification*, Revision 2.3 and *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b.

Signal Description 2

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name the signal is asserted when at the high voltage level. The following notations are used to describe the signal type:

I: Input pin

O: Output pin

OD: Open-drain Output pin

I/O: Bidirectional Input/Output pin

I/OD: Bidirectional Input/Open-drain Output pin

2.1 On Die Termination (ODT)

The 41210 Bridge incorporates on-die termination for most of the PCI interface signals. This eliminates the need for the system designer to incorporate external pull-up resistors in the design.

The following signals have an on die termination of 8.33KOhm @40%:

Table 1. ODT Signals

A_ACK64#	B_ACK64#
A_AD[63:32]	B_AD[63:32]
A_CBE#[7:4]	B_CBE#[7:4]
A_DEVSEL#	B_DEVSEL#
A_FRAME#	B_FRAME#
A_GNT#[5:0]	B_GNT#[5:0]
A_IRDY#	B_IRDY#
A_PAR	B_PAR
A_PAR64	B_PAR64
A_PERR#	B_PERR#
A_LOCK#	B_LOCK#
A_REQ#[5:0]	B_REQ#[5:0]
A_REQ64#	B_REQ64#
A_SERR#	B_SERR#
A_STOP#	B_STOP#
A_TRDY#	B_TRDY#
A_INTA#	B_INTA#
A_INTB#	B_INTB#
A_INTC#	B_INTC#
A_INTD#	B_INTD#
TCK	
TDI	
TDO	
TMS	

2.2 PCI Express Interface

Table 2. PCI Express Interface Pins

Signal	I/O	Description
REFCLKp/ REFCLKn	I	**PCI Express Reference Clocks**: 100 MHz differential clock pair.
PETp[7:0]/ PETn[7:0]	O	PCI Express **Serial Data Transmit:** PCI Express differential data transmit signals. X8 Mode: All PETp[7:0]/ PETn[7:0] are used X4 Mode: Only PETp[3:0]/ PETn[3:0] are used x1 Mode: Either PETp[0]/ PETn[0] is used or PETp[7]/ PETn[7] is used
PERp[7:0]/ PERn[7:0]	I	PCI Express **Serial Data Receive:** PCI Express differential data receive signals. X8 Mode: All PERp[7:0]/ PERn[7:0] are used X4 Mode: Only PERp[3:0]/ PERn[3:0] are used x1 Mode: Either PERp[0]/ PERn[0] is used or PERp[7]/ PERn[7] is used
PE_RCOMP[1:0]	I	**PCI Express Compensation Inputs:** Analog signals. Connect to a 24.9Ω±1% pull-up resitor to 1.5V. A single resistor can be used for both signals.
Total	36	

2.3 PCI Bus Interface (Two Instances)

Each interface is marked by either the letter “A” or “B” to signify the interface. Therefore, A_AD refers to the AD bus on PCI bus A, and B_AD refers to the AD bus on PCI bus B. For pin names described in the following sections, an ‘X’ in the name indicates either A or B, for the PCI bus A and PCI bus B sides. For example, X_PAR signal would be called A_PAR on the PCI bus A and B_PAR on the PCI bus B.

Table 3. PCI Interface Pins (Sheet 1 of 2)

Signal	I/O	Description
A_AD[31:0] B_AD[31:0]	I/O	**PCI Address/Data:** These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on X_AD[31:0]. During the data phases of a transaction, the initiator drives write data, or the target drives read data. No External pull-up resistors are required on the system board for these signals.
A_C/BE#[3:0] B_C/BE#[3:0]	I/O	**Bus Command and Byte Enables:** These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on C/BE#[3:0]. When there are two address phases, the first address phase carries the dual address command and the second address phase carries the transaction type. For both read and write transactions, the initiator drives byte enables on C/BE#[3:0] during the data phases. No External pull-up resistors are required on the system board for these signals.
A_PAR B_PAR	I/O	**Parity:** Even parity calculated on 36 bits - AD[31:0] plus C/BE[3:0]#. It is calculated on all 36 bits regardless of the valid byte enables. It is generated for address and data phases. It is driven identically to the AD[31:0] lines, except it is delayed by exactly one PCI clock. It is an output during the address phase for all 41210 Bridge initiated transactions and all data phases when the 41210 Bridge is the initiator of a PCI write transaction, and when it is the target of a read transaction. 41210 Bridge checks parity when it is the initiator of PCI read transactions and when it is the target of PCI write transactions. No External pull-up resistors are required on the system board for these signals.
A_DEVSEL# B_DEVSEL#	I/O	**Device Select:** The bridge asserts DEVSEL# to claim a PCI transaction. As a target, the 41210 Bridge asserts DEVSEL# when a PCI master peripheral attempts an access an address destined for PCI Express. As an initiator, DEVSEL# indicates the response to a 41210 Bridge initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the 41210 Bridge until driven as a target. No External pull-up resistors are required on the system board for these signals.
A_FRAME# B_FRAME#	I/O	**Frame:** FRAME# is driven by the Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. No External pull-up resistors are required on the system board for these signals.
A_IRDY# B_IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ability of the initiator to complete the current data phase of the transaction. A data phase is completed when both IRDY# and TRDY# are sampled asserted. No External pull-up resistors are required on the system board for these signals.
A_TRDY# B_TRDY#	I/O	**Target Ready:** Indicates the ability of the target to complete the current data phase of the transaction. A data phase is completed when both TRDY# and IRDY# are sampled asserted. TRDY# is tri-stated from the leading edge of RST#. TRDY# remains tri-stated by the 41210 Bridge until driven as a target. No External pull-up resistors are required on the system board for these signals.
A_STOP# B_STOP#	I/O	**Stop:** Indicates that the target is requesting an initiator to stop the current transaction. No External pull-up resistors are required on the system board for these signals.
A_PERR# B_PERR#	I/O	**Parity Error:** Driven by an external PCI device when it receives data that has a parity error. Driven by 41210 Bridge when, as a initiator it detects a parity error during a read transaction and as a target during write transactions. No External pull-up resistors are required on the system board for these signals.
A_SERR# B_SERR#	I	**System Error:** The 41210 Bridge samples SERR# as an input and conditionally forwards it to the PCI Express. No External pull-up resistors are required on the system board for these signals.
A_M66EN B_M66EN	I/OD	**66 MHz Enable:** This input signal from the PCI Bus indicates the speed of the PCI Bus. If it is high then the Bus speed is 66 MHz and if it is low then the bus speed is 33 MHz. This signal will be used to generate appropriate clock (33 or 66 MHz) on the PCI Bus. Use an approximately 8.2KΩ resistor to pull to VCC33 or pull-down to ground.

Table 3. PCI Interface Pins (Sheet 2 of 2)

Signal	I/O	Description
A_PCIXCAP B_PCIXCAP	I	**PCI-X Capable:** Indicates whether all devices on the PCI bus are PCI-X devices, so that the 41210 Bridge can switch into PCI-X mode. Use an approximately 8.2KΩ resistor to pull to VCC33.
A_LOCK# B_LOCK#	O	**PCI Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. This signal is an output from the bridge when it is initiating exclusive transactions on PCI. LOCK# is ignored when PCI masters are granted the bus. Locked transaction do not propagate upstream. No External pull-up resistors are required on the system board for these signals.
Total	118	

2.4 PCI Bus Interface 64-Bit Extension (Two Interfaces)

Table 4. PCI Interface Pins: 64-Bit Extensions

Signal	I/O	Description
A_AD[63:32] B_AD[63:32]	I/O	PCI Address/Data: These signals are a multiplexed address and data bus. This bus provides an additional 32 bits to the PCI bus. During the data phases of a transaction, the initiator drives the upper 32 bits of 64-bit write data, or the target drives the upper 32 bits of 64-bit read data, when REQ64# and ACK64# are both asserted.
A_C/BE#[7:4] B_C/BE#[7:4]	I/O	Bus Command and Byte enables upper 4 bits: These signals are a multiplexed command field and byte enable field. For both reads and write transactions, the initiator will drive byte enables for the AD[63:32] data bits on C/BE7:4] during the data phases when REQ64# and ACK64# are both asserted.
A_PAR64 B_PAR64	I/O	PCI interface upper 32 bits parity: This carries the even parity of the 36 bits of AD[63:32] and C/BE#[7:4] for both address and data phases.
A_REQ64# B_REQ64#	I/O	PCI interface request 64-bit transfer: This is asserted by the initiator to indicate that the initiator is requesting a 64-bit data transfer. It has the same timing as FRAME#. When the 41210 Bridge is the initiator, this signal is an output. When the 41210 Bridge is the target this signal is an input.
A_ACK64# B_ACK64#	I/O	PCI interface acknowledge 64-bit transfer: This is asserted by the target only when REQ64# is asserted by the initiator, to indicate the target ability to transfer data using 64 bits. It has the same timing as DEVSEL#.
Total	78	

2.5 PCI Bus Interface Clocks and, Reset and Power Management (Two Interfaces)

Table 5. PCI Clock and Reset Pins

Signal	I/O	Description
A_CLKO[6:0] B_CLKO[6:0]	O	**PCI Clock Output:** 33/66/100/133 MHz clock for a PCI device. X_CLK[6] must be connected to the respective X_CLKIN input. for feeding the PCI interface logic. Unused clock outputs may be disabled via the "Offset 43: PCLKC – PCI Clock Control" register and should be treated as no connects on the board. ***Note:*** Registers are listed in the *Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual*.
A_CLKIN B_CLKIN	I	**PCI Clock In:** This signal is PCI clock feedback input. This pin should be connected to the corresponding X_CLKO[6] through a 22Ω±1% series resistor.
A_RST# B_RST#	O	**PCI Reset:** The bridge asserts RST# to reset devices that reside on the secondary PCI bus.
A_PME# B_PME#	I	**PCI Power Management Event:** PCI bus power management event signal. This is a shared open drain input from all the PCI cards on the corresponding PCI bus segment. This is a level sensitive signal that will be converted to a PME event on PCI Express. This pin does not have on-die 8.3K pull-up. This pull-up must be provided externally.
Total	20	

2.6 Interrupt Interface (Two Interfaces)

This section lists the interrupt interface signals. There are two sets of interrupt signals for the standard INTA:INTD pci signals.

Table 6. Interrupt Interface Pins

Signal	I/O	Description
A_INTA# A_INTB# A_INTC# A_INTD# B_INTA# B_INTB# B_INTC# B_INTD#	I	**Interrupt Request Bus:** The interrupt lines from PCI interrupts INTA#:INTD# can be routed to these interrupt lines. Refer to the *Intel® 41210 Serial to Parallel PCI Bridge Design Guide* for more information on device numbering.
Total	8	

2.7 Reset Straps

The following signals are used for static configuration. These signals are all sampled on the rising edge of PERST#.

Table 7. Reset Strap Pins

Signal	I/O	Description
A_133EN B_133EN	I	**PCI-X 133 MHz Enable:** This pin, when high, allows the PCI-X segment to run at 133 MHz when X_PCIXCAP is sampled high. When low, the PCI-X segment will only run at 100 MHz when X_PCIXCAP is sampled high. Use an approximately 8.2KΩ resistor to pull to VCC33 or pull-down to ground.
A_STRAP[6:0] B_STRAP[6:0]	I	**Internal Test Modes:** Straps 6, 2:0 should be pulled low and straps 5:3 must be pulled high for normal operation. X_STRAP Logic Level 0 '0' 1 '0' 2 '0' 3 '1' 4 '1' 5 '1' 6 '0' Use approximately an 8.2KΩ resistor to pull-up to VCC33 or pull-down to VSS
A_TEST[2:1] B_TEST{2:1]	I	**Internal Test Modes:** These straps should be pulled high to VCC33. Use approximately an 8.2KΩ resistor to pull-up to VCC33.
CFGRETRY	I	**Configuration Retry:** This pin, when sampled high sets the Configuration Cycle Retry Bit (bit 3) in the Bridge Initialization Register at Offset FC. If no local initialization is needed, this pin should be pulled low to VSS. Refer to the *Intel® 41210 Serial to Parallel PCI Bridge Design Guide* for more information.
Total	19	

2.8 SMBus Interface

Table 8. SMBus Interface Pins

Signal	I/O	Description
SMBCLK	I/OD	SMBus Clock: This signal should be pulled to 3.3V via an 8.2KOhm resistor.
SMBDAT	I/OD	SMBus Data: This signal should be pulled to 3.3V via an 8.2KOhm resistor.
SMBUS[5] SMBUS[3:1]	I	SMBus Addressing Straps: These straps set the SMBus Address for 41210 Bridge. The address is determined as indicated below: Bit 7‘1’ Bit 6‘1’ Bit 5SMBUS[5] Bit 4‘0’ Bit 3SMBUS[3] Bit 2SMBUS[2] Bit 1SMBUS[1] These signals (bits 5, 3:1) should be pulled up to 3.3V or down to ground. Sampled at the rising edge of PERST#.
Total	6	

2.9 Miscellaneous Pins

Table 9. Miscellaneous Pins

Signal	I/O	Description
CFGRST#	O	**Configuration Reset:** This signal is asserted low when ever the bridge goes through a fundemental reset (PERST#, RSTIN#, or PCI Express Reset). This signal should be used to indicate when the local initialization methods should be executed. Refer to the *Intel® 41210 Serial to Parallel PCI Bridge Design Guide* for more information.
PERST#	I	**PCI Express Fundamental Reset:** When low, asynchronously resets the internal logic (including sticky bits).
RSTIN#	I	**Reset In:** When Asserted, this signal asynchronously resets the internal logic and asserts X_RST# output for both PCI interfaces. This signal should be pulled high for adapter card usage.
TCK	I	**TAP Clock In**: This is the input clock to the JTAG TAP controller. Acceptable frequency is 0-16MHz If not utilizing JTAG, this signal can be left as a no connect.
TDI	I	**Test Data In:** This is the serial data input to the JTAG BSCAN shift register chain and to the JTAG BSCAN control logic. This is latched in on the rising edge of TCK. If not utilizing JTAG, this signal can be left as a no connect.
TDO	O	**Test Data Output:** This is the serial data output from the JTAG BSCAN logic If not utilizing JTAG, this signal can be left as a no connect.

Signal	I/O	Description
TMS	I	**Test Mode Select:** This signal controls the TAP controller state machine to move to different states and is sampled on the rising edge of TCK. If not utilizing JTAG, this signal can be left as a no connect.
TRST#	I	**Test Reset In:** This signal is used to asynchronously reset the JTAG BSCAN logic. If not utilizing JTAG, connect this signal to ground through a 1KΩ pull-down resistor.
RESERVED[8:1]	I	**Reserved:** (8 pins) These input pins should be pulled low Use an approximately 8.2KΩ resistor to pull-down to ground.
NC[19:18], NC[16:1] A_NC[10:1] B_NC[10:1]	O	**No Connect:** (39 pins) These output pins should be left floating
NC[17]	O	This signal requires an external pull-up, 8.2K ohm to 3.3V
Total	57	

Electrical and Thermal Characteristics 3

3.1 DC Voltage and Current Specifications

3.1.1 41210 Bridge DC Specifications

Table 10. Intel® 41210 Bridge DC Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCC15	Intel® 41210 Bridge Core	1.425	1.5	1.575	V	
VCC15	PCI-X I/O Voltage	1.425	1.5	1.575	V	
VCCAPE	Analog PCI Express Voltage	1.455	1.5	1.545	V	1
VCCAPCI[2:0]	Analog PCI Voltages	1.455	1.5	1.545		
VCCBGPE	Analog Bandgap Voltage	2.425	2.5	2.575		2
VCCPE	PCI Express Interface Voltage	1.46	1.5	1.55	V	
VCC33	PCI Bus Interface Voltage	3.0	3.3	3.6	V	
P_{TDP}	Thermal Design Power			10.2	W	

1. Transient tolerance ±5 mV above 1 MHz at package pin under DC load conditions.
2. Transient tolerance ±10 mV above 1 MHz at package pin under DC load conditions.

3.1.2 Input Characteristic Signal Association

Table 11. DC Characteristics Input Signal Association

Symbol	Signals
V_{IH1}/V_{IL1}	**Interrupt Signals**: A_IRQ[15:0]#, B_IRQ[15:0]# **PCI Signals:** A_AD[63:0], B_AD[63:0], A_CBE[7:0]#, B_CBE[7:0]#, A_PAR, B_PAR, A_DEVSEL#, B_DEVSEL#, A_FRAME#, B_FRAME#, A_IRDY#, B_IRDY#, A_TRDY#, B_TRDY#, A_STOP#, B_STOP#, A_PERR#, B_PERR#, A_SERR#, B_SERR#, A_REQ[5:0]#, B_REQ[5:0]#, A_M66EN, B_M66EN, A_133EN, B_133EN, A_PCIXCAP, B_PCIXCAP, A_PAR64, B_PAR64, A_REQ64#, B_REQ64#, A_ACK64#, B_ACK64# **Clock Signals (3.3 V Only):** A_CLKI, B_CLKI **Miscellaneous Signals:** PERST#
V_{IH2}/V_{IL2}	**PCI Express Signals**: REFCLK, REFCLK#, PETP[7:0], PETN[7:0], PE_RCOMP[1:0]
V_{IH3}/V_{IL3}	**SMB Signals:** SMBDAT, SMBCLK

3.1.3 DC Input Characteristics

Table 12. DC Input Characteristics

Symbol	Parameter	3.3 V Signal		Unit
		Min	Max	
V_{IL1}	Input Low Voltage	-0.5	0.35 VCC33	V
V_{IH1}	Input High Voltage	0.5 VCC33	VCC33 +0.5	V
Symbol	**Parameter**	**Max**		
V_{IL2}	Input Low Voltage	N/A		V
V_{IH2}	Input High Voltage	N/A		V
V_{IL3}	Input Low Voltage	0.6		V
V_{IH3}	Input High Voltage	VCC33 + 0.5		V

3.1.4 DC Characteristic Output Signal Association

Table 13. DC Characteristic Output Signal Association

Symbol	Signals
V_{OH1}/V_{OL1}	**PCI Signals**: A_AD[63:0], B_AD[63:0], A_CBE[7:0]#, B_CBE[7:0]#, A_PAR, B_PAR, A_DEVSEL#, B_DEVSEL#, A_FRAME#, B_FRAME#, A_IRDY#, B_IRDY#, A_TRDY#, B_TRDY#, A_STOP#, B_STOP#, A_PERR#, B_PERR#, A_M66EN, B_M66EN, A_GNT[6:0]#, B_GNT[5:0]#, A_LOCK#, B_LOCK#, A_PAR64, B_PAR64, A_REQ64#, B_REQ64#, A_ACK64#, B_ACK64# **PCI Clock Signals (3.3 V Only):** A_CLKO[6:0], B_CLKO[6:0], A_RST#, B_RST# **Miscellaneous Signals**: RASERR#
V_{OH2}/V_{OL2}	**PCI Express Signals:** PERP[7:0], PERN[7:0]
V_{OH3}/V_{OL3}	**SMBus Signals:** SMBDAT, SMBCLK

3.1.5 DC Output Characteristics

Table 14. DC Output Characteristic

Symbol	Parameter	3.3 V Signal		Unit	Notes
		Min	Max		
V_{OL1}	Output Low Voltage		0.1VCC33	V	(5 V) Iout = 6 mA (3.3 V) Iout = 1500 uA
V_{OH1}	Output High Voltage	0.9VCC33		V	(5 V) Iout = -2 mA (3.3 V) Iout = -500 uA
Symbol	**Parameter**	**Max**		**Unit**	**Notes**
V_{OL2}	Output Low Voltage	N/A		V	
V_{OH2}	Output High Voltage	N/A		V	
V_{OL3}	Output Low Voltage	0.4		V	I_{OL4}=14 mA
V_{OH3}	Output High Voltage	N/A		V	Open Drain

3.1.6 PCI Express Interface DC Specifications

3.1.6.1 Differential Transmitter (TX) DC Output Specifications

Table 15 defines the DC specifications of parameters for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 15. Differential Transmitter (TX) DC Output Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.80		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+}-V_{TX-D-}\|$ See Note 1.
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition See Note 1.
$V_{TX-CM-ACp}$	AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = \|V_{TX-D+} + v_{TX-D-}\| / 2 – v_{TX-CM-DC}$ $v_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\| / 2$ during L0 See Note 1.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0		100	mV	$\|V_{TX-CM-DC\ [during\ L0]} – V_{TX-CM-Idle-DC[during\ electrical\ idle]}\| <= 100mv$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\| / 2$ [electrical idle] See Note 1.

Table 15. Differential Transmitter (TX) DC Output Specifications (Sheet 2 of 2)

$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-.	0		25	mV	$\lvert V_{TX-CM-DC-D+ [during L0]} - V_{TX-CM-DC-D- [During L0.]}\rvert <= 25mV$ $V_{TX-CM-DC-D+ =} DC_{(avg)}$ of $\lvert V_{TX-D+}\rvert$ [during L0] $V_{TX-CM-DC-D- =} DC_{(avg)}$ of $\lvert V_{TX-D-}\rvert$ [during L0] See Note 1.
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-Idle-D+} - V_{Tx-Idle-D-}\rvert <= 20mV$ See Note 1.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection.			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	W	TX DC Differential Mode Low impedance
$Z_{TX-COM-High-IMP-DC}$	Transmitter Common Mode High Impedance State (DC)	5 k		20k	W	TX DC High Impedance.
C_{TX}	AC Coupling Capacitor	75		200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2, “Compliance Test/Measurement Load” on page 23 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram as shown in Minimum Transmitter Timing and Voltage Output Compliance Specification.)
2. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50W to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50W probes – see Figure 2). Note that the series capacitors CTX is optional for the return loss measurement.

3.1.6.2 Differential Receiver (RX) DC Input Specifications

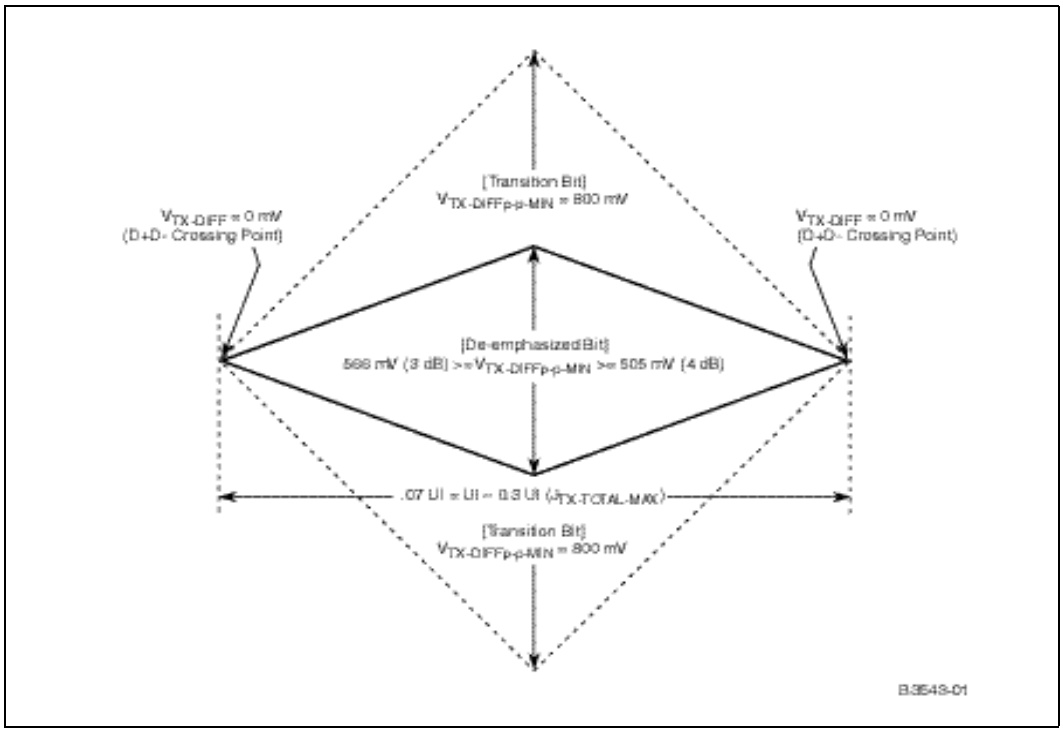
Table 16 defines the DC specifications of parameters for all differential Receivers (RXs). The parameters are specified at the component pins.

Table 16. Differential Receiver (RX) DC Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 1.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-AC}= \|V_{RX-D+} + V_{RX-D-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+}+V_{RX-D-}\|/2$ during L0 See Note 1.
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz See Note 2
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	RX DC Differential Mode impedance. See Note 3.
$Z_{RX-COM-DC}$	DC Input Common Mode Input Impedance	40	50	60	W	RX DC Common Mode impedance 50 ?+/-20% tolerance. See Notes 1 and 3.
$Z_{RX-COM-INITIAL-DC}$	Initial DC Input Common Mode Input Impedance	5	50	60	W	RX DC Common Mode impedance allowed when the receiver terminations are first powered on. See Note 4.
$Z_{RX-COM-HIGH-IMP-DC}$	Powered Down DC Input Common Mode Input Impedance	200 k			W	RX DC Common Mode impedance when the receiver terminations are not powered (i.e., no power). See Note 5.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver.

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 2, “Compliance Test/Measurement Load” on page 23 should be used as the RX device when taking measurements (also refer to the Receiver Compliance Eye Diagram as shown in Figure 3, “Minimum Receiver Eye Timing and Voltage Compliance Specification” on page 23). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
2. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50Ω probes - see Figure 2). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
3. Impedance during all operating conditions.
4. The Rx DC Common Mode Impedance that must be present when the receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the ($Z_{RX-COM-DC}$)RxDC Common Mode Impedance must be with in the specified range by the time Detect is entered.
5. The Rx DC Common Mode Impedance that exists when the receiver terminations are disabled or when no power is present. This helps ensure that the Receiver Detect circuit will not falsely assume a receiver is powered on when it is not.

Figure 1. Minimum Transmitter Timing and Voltage Output Compliance Specification



There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit.

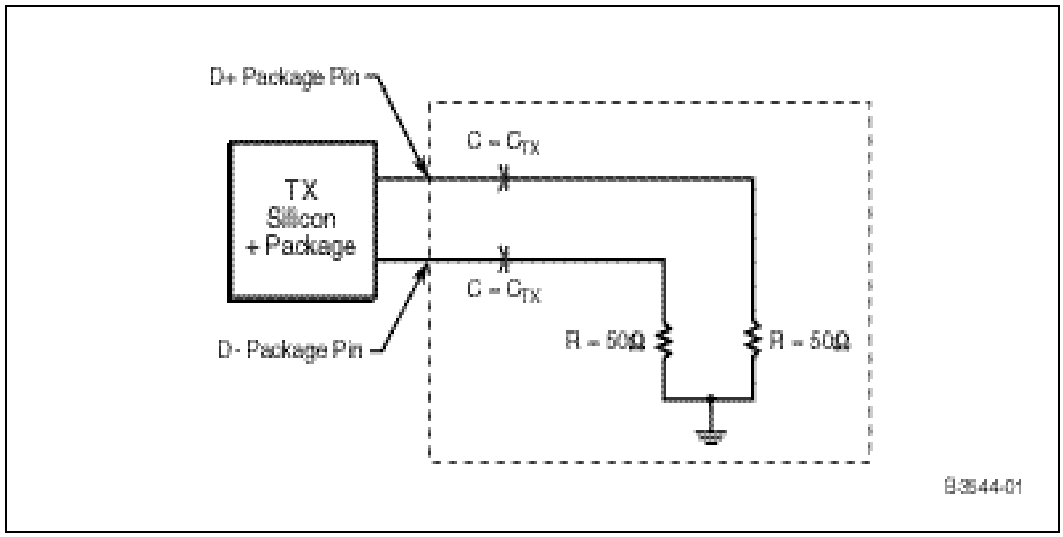
The eye diagram must be valid for any 250 consecutive UIs. An appropriate average TX UI must be used as the interval for measuring the eye diagram.

3.1.6.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified by the device vendor within 0.2 inches of the package pins, into a test/measurement load shown in Figure 2.

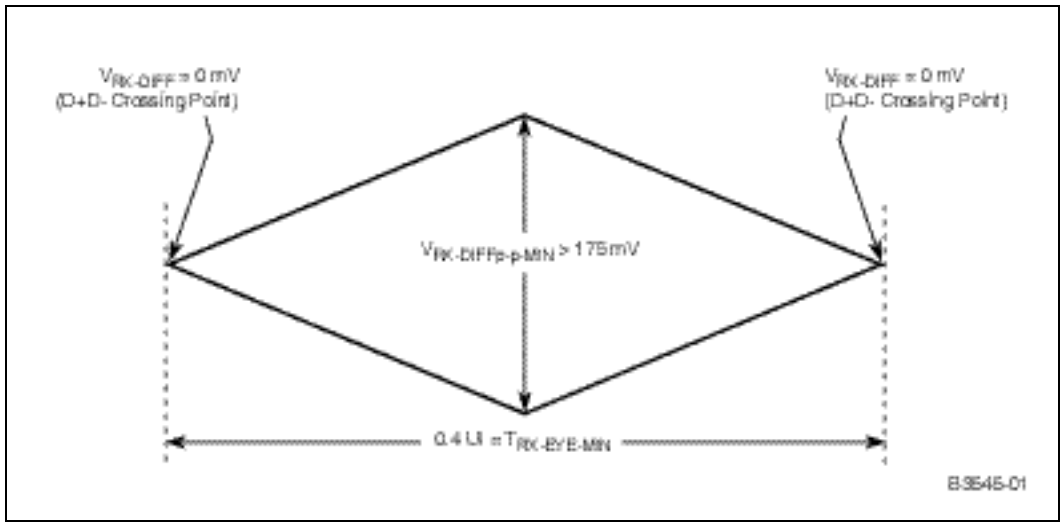
Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D-package pins.

Figure 2. Compliance Test/Measurement Load



The test load is shown at the transmitter package reference plane, but the same Test/Measurement load is applicable to the receiver package reference plane. CTX is an optional portion of the measurement test load. The measurement should be taken on the opposite side of the capacitor from the package, and the value of the CTX must be in the range of 75 nF to 200 nF.

Figure 3. Minimum Receiver Eye Timing and Voltage Compliance Specification



The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram. The eye diagram must be valid for any 250 consecutive UIs. An appropriate average TX UI must be used as the interval for measuring the eye diagram.

3.1.6.4 PCI and PCI-X Interface DC Specifications

Table 17 summarizes the DC specifications for 3.3V signaling.

Table 17. DC Specifications for PCI and PCI-X 3.3 V Signaling

Symbol	Parameter	Min	Max	Units	Condition	Notes
VCC33	Supply Voltage	3.0	3.6	V		
V_{ih}	Input High Voltage	0.5 VCC33	VCC33 +0.5	V		
V_{il}	Input Low Voltage	-0.5	0.3VCC33	V		
V_{ipu}	Input Pull-up Voltage	0.7VCC33		V		1
I_{il}	Input Leakage Current		±10	µA	$0 < V_{in} <$ VCC33	2
V_{oh}	Output High Voltage	0.9VCC33		V	I_{out} = -500 µA	
V_{ol}	Output Low Voltage		0.1VCC33	V	I_{out} = 1500 µA	
C_{in}	Input Pin Capacitance		10	pF		3
C_{clk}	X_CLKIN Pin Capacitance	5	8	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8	pF		4
L_{pin}	Pin Inductance		20	nH		5
I_{Off}	X_PME# input leakage	-	1	µA	$V_o \leq 3.6$ VCC33 off or floating	6

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
3. Absolute maximum pin capacitance for a PCI/PCIX input except X_CLKIN and X_IDSEL.
4. For conventional PCI only, lower capacitance on this input-only pin allows for non-resistive coupling to X_AD[xx]. PCI-X configuration transactions drive the AD bus four clocks before X_FRAME# asserts (see Section 2.7.2.1, “Configuration Transaction Timing,” in the *PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0a*).
5. For conventional PCI, this is a recommendation, not an absolute requirement. For PCI-X, this is a requirement.
6. This input leakage is the maximum allowable leakage into the X_PME# open drain driver when power is removed from VCC33 of the component. This assumes that no event has occurred to cause the device to attempt to assert X_PME#.

3.1.6.5 Input Clock DC Specifications

Table 18. DC Specification for Input Clock Signals

Symbol	Parameter	Min	Max	Units
CLK100	Input Low Voltage	-0.5	0.8	V
CLK100	Input High Voltage	2.0	VCC3.3 + 0.5	V
CLK133	Input Low Voltage	-0.5	0.8	V
CLK133	Input High Voltage	2.0	VCC3.3 + 0.5	V

3.1.6.6 Output Clock DC Specifications

Table 19. DC Specification for Output Clock Signals

Symbol	Parameter	Min	Max	Units	Condition
CLK33	Output Low Voltage		0.4	V	Iol = 1 mA
CLK33	Output High Voltage	2.4		V	Ioh= -1 mA
CLK66	Output Low Voltage		0.4	V	Iol = 1 mA
CLK66	Output High Voltage	2.4		V	Ioh= -1 mA
CLK100	Output Low Voltage		0.4	V	Iol = 1 mA
CLK100	Output High Voltage	2.4		V	Ioh= -1 mA
CLK133	Output Low Voltage		0.4	V	Iol = 1 mA
CLK133	Output High Voltage	2.4		V	Ioh= -1 mA

3.2 AC Specifications

3.2.1 PCI and PCI-X AC Characteristics

Table 20. Conventional PCI 3.3V AC Characteristics (Sheet 1 of 2)

Sym	Parameter	Condition	Min	Max	Unit	Note
$I_{oh(AC)}$	Switching Current High	V_{out} = 0.7VCC33		-32VCC33	mA	
		V_{out} = 0.3VCC33	-12VCC33		mA	1
$I_{ol(AC)}$	Switching Current Low	V_{out} = 0.18VCC33		38VCC33	mA	
		V_{out} = 0.6VCC33	16VCC33		mA	1
I_{ch}	High Clamp Current	VCC33 + 4 > V_{in} VCC33 + 1	25 + (V_{in} – VCC33 – 1) / 0.015		mA	

Table 20. Conventional PCI 3.3V AC Characteristics (Sheet 2 of 2)

I_{cl}	Low Clamp Current	-3 < V_{in} -1	-25 + (V_{in} + 1) / 0.015		mA	
$slew_r$	Output Rise Slew Rate	0.3VCC33 to 0.6VCC33	1	4	V/ns	2
$slew_f$	Output Fall Slew Rate	0.6VCC33 to 0.3VCC33	1	4	V/ns	2

1. In conventional PCI switching, current characteristics for X_REQ# and X_GNT# are permitted to be one half of that specified here; i.e., half size drivers may be used on these signals. This specification does not apply to CLK and RSTIN# which are system outputs. “Switching Current High” specifications are not relevant to X_SERR# which is an open drain output.
2. This parameter is to be interpreted as the cumulative edge rate across the specified range rather than the instantaneous rate at any point within the transition range. For more details on slew rate measurement conditions please refer to the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a*

Table 21. PCI-X 3.3V AC Characteristics

Sym	Parameter	Condition	Min	Max	Unit	Note
$I_{oh(AC)}$	Switching Current High	0 < VCC33 – V_{out} 3.6V		-74(VCC33 - V_{out})	mA	
		0 < VCC33 – V_{out} 1.2V	-32 (VCC33 – V_{out})		mA	1
		1.2V < VCC33 – V_{out} 1.9V	-11 (VCC33 - V_{out}) – 25.2		mA	1
		1.9V < VCC33 – V_{out} 3.6V	-1.8 (VCC33 - V_{out}) – 42.7		mA	1
$I_{ol(AC)}$	Switching Current Low	0 V_{out} 3.6V		$100V_{out}$	mA	
		0 < V_{out} 1.3V	$48V_{out}$			1
		1.3V < V_{out} 3.6V	$5.7V_{out}$ + 55			1
I_{cl}	Low Clamp Current	-3V < V_{in} ≤ -0.8875V	-40 + (V_{in} + 1) / 0.005		mA	
		-0.8875V < V_{in} ≤ -0.625V	-25 + (V_{in} + 1) / 0.015		mA	
I_{ch}	High Clamp Current	0.8875V < V_{in} – VCC33 ≤ -4V	40 + (V_{in} – VCC33 - 1) / 0.005		mA	
		0.625V < V_{in} – VCC33 ≤ 0.8875V	25 + (V_{in} – VCC33 - 1) / 0.015		mA	
$slew_r$	Output Rise Slew Rate	0.3VCC33 to 0.6VCC33	1	4	V/ns	2
$slew_f$	Output Fall Slew Rate	0.6VCC33 to 0.3VCC33	1	4	V/ns	2

1. In conventional PCI switching, current characteristics for X_REQ# and X_GNT# are permitted to be one half of that specified here; i.e., half size drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. “Switching Current High” specifications are not relevant to X_SERR#, which is an open drain output.

2. This parameter is to be interpreted as the cumulative edge rate across the specified range rather than the instantaneous rate at any point within the transition range. For more details on slew rate measurement conditions please refer to the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0*a.

3.3 Voltage Filter Specifications

The 41210 Bridge requires voltage filtering to reduce noise on critical voltage planes. There are two filter types necessary on the platform:

- Analog Voltage Filter (PCI-Express and PCI)
- Bandgap Filter

Note: For filter specifications, refer to the 41210 Serial to Parallel PCI Bridge Design Guide.

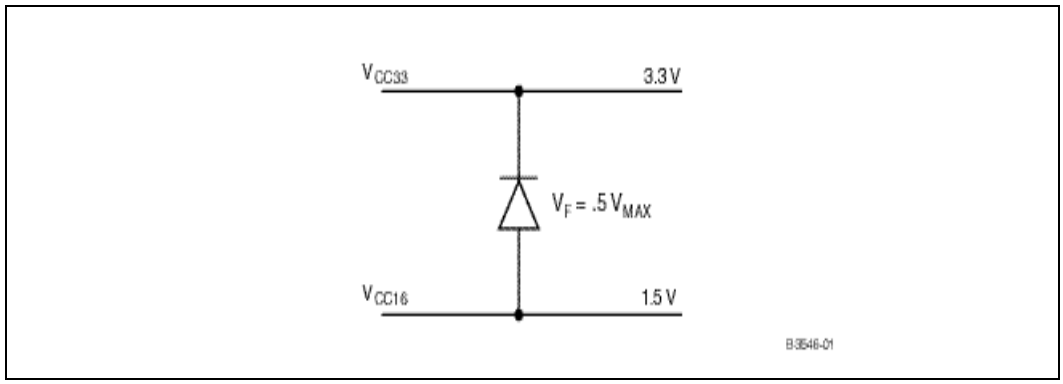
3.4 VCC15 and VCC33 Voltage Requirements

The 41210 Bridge requires that the VCC33 voltage rail be equal to or no less than 0.5V below VCC15 (absolute voltage value) at all times during 41210 Bridge operation, including during system power up and power down. In other words, the following must always be true:

$VCC33 \geq (VCC15 - 0.5V)$

Figure 4 graphically illustrates this requirement. This can be accomplished by placing a diode (with a voltage drop < 0.5V) between VCC15 and VCC33. Anode will be connected to VCC15 and cathode will be connected to VCC33.

Figure 4. Voltage Requirements VCC33 versus VCC15



3.5 Timing Specifications

3.5.1 PCI Express Interface Timing

3.5.1.1 Differential Transmitter (TX) AC Output Specifications

Table 22 defines the AC specifications of parameters for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 22. Differential Transmitter (TX) AC Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
T_{TX-EYE}	Minimum TX Eye Width	0.70			UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = .3 UI See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation for the median			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0V) in relation to an appropriate average TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes 2 and 4.
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a transmitter must be in electrical idle.
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered-set			20	UI	After sending an electrical idle ordered-set, the transmitter must meet all electrical idle specifications within this time.
$T_{TX-IDLE-RCV-DETECT-MAX}$	Maximum time spent in Electrical Idle before initiating a receiver detect sequence.			100	ms	Maximum time spent in Electrical Idle before initiating a receiver detect sequence.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500	ps	Between any two Lanes within a single Transmitter.

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2, “Compliance Test/Measurement Load” on page 23 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram as shown in Minimum Transmitter Timing and Voltage Output Compliance Specification.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4. Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 2 for both V_{TX-D+} and V_{TX-D-}.

3.5.1.2 Differential Receiver (RX) AC Input Specifications

Table 23 defines the AC specifications of parameters for all differential Receivers (RXs). The parameters are specified at the component pins.

Table 23. Differential Receiver (RX) AC Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	The UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ =1 -T_{RX-EYE} =0.6 UI See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to an appropriate average TX UI. See Notes 2 and 3.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p}$ <$V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Skew			20	ns	Across all Lanes on a port. This includes variation in the length of a skip ordered-set (e.g., COM and 1 to 5 SKP symbols) at the RX as well as any delay differences arising from the interconnect itself.

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 2, “Compliance Test/Measurement Load” on page 23 should be used as the RX device when taking measurements (also refer to the Receiver Compliance Eye Diagram as shown in Figure 3, “Minimum Receiver Eye Timing and Voltage Compliance Specification” on page 23). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same clock chip, the appropriate average TX UI must be used as the reference for the eye diagram.

3.5.2 PCI and PCI-X Interface Timing

Table 24. PCI Interface Timing

Functional Operating Range (VCC33 = 3.3 V ± 5%, Tcase=0°C to 105°C)

Symbol	Parameter	66 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max		
T_{val}	CLK to Signal Valid Delay; bused signals	2	6	2	11	ns	1, 2, 3
$T_{val}(ptp)$	CLK to Signal Valid Delay; point-to-point signals	2	6	2	12	ns	1, 2, 3
T_{on}	Float to Active Delay	2		2		ns	1, 7
T_{off}	Active to Float Delay		14		28	ns	1, 7
T_{su}	Input Setup Time to CLK; Bused signals	3		7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to CLK; point-to-point	5		10,12		ns	3, 4
T_{h}	Input Hold Time from CLK	0		0		ns	4
T_{rst}	Reset Active Time after power stable	1		1		ms	5
$T_{rst-clk}$	Reset Active Time after CLK stable	100		100		µs	5
$T_{rst-off}$	Reset Active to output float delay		40		40	ns	5, 6
T_{rrsu}	PxREQ64# to RSTIN# setup time	10		10		clocks	
T_{rrh}	RSTIN# to PxREQ64# hold Time	0	50	0	50	ns	9
T_{rhfa}	RSTIN# high to first configuration access	2^{25}		2^{25}		clocks	
T_{rhff}	RSTIN# high to first PxFRAME# Assertion	5		5		clocks	
T_{pvrh}	Power Valid to RSTIN# High	100		100		ms	

1. It is important that all driven signal transitions drive to their V_{oh} or V_{ol} level within one T_{cyc}.
2. Minimum times are measured at the package pin (not the test point) with the load circuit shown in the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.* Maximum times are measured with the test point and load circuit shown in the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.*
3. X_REQ_[5:0]# and X_GNT_[5:0]# are point-to-point signals and have different input setup times than do bused signals. X_GNT_[5:0]# and X_REQ_[5:0]# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See Section 3.5, “Timing Specifications” on page 28 and the measurement conditions in the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.*
5. If X_M66EN is asserted, CLK is stable when it meets the requirements in the *PCI Local Bus Specification Revision 2.3.* RSTIN# is asserted and deasserted asynchronously with respect to CLK.
6. When X_M66EN is asserted, the minimum specification for T_{val}(min), T_{val}(ptp)(min), and T_{on} may be reduced to 1 ns if a mechanism is provided to guarantee a minimum value of 2 ns when X_M66EN is deasserted.
7. For purposes of active/float timing measurements, the Hi-Z or “off” state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time. Refer to the *PCI Local Bus Specification Revision 2.3* for more details.
9. Maximum value is also limited by delay to the first transaction (T_{rhff}).

Figure 5. PCI Output Timing

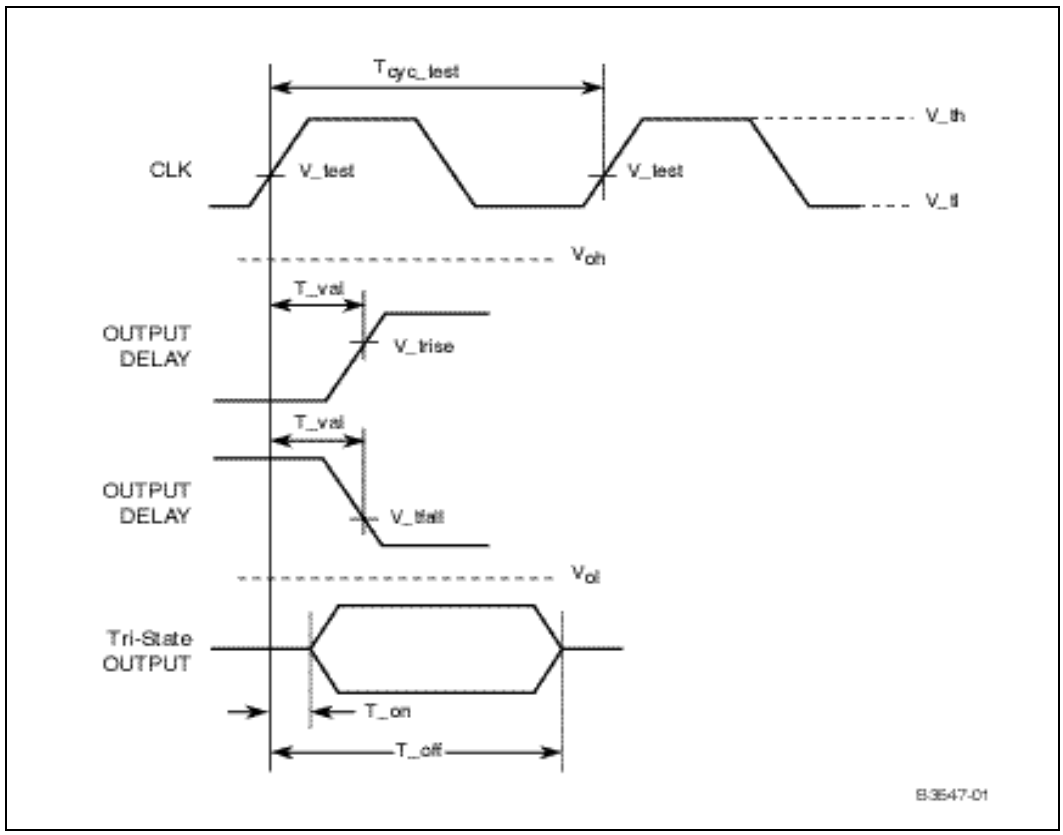


Figure 6. PCI Input Timing

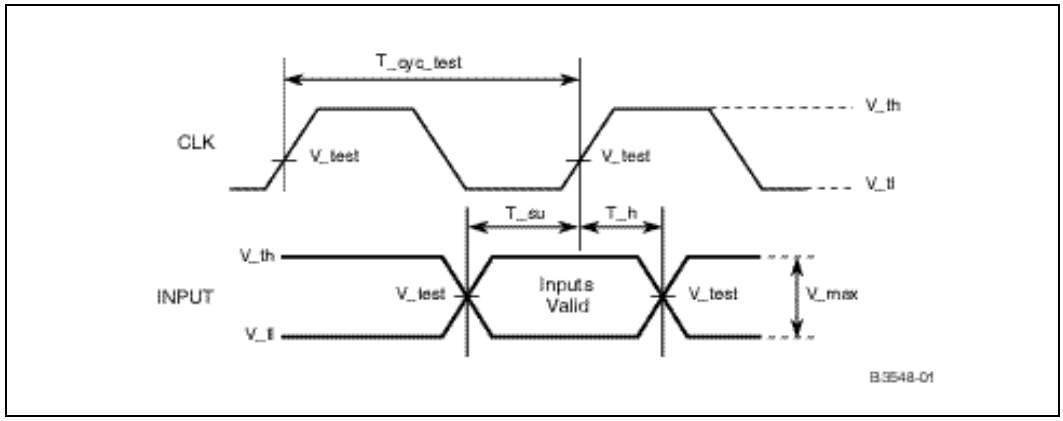


Table 25. PCI-X 3.3V Signal Timing Parameters (Sheet 1 of 2)

Sym	Parameter	PCI-X 133		PCI-X 66		Units	Notes
		Min	Max	Min	Max		
T_{val}	CLK to Signal Valid Delay	0.7	3.8	0.7	3.8	ns	1, 2, 8

Table 25. PCI-X 3.3V Signal Timing Parameters (Sheet 2 of 2)

T_{on}	Float to Active Delay	0		0		ns	1, 6, 8
T_{off}	Active to Float Delay		7		7	ns	1, 6, 8
T_{su}	Input Setup Time to CLK	1.2		1.7		ns	3, 7
T_{h}	Input Hold Time from CLK	0.5		0.5		ns	3
T_{rst}	Reset Active Time after power stable	1		1		ms	4
$T_{rst-clk}$	Reset Active Time after CLK stable	100		100		µs	4
$T_{rst-off}$	Reset Active to output float delay		40		40	ns	4
T_{rrsu}	PxREQ64# to RSTIN# setup time	10		10		ns	
T_{rrh}	RSTIN# to PxREQ64# hold Time	0	50	0	50	ns	7
T_{rhfa}	RSTIN# high to first configuration access	2^{26}		2^{26}		clocks	
T_{rhff}	RSTIN# high to first PxFRAME# Assertion	5		5		clocks	
T_{pvrh}	Power valid to RSTIN# high	100		100		ms	
T_{prsu}	PCI-X initialization pattern to RSTIN# setup time	10		10		clocks	
T_{prh}	RSTIN# to PCI-X initialization pattern hold time	0	50	0	50	ns	7
T_{rlcx}	Delay from RSTIN# low to CLK frequency change	0		0		ns	

1. See the timing measurement conditions in Section 3.5, “Timing Specifications” on page 28.
2. Minimum times are measured at the package pin (not the test point) with the load circuit shown in the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.* Maximum times are measured with the test point and load circuit shown in *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.*
3. See the timing measurement conditions in Section 3.5, “Timing Specifications” on page 28 and the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.*
4. RST# is asserted and deasserted asynchronously with respect to CLK.
5. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification
6. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
7. Maximum value is also limited by delay to the first transaction (T_{rhfa}). The PCI-X initialization pattern control signals after the rising edge of RSTIN# must be deasserted no later than two clocks before the first PxFRAME# and must be floated no later than one clock before PxFRAME# is asserted.
8. Device must meet this specification independent of how many outputs switch simultaneously.

3.5.3 PCI and PCI-X Clock Specification

Clock measurement conditions are the same for PCI-X devices as for conventional PCI devices in a 3.3V signaling environment except for voltage levels specified in Table 26, "PCI and PCI-X Clock Timings" on page 33. The same spread-spectrum clocking techniques are allowed in PCI-X as for 66 MHz conventional PCI. If a device includes a PLL, that PLL must track the input variations of spread-spectrum clocking specified in Table 26.

Figure 7. PCI-X 3.3V Clock Waveform

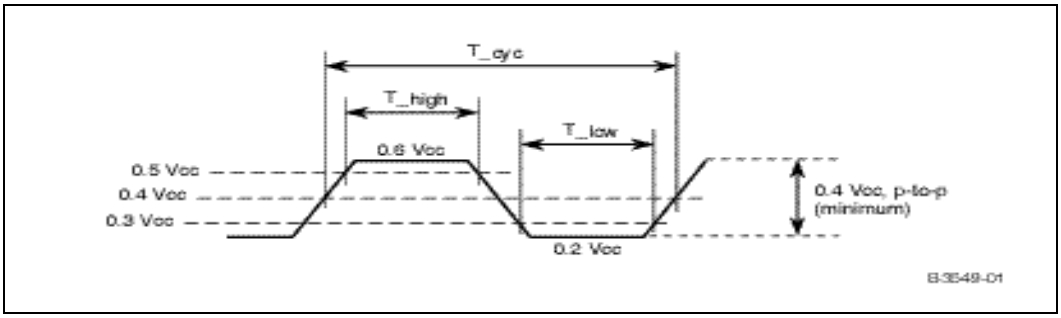


Table 26. PCI and PCI-X Clock Timings

Symbol	Parameter		PCI-X 133		PCI-X 66		PCI 66		PCI 33		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
T_{cyc}	CLK Cycle Time	Average	7.5	20	15	20	15	30	30	∞	ns	1,3,4
		Absolute Minimum	7.375		14.8		14.8		29.7		ns	1,3
T_{high}	CLK high time		3		6		6		11		ns	
T_{low}	CLK low time		3		6		6		11		ns	
T_{jit}	CLK Period Jitter		125	-125	200	-200	200	-200	300	-300	ps	5
Slew Rate												
—	CLK slew rate		1.5	4	1.5	4	1.5	4	1	4	V/ns	2
Spread Spectrum Requirements												
fmod	Modulation frequency		30	33	30	33	30	33			kHz	
fspread	Frequency spread		-1	0	-1	0	-1	0			%	

1. For clock frequencies above 33 MHz, the clock frequency may not change beyond the spread-spectrum and jitter limits except while RSTIN# is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in the *PCI-X Electrical and Mechanical Addendum, Revision 2.0a.*
3. The minimum clock period must not be violated for any single clock cycle (i.e. accounting for all system jitter).
4. Average T_{cyc} is measured over any 1 µs period of time and must include all sources of clock variation.

5. Period jitter is the deviation between any single period of the clock, T_{cyc}, and the average period of the clock, $T_{cyc(average)}$.

3.5.4 41210 Bridge Clock Timings

Table 27. 41210 Bridge Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
CLK100					
T_{period}	Average Period	10.0	10.2	ns	6
T_{rise}	Rise time across 600 mV	300	600	ps	7,8
T_{fall}	Fall time across 600 mV	300	600	ps	7,8
—	Rise/Fall Matching		20%		7,9
—	Cross point at 1 V	0.51	0.76	V	
$T_{ccjitter}$	Cycle to Cycle jitter		200	ps	
—	Duty Cycle	45	55	%	
—	Maximum voltage allowed at input		1.45	V	
—	Minimum voltage allowed at input		-200	mV	
—	Rising edge ringback	0.85		V	
—	Falling edge ring back		0.35	V	
CLK133					
T_{period}	Average Period	7.5	7.65	ns	6
T_{rise}	Rise time across 600 mV	300	600	ps	7,8
T_{fall}	Fall time across 600 mV	300	600	ps	7,8
—	Rise/Fall Matching		20%		7,9
—	Cross point at 1V	0.51	0.76	V	
$T_{ccjitter}$	Cycle to Cycle jitter		125	ps	10
—	Duty Cycle	45	55	%	
—	Maximum voltage allowed at input		1.45	V	
—	Minimum voltage allowed at input		-200	mV	
—	Rising edge ringback	0.85		V	
—	Falling edge ring back		0.35	V	
CLK33					
T_{period}	CLK period	30.0	N/A	ns	1,2
T_{high}	CLK high time	12.0	N/A	ns	3
T_{low}	CLK low time	12.0	N/A	ns	4
—	Rising edge rate	1.0	4.0	V/ns	5
—	Falling edge rate	1.0	4.0	V/ns	5
T_{rise}	CLK rise time	0.5	2.0	ns	5
T_{fall}	CLK fall time	0.5	2.0	ns	5

1. Period, jitter, offset and skew measured on rising edge @ 1.5V for 3.3V clocks.

2. The average period over any 1 us period of time must be greater than the minimum specified period.
3. T_{high} is measured at 2.4V for non-host outputs.
4. T_{low} is measured at 0.4V for all outputs.
5. For 3.3V clocks T_{rise} and T_{fall} are measured as a transition through the threshold region V_{ol} = 0.4V and V_{oh} = 2.4V (1 mA) JEDEC Specification.
6. Measured at crossing point.
7. Measured from V_{ol} = 0.2V to V_{oh} = 0.8V.
8. Still simulating to determine [0.2–0.8 V] or [0.3–0.9 V].
9. Determined as a fraction of $2*(T_{rise} - T_{fall}) / (T_{rise} + T_{fall})$.
10. Period jitter is the deviation between any single period of the clock, T_{cyc}, and the average period of the clock, T_{cyc}(average).

3.5.4.1 Spread Spectrum Clocking

Spread spectrum clocking can be used on the 41210 Bridge to reduce energy. Spread Spectrum clocking is a common technique used by system designers to meet FCC emissions, where the frequency is deliberately shifted around to spread the energy off of the peak. The following is to be observed when using Spread Spectrum clocking:

- All device timings (including jitter, skew, min/max clock period, output rise/fall time) MUST meet the existing non-spread spectrum specifications
- All non-spread Host and PCI functionality must be maintained in the spread spectrum mode (includes all power management functions.)
- The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called “down-spreading”. The modulation profile in a modulation period can be expressed as:

  Equations:

$$f = \begin{cases} (1-\delta) f_{nom} + 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad 0 < t < \dfrac{1}{2 f_m}; \\ (1+\delta) f_{nom} - 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad \dfrac{1}{2 f_m} < t < \dfrac{1}{f_m}, \end{cases}$$

  where:

  f_{nom} is the nominal frequency in the non-SSC mode

  f_m is the modulation frequency

  f_m is the modulation amount

  t is time.

3.6 41210 Bridge Power Consumption

Table 28 provides details on the maximum draw from the power planes by the 41210 Bridge for use in voltage regulation.

Table 28. 41210 Bridge Maximum Voltage Plane Currents

Power Plane	Maximum Voltage Plane Current (Amps)		
Frequency (MHz)	133	100	66
Number of Slots	1	2	4
I_{VCC15} (core 1.5V)	1.68	1.61	1.55
I_{VCC15} (I/O 1.5V)	0.22	0.22	0.22
VCCBGPE	0.005	0.005	0.005
I_{VCCPE} (PCI Express 1.5V)	0.70	0.70	0.70
I_{VCC33} (PCI/PCI-X Mode 1 3.3V) [1]	1.05	1.14	1.22

1. Per PCI-X Bus segment

Table 29 provides details on the maximum nominal draw from the power planes by the 41210 Bridge for use in thermal design.

Table 29. 41210 Bridge Thermal Voltage Plane Currents

Power Plane	Thermal Voltage Plane Current (Amps)		
Frequency (MHz)	133	100	66
Number of Slots	1	2	4
I_{VCC15} (core 1.5V)	1.24	1.18	1.11
I_{VCC15} (I/O 1.5V)	0.22	0.22	0.22
VCCBGPE	0.005	0.005	0.005
I_{VCCPE} (PCI Express 1.5V)	0.69	0.69	0.69
I_{VCC33} (PCI/PCI-X Mode 1 3.3V) [1]	0.99	1.04	1.10

1. Per PCI-X Bus segment

3.7 Power Delivery Guidelines

Please refer to the *Intel® 41210 Serial to Parallel PCI Bridge Design Guide*.

3.8 Reference and Compensation Pins

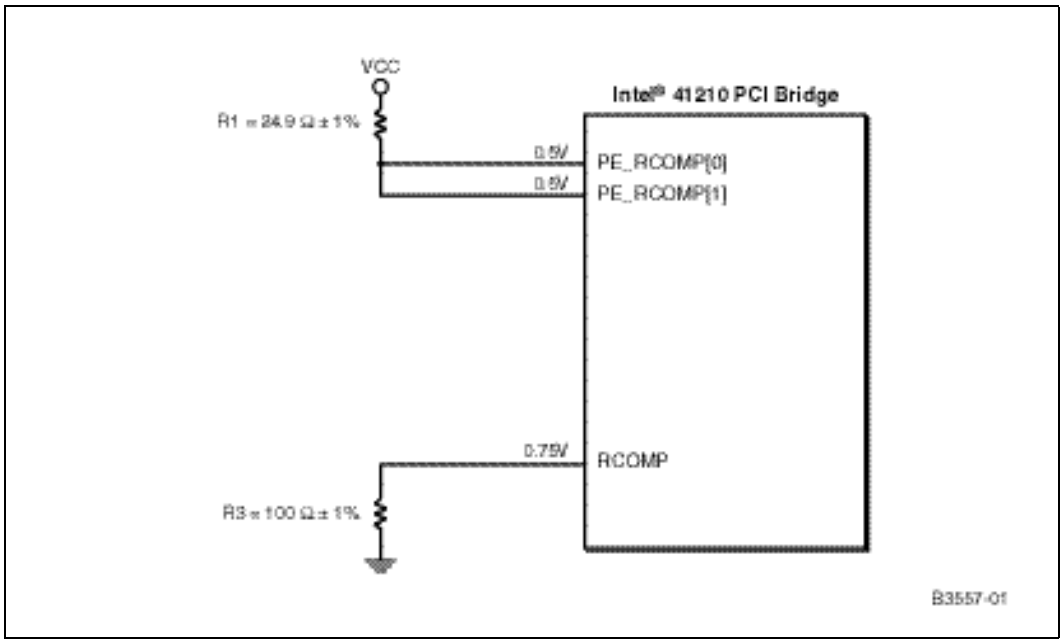
The 41210 Bridge has one reference pin and three compensation pins:

- **PE_RCOMP[1:0]** are two separate pins that provide voltage compensation for the PCI Express interface on the 41210 Bridge. The nominal compensation voltage is 0.5V. An external 24.9 ±1% pull-up resistor should be used to connect to VCC15. A single pull-up resistor can be used to for both of these signals.

- **RCOMP** is an analog PCI interface compensation pin to the 41210 Bridge. A 100 ±1% pull-down resistor should be used to connect the **RCOMP** pin to ground.

All three of these implementations are shown in Figure 8.

Figure 8. 41210 Bridge Reference and Compensation Circuit Implementations



3.9 Thermal Specifications

3.9.1 Power

For TDP specifications, see 41210 Bridge Thermal Specifications for the 41210 Bridge component. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for a heatsink when using the 41210 Bridge component.

3.9.2 Die Temperature

To ensure proper operation and reliability of the 41210 Bridge component, the die temperatures must be at or below the values specified in Table 30. System and/or component level thermal solutions are required to maintain die temperatures below the maximum temperature specifications.

Table 30. 41210 Bridge Thermal Specifications

Parameter	Maxinum
T_{case}	105×C
$TDP_{Mode\#1/Mode\#1}$	8.70W
$TDP_{Mode\#1/No\ Connect}$	8.30W
$TDP_{DDR/No\ Connect}$	8.10W

Note: Mode 1: PCI-X 66MHz, 64-bit, 4 slots/devices

No Connect: Unused PCI segment (no slots/devices on PCI bus segment)

3.9.3 Thermal Solution Component Suppliers

3.9.3.1 Torsional Clip Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: Unidirectional Fin Heatsink Thermal Interface Material Torsional Clip	C76435-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Unidirectional Fin Heatsink (31.0 x 31.0 x 12.2mm)	C76434-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Thermal Interface (Chomerics T-710)	A69230-001	Chomerics 69-12-22066-T710	Todd Sousa (USA) 360-606-8171 tsousa@parker.com
Heatsink Attach Clip	C17725-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Solder-Down Anchor	A13494-005	Foxconn (HB96030-DW)	Julia Jiang (USA) 408-919-6178 juliaj@foxconn.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

Package Specification and Ballout 4

4.1 Package Specification

The 41210 Bridge is in a 567-ball FCBGA package, 31mm X 31mm in size, with a 1.27mm ball pitch (see Figure 9 and Figure 10).

Figure 9. 41210 Bridge Package Dimensions (Top View)

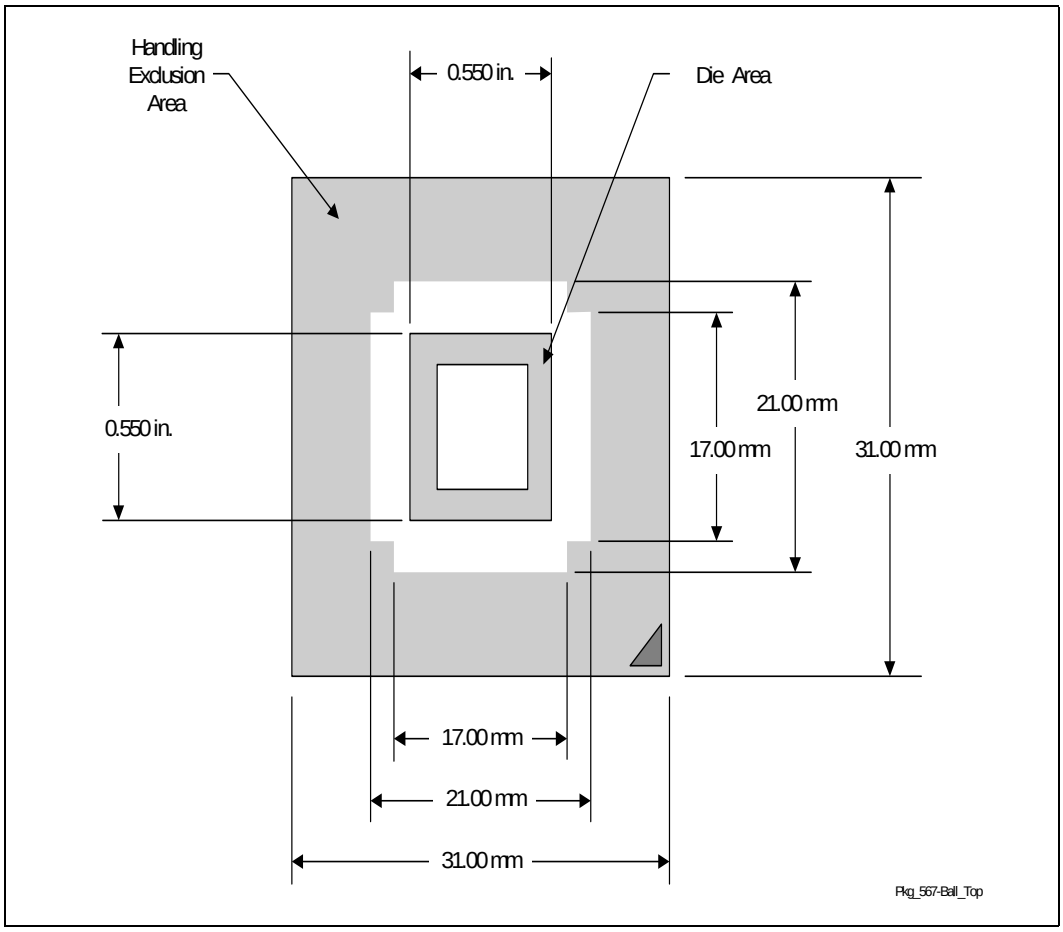
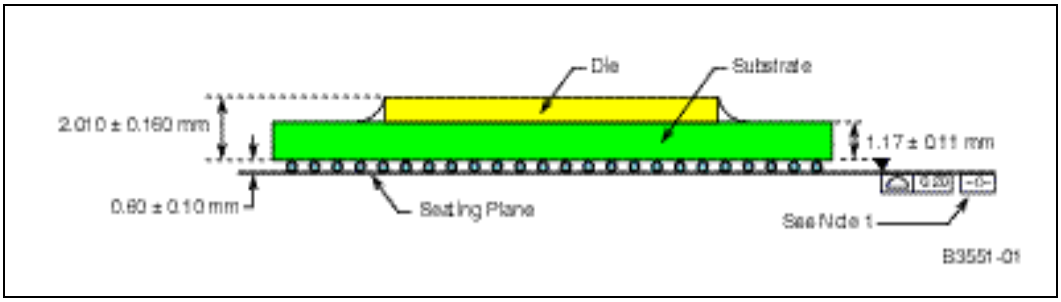


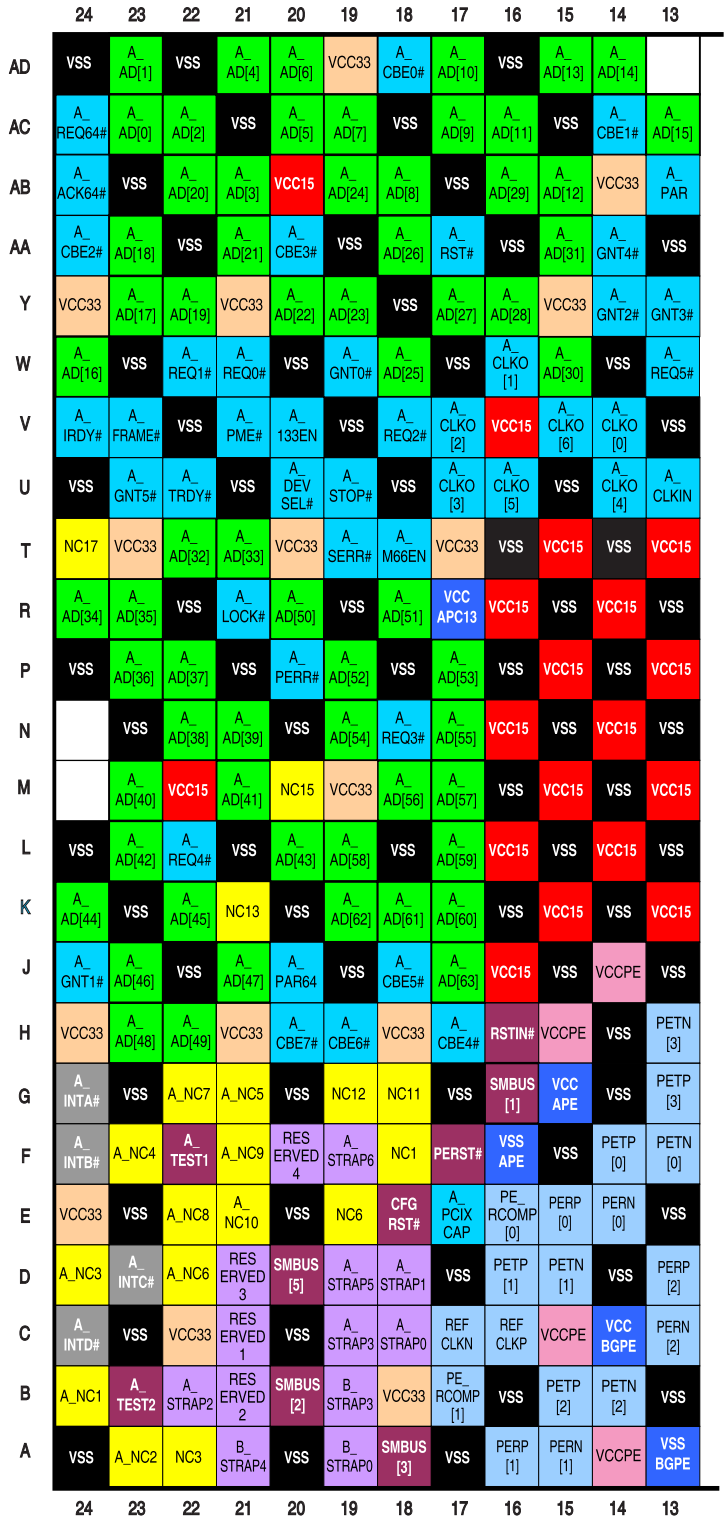
Figure 10. 41210 Bridge Package Dimensions (Side View)



Note: Primary datum -C- and seating plane are defined by the spherical crowns of the solder balls.

Note: All dimensions and tolerances conform to ANSI Y14.5M-1982

4.2 Ball Map



	24	23	22	21	20	19	18	17	16	15	14	13
AD	VSS	A_AD[1]	VSS	A_AD[4]	A_AD[6]	VCC33	A_CBE0#	A_AD[10]	VSS	A_AD[13]	A_AD[14]	
AC	A_REQ64#	A_AD[0]	A_AD[2]	VSS	A_AD[5]	A_AD[7]	VSS	A_AD[9]	A_AD[11]	VSS	A_CBE1#	A_AD[15]
AB	A_ACK64#	VSS	A_AD[20]	A_AD[3]	VCC15	A_AD[24]	A_AD[8]	VSS	A_AD[29]	A_AD[12]	VCC33	A_PAR
AA	A_CBE2#	A_AD[18]	VSS	A_AD[21]	A_CBE3#	VSS	A_AD[26]	A_RST#	VSS	A_AD[31]	A_GNT4#	VSS
Y	VCC33	A_AD[17]	A_AD[19]	VCC33	A_AD[22]	A_AD[23]	VSS	A_AD[27]	A_AD[28]	VCC33	A_GNT2#	A_GNT3#
W	A_AD[16]	VSS	A_REQ1#	A_REQ0#	VSS	A_GNT0#	A_AD[25]	VSS	A_CLKO[1]	A_AD[30]	VSS	A_REQ5#
V	A_IRDY#	A_FRAME#	VSS	A_PME#	A_133EN	VSS	A_REQ2#	A_CLKO[2]	VCC15	A_CLKO[6]	A_CLKO[0]	VSS
U	VSS	A_GNT5#	A_TRDY#	VSS	A_DEVSEL#	A_STOP#	VSS	A_CLKO[3]	A_CLKO[5]	VSS	A_CLKO[4]	A_CLKIN
T	NC17	VCC33	A_AD[32]	A_AD[33]	VCC33	A_SERR#	A_M66EN	VCC33	VSS	VCC15	VSS	VCC15
R	A_AD[34]	A_AD[35]	VSS	A_LOCK#	A_AD[50]	VSS	A_AD[51]	VCC APC13	VCC15	VSS	VCC15	VSS
P	VSS	A_AD[36]	A_AD[37]	VSS	A_PERR#	A_AD[52]	VSS	A_AD[53]	VSS	VCC15	VSS	VCC15
N		VSS	A_AD[38]	A_AD[39]	VSS	A_AD[54]	A_REQ3#	A_AD[55]	VCC15	VSS	VCC15	VSS
M		A_AD[40]	VCC15	A_AD[41]	NC15	VCC33	A_AD[56]	A_AD[57]	VSS	VCC15	VSS	VCC15
L	VSS	A_AD[42]	A_REQ4#	VSS	A_AD[43]	A_AD[58]	VSS	A_AD[59]	VCC15	VSS	VCC15	VSS
K	A_AD[44]	VSS	A_AD[45]	NC13	VSS	A_AD[62]	A_AD[61]	A_AD[60]	VSS	VCC15	VSS	VCC15
J	A_GNT1#	A_AD[46]	VSS	A_AD[47]	A_PAR64	VSS	A_CBE5#	A_AD[63]	VCC15	VSS	VCCPE	VSS
H	VCC33	A_AD[48]	A_AD[49]	VCC33	A_CBE7#	A_CBE6#	VCC33	A_CBE4#	RSTIN#	VCCPE	VSS	PETN[3]
G	A_INTA#	VSS	A_NC7	A_NC5	VSS	NC12	NC11	VSS	SMBUS[1]	VCC APE	VSS	PETP[3]
F	A_INTB#	A_NC4	A_TEST1	A_NC9	RESERVED 4	A_STRAP6	NC1	PERST#	VSS APE	VSS	PETP[0]	PETN[0]
E	VCC33	VSS	A_NC8	A_NC10	VSS	NC6	CFG RST#	A_PCIX CAP	PE_RCOMP[0]	PERP[0]	PERN[0]	VSS
D	A_NC3	A_INTC#	A_NC6	RESERVED 3	SMBUS[5]	A_STRAP5	A_STRAP1	VSS	PETP[1]	PETN[1]	VSS	PERP[2]
C	A_INTD#	VSS	VCC33	RESERVED 1	VSS	A_STRAP3	A_STRAP0	REF CLKN	REF CLKP	VCCPE	VCC BGPE	PERN[2]
B	A_NC1	A_TEST2	A_STRAP2	RESERVED 2	SMBUS[2]	B_STRAP3	VCC33	PE_RCOMP[1]	VSS	PETP[2]	PETN[2]	VSS
A	VSS	A_NC2	NC3	B_STRAP4	VSS	B_STRAP0	SMBUS[3]	VSS	PERP[1]	PERN[1]	VCCPE	VSS BGPE
	24	23	22	21	20	19	18	17	16	15	14	13

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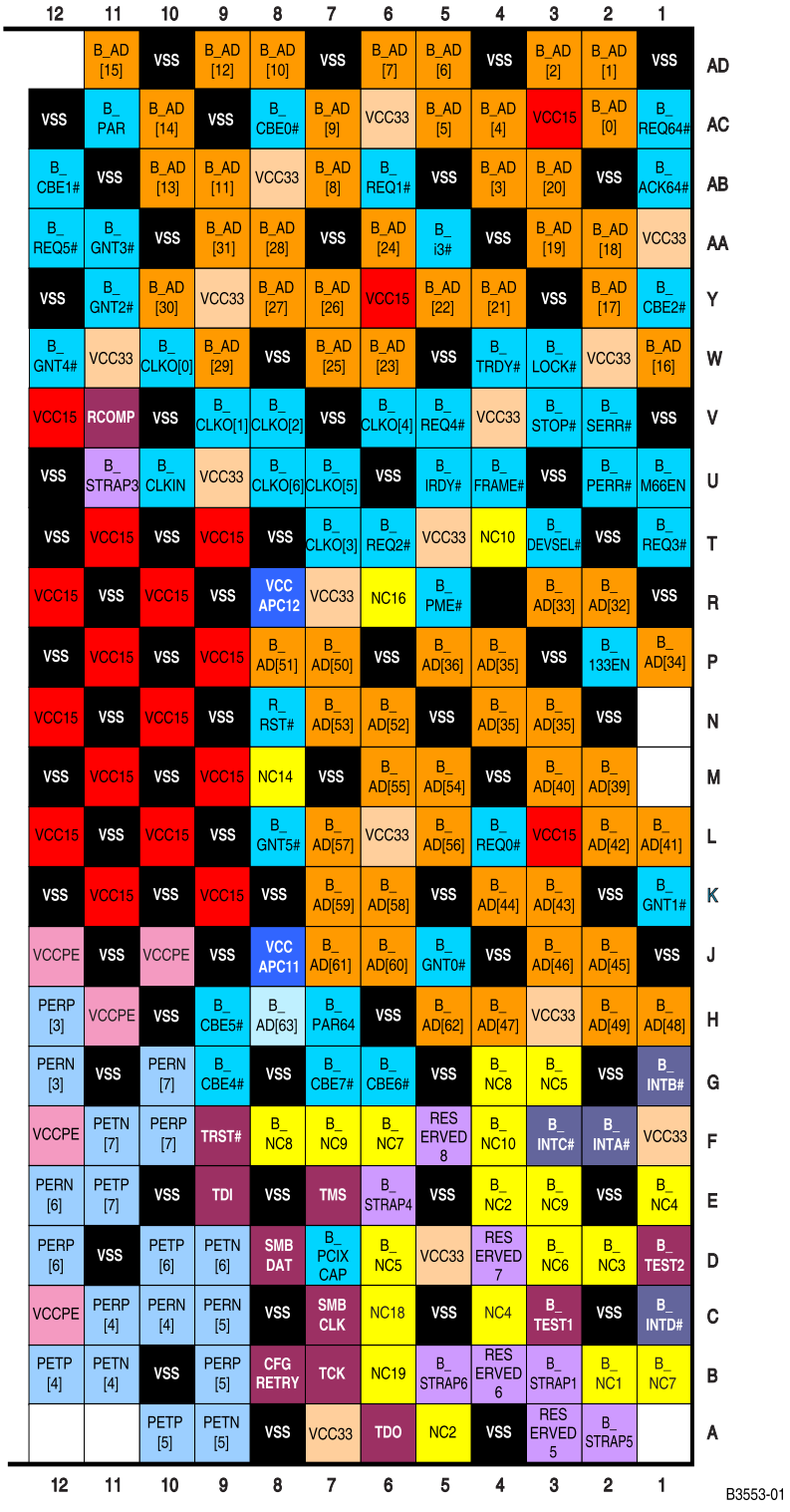
12 11 10 9 8 7 6 5 4 3 2 1
AD: | | B_AD [15] | VSS | B_AD [12] | B_AD [10] | VSS | B_AD [7] | B_AD [6] | VSS | B_AD [2] | B_AD [1] | VSS |
AC: VSS | B_ PAR | B_AD [14] | VSS | B_ CBE0# | B_AD [9] | VCC33 | B_AD [5] | B_AD [4] | VCC15 | B_AD [0] | B_ REQ64#
AB: B_ CBE1# | VSS | B_AD [13] | B_AD [11] | VCC33 | B_AD [8] | B_ REQ1# | VSS | B_AD [3] | B_AD [20] | VSS | B_ ACK64#
AA: B_ REQ5# | B_ GNT3# | VSS | B_AD [31] | B_AD [28] | VSS | B_AD [24] | B_ i3# | VSS | B_AD [19] | B_AD [18] | VCC33
Y: VSS | B_ GNT2# | B_AD [30] | VCC33 | B_AD [27] | B_AD [26] | VCC15 | B_AD [22] | B_AD [21] | VSS | B_AD [17] | B_ CBE2#
W: B_ GNT4# | VCC33 | B_ CLKO[0] | B_AD [29] | VSS | B_AD [25] | B_AD [23] | VSS | B_ TRDY# | B_ LOCK# | VCC33 | B_AD [16]
V: VCC15 | RCOMP | VSS | B_ CLKO[1] | B_ CLKO[2] | VSS | B_ CLKO[4] | B_ REQ4# | VCC33 | B_ STOP# | B_ SERR# | VSS
U: VSS | B_ STRAP3 | B_ CLKIN | VCC33 | B_ CLKO[6] | B_ CLKO[5] | VSS | B_ IRDY# | B_ FRAME# | VSS | B_ PERR# | B_ M66EN
T: VSS | VCC15 | VSS | VCC15 | VSS | B_ CLKO[3] | B_ REQ2# | VCC33 | NC10 | B_ DEVSEL# | VSS | B_ REQ3#
R: VCC15 | VSS | VCC15 | VSS | VCC APC12 | VCC33 | NC16 | B_ PME# | | B_ AD[33] | B_ AD[32] | VSS
P: VSS | VCC15 | VSS | VCC15 | B_ AD[51] | B_ AD[50] | VSS | B_ AD[36] | B_ AD[35] | VSS | B_ 133EN | B_ AD[34]
N: VCC15 | VSS | VCC15 | VSS | R_ RST# | B_ AD[53] | B_ AD[52] | VSS | B_ AD[35] | B_ AD[35] | VSS | |
M: VSS | VCC15 | VSS | VCC15 | NC14 | VSS | B_ AD[55] | B_ AD[54] | VSS | B_ AD[40] | B_ AD[39] | |
L: VCC15 | VSS | VCC15 | VSS | B_ GNT5# | B_ AD[57] | VCC33 | B_ AD[56] | B_ REQ0# | VCC15 | B_ AD[42] | B_ AD[41]
K: VSS | VCC15 | VSS | VCC15 | VSS | B_ AD[59] | B_ AD[58] | VSS | B_ AD[44] | B_ AD[43] | VSS | B_ GNT1#
J: VCCPE | VSS | VCCPE | VSS | VCC APC11 | B_ AD[61] | B_ AD[60] | B_ GNT0# | VSS | B_ AD[46] | B_ AD[45] | VSS
H: PERP [3] | VCCPE | VSS | B_ CBE5# | B_ AD[63] | B_ PAR64 | VSS | B_ AD[62] | B_ AD[47] | VCC33 | B_ AD[49] | B_ AD[48]
G: PERN [3] | VSS | PERN [7] | B_ CBE4# | VSS | B_ CBE7# | B_ CBE6# | VSS | B_ NC8 | B_ NC5 | VSS | B_ INTB#
F: VCCPE | PETN [7] | PERP [7] | TRST# | B_ NC8 | B_ NC9 | B_ NC7 | RES ERVED 8 | B_ NC10 | B_ INTC# | B_ INTA# | VCC33
E: PERN [6] | PETP [7] | VSS | TDI | VSS | TMS | B_ STRAP4 | VSS | B_ NC2 | B_ NC9 | VSS | B_ NC4
D: PERP [6] | VSS | PETP [6] | PETN [6] | SMB DAT | B_ PCIX CAP | B_ NC5 | VCC33 | RES ERVED 7 | B_ NC6 | B_ NC3 | B_ TEST2
C: VCCPE | PERP [4] | PERN [4] | PERN [5] | VSS | SMB CLK | NC18 | VSS | NC4 | B_ TEST1 | VSS | B_ INTD#
B: PETP [4] | PETN [4] | VSS | PERP [5] | CFG RETRY | TCK | NC19 | B_ STRAP6 | RES ERVED 6 | B_ STRAP1 | B_ NC1 | B_ NC7
A: | | PETP [5] | PETN [5] | VSS | VCC33 | TDO | NC2 | VSS | RES ERVED 5 | B_ STRAP5 | |
12 11 10 9 8 7 6 5 4 3 2 1

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4.3 Signal List, sorted by Ball Location

Table 31. Signal List, sorted by Ball Name (Sheet 1 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1		C1	B_INTD#	E1	B_NC4
A2	B_STRAP5	C2	VSS	E2	VSS
A3	RESERVED5	C3	B_TEST1	E3	B_NC9
A4	VSS	C4	NC4	E4	B_NC2
A5	NC2	C5	VSS	E5	VSS
A6	TDO	C6	NC18	E6	B_STRAP4
A7	VCC33	C7	SMBCLK	E7	TMS
A8	VSS	C8	VSS	E8	VSS
A9	PETN[5]	C9	PERN[5]	E9	TDI
A10	PETP[5]	C10	PERN[4]	E10	VSS
A11		C11	PERP[4]	E11	PETP[7]
A12		C12	VCCPE	E12	PERN[6]
A13	VSSBGPE	C13	PERN[2]	E13	VSS
A14	VCCPE	C14	VCCBGPE	E14	PERN[0]
A15	PERN[1]	C15	VCCPE	E15	PERP[0]
A16	PERP[1]	C16	REFCLKP	E16	PE_RCOMP[0]
A17	VSS	C17	REFCLKN	E17	A_PCIXCAP
A18	SMBUS[3]	C18	A_STRAP0	E18	CFGRST#
A19	B_STRAP0	C19	A_STRAP3	E19	NC6
A20	VSS	C20	VSS	E20	VSS
A21	A_STRAP4	C21	RESERVED1	E21	A_NC10
A22	NC3	C22	VCC33	E22	A_NC8
A23	A_NC2	C23	VSS	E23	VSS
A24	VSS	C24	A_INTD#	E24	VCC33
B1	B_NC7	D1	B_TEST2	F1	VCC33
B2	B_NC1	D2	B_NC3	F2	B_INTA#
B3	B_STRAP1	D3	B_NC6	F3	B_INTC#
B4	RESERVED6	D4	RESERVED7	F4	B_NC10
B5	B_STRAP6	D5	VCC33	F5	RESERVED8
B6	NC19	D6	NC5	F6	NC7
B7	TCK	D7	B_PCIXCAP	F7	NC9
B8	CFGRETRY	D8	SMBDAT	F8	NC8
B9	PERP[5]	D9	PETN[6]	F9	TRST#
B10	VSS	D10	PETP[6]	F10	PERP[7]
B11	PETN[4]	D11	VSS	F11	PETN[7]
B12	PETP[4]	D12	PERP[6]	F12	VCCPE
B13	VSS	D13	PERP[2]	F13	PETN[0]
B14	PETN[2]	D14	VSS	F14	PETP[0]
B15	PETP[2]	D15	PETN[1]	F15	VSS
B16	VSS	D16	PETP[1]	F16	VSSAPE
B17	PE_RCOMP[1]	D17	VSS	F17	PERST#
B18	VCC33	D18	A_STRAP1	F18	NC1
B19	B_STRAP2	D19	A_STRAP5	F19	A_STRAP6
B20	SMBUS[2]	D20	SMBUS[5]	F20	RESERVED4
B21	RESERVED2	D21	RESERVED3	F21	A_NC9
B22	A_STRAP2	D22	A_NC6	F22	A_TEST1
B23	A_TEST2	D23	A_INTC#	F23	A_NC4
B24	A_NC1	D24	A_NC3	F24	A_INTB#

Table 31. Signal List, sorted by Ball Name (Sheet 2 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
G1	B_INTB#	J1	VSS	L1	B_AD[41]
G2	VSS	J2	B_AD[45]	L2	B_AD[42]
G3	B_NC5	J3	B_AD[46]	L3	VCC15
G4	B_NC8	J4	VSS	L4	B_REQ0#
G5	VSS	J5	B_GNT0#	L5	B_AD[56]
G6	B_CBE6#	J6	B_AD[60]	L6	VCC33
G7	B_CBE7#	J7	B_AD[61]	L7	B_AD[57]
G8	VSS	J8	VCCAPCI1	L8	B_GNT5#
G9	B_CBE4#	J9	VSS	L9	VSS
G10	PERN[7]	J10	VCCPE	L10	VCC15
G11	VSS	J11	VSS	L11	VSS
G12	PERN[3]	J12	VCCPE	L12	VCC15
G13	PETP[3]	J13	VSS	L13	VSS
G14	VSS	J14	VCCPE	L14	VCC15
G15	VCCAPE	J15	VSS	L15	VSS
G16	SMBUS[1]	J16	VCC15	L16	VCC15
G17	VSS	J17	A_AD[63]	L17	A_AD[59]
G18	NC11	J18	A_CBE5#	L18	VSS
G19	NC12	J19	VSS	L19	A_AD[58]
G20	VSS	J20	A_PAR64	L20	A_AD[43]
G21	A_NC5	J21	A_AD[47]	L21	VSS
G22	A_NC7	J22	VSS	L22	A_REQ4#
G23	VSS	J23	A_AD[46]	L23	A_AD[42]
G24	A_INTA#	J24	A_GNT1#	L24	VSS
H1	B_AD[48]	K1	B_GNT1#	M1	
H2	B_AD[49]	K2	VSS	M2	B_AD[39]
H3	VCC33	K3	B_AD[43]	M3	B_AD[40]
H4	B_AD[47]	K4	B_AD[44]	M4	VSS
H5	B_AD[62]	K5	VSS	M5	B_AD[54]
H6	VSS	K6	B_AD[58]	M6	B_AD[55]
H7	B_PAR64	K7	B_AD[59]	M7	VSS
H8	B_AD[63]	K8	VSS	M8	NC14
H9	B_CBE5#	K9	VCC15	M9	VCC15
H10	VSS	K10	VSS	M10	VSS
H11	VCCPE	K11	VCC15	M11	VCC15
H12	PERP[3]	K12	VSS	M12	VSS
H13	PETN[3]	K13	VCC15	M13	VCC15
H14	VSS	K14	VSS	M14	VSS
H15	VCCPE	K15	VCC15	M15	VCC15
H16	RSTIN#	K16	VSS	M16	VSS
H17	A_CBE4#	K17	A_AD[61]	M17	A_AD[57]
H18	VCC33	K18	A_AD[60]	M18	A_AD[56]
H19	A_CBE6#	K19	A_AD[62]	M19	VCC33
H20	A_CBE7#	K20	VSS	M20	NC15
H21	VCC33	K21	NC13	M21	A_AD[41]
H22	A_AD[49]	K22	A_AD[45]	M22	VCC15
H23	A_AD[48]	K23	VSS	M23	A_AD[40]
H24	VCC33	K24	A_AD[44]	M24	

Table 31. Signal List, sorted by Ball Name (Sheet 3 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N1		R1	VSS	U1	B_M66EN
N2	VSS	R2	B_AD[32]	U2	B_PERR#
N3	B_AD[37]	R3	B_AD[33]	U3	VSS
N4	B_AD[38]	R4	VSS	U4	B_FRAME#
N5	VSS	R5	B_PME#	U5	B_IRDY#
N6	B_AD[52]	R6	NC16	U6	VSS
N7	B_AD[53]	R7	VCC33	U7	B_CLKO[5]
N8	B_RST#	R8	VCCAPCI2	U8	B_CLKO[6]
N9	VSS	R9	VSS	U9	VCC33
N10	VCC15	R10	VCC15	U10	B_CLKIN
N11	VSS	R11	VSS	U11	B_STRAP3
N12	VCC15	R12	VCC15	U12	VSS
N13	VSS	R13	VSS	U13	A_CLKIN
N14	VCC15	R14	VCC15	U14	A_CLKO[4]
N15	VSS	R15	VSS	U15	VSS
N16	VCC15	R16	VCC15	U16	A_CLKO[5]
N17	A_AD[55]	R17	VCCAPCI3	U17	A_CLKO[3]
N18	A_REQ3#	R18	A_AD[51]	U18	VSS
N19	A_AD[54]	R19	VSS	U19	A_STOP#
N20	VSS	R20	A_AD[50]	U20	A_DEVSEL#
N21	A_AD[39]	R21	A_LOCK#	U21	VSS
N22	A_AD[38]	R22	VSS	U22	A_TRDY#
N23	VSS	R23	A_AD[35]	U23	A_GNT5#
N24		R24	A_AD[34]	U24	VSS
P1	B_AD[34]	T1	B_REQ3#	V1	VSS
P2	B_133EN	T2	VSS	V2	B_SERR#
P3	VSS	T3	B_DEVSEL#	V3	B_STOP#
P4	B_AD[35]	T4	NC10	V4	VCC33
P5	B_AD[36]	T5	VCC33	V5	B_REQ4#
P6	VSS	T6	B_REQ2#	V6	B_CLKO[4]
P7	B_AD[50]	T7	B_CLKO[3]	V7	VSS
P8	B_AD[51]	T8	VSS	V8	B_CLKO[2]
P9	VCC15	T9	VCC15	V9	B_CLKO[1]
P10	VSS	T10	VSS	V10	VSS
P11	VCC15	T11	VCC15	V11	RCOMP
P12	VSS	T12	VSS	V12	VCC15
P13	VCC15	T13	VCC15	V13	VSS
P14	VSS	T14	VSS	V14	A_CLKO[0]
P15	VCC15	T15	VCC15	V15	A_CLKO[6]
P16	VSS	T16	VSS	V16	VCC15
P17	A_AD[53]	T17	VCC33	V17	A_CLKO[2]
P18	VSS	T18	A_M66EN	V18	A_REQ2#
P19	A_AD[52]	T19	A_SERR#	V19	VSS
P20	A_PERR#	T20	VCC33	V20	A_133EN
P21	VSS	T21	A_AD[33]	V21	A_PME#
P22	A_AD[37]	T22	A_AD[32]	V22	VSS
P23	A_AD[36]	T23	VCC33	V23	A_FRAME#
P24	VSS	T24	NC17	V24	A_IRDY#

Table 31. Signal List, sorted by Ball Name (Sheet 4 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
W1	B_AD[16]	AA1	VCC33	AC1	B_REQ64#
W2	VCC33	AA2	B_AD[18]	AC2	B_AD[0]
W3	B_LOCK#	AA3	B_AD[19]	AC3	VCC15
W4	B_TRDY#	AA4	VSS	AC4	B_AD[4]
W5	VSS	AA5	B_CBE3#	AC5	B_AD[5]
W6	B_AD[23]	AA6	B_AD[24]	AC6	VCC33
W7	B_AD[25]	AA7	VSS	AC7	B_AD[9]
W8	VSS	AA8	B_AD[28]	AC8	B_CBE0#
W9	B_AD[29]	AA9	B_AD[31]	AC9	VSS
W10	B_CLKO[0]	AA10	VSS	AC10	B_AD[14]
W11	VCC33	AA11	B_GNT3#	AC11	B_PAR
W12	B_GNT4#	AA12	B_REQ5#	AC12	VSS
W13	A_REQ5#	AA13	VSS	AC13	A_AD[15]
W14	VSS	AA14	A_GNT4#	AC14	A_CBE1#
W15	A_AD[30]	AA15	A_AD[31]	AC15	VSS
W16	A_CLKO[1]	AA16	VSS	AC16	A_AD[11]
W17	VSS	AA17	A_RST#	AC17	A_AD[9]
W18	A_AD[25]	AA18	A_AD[26]	AC18	VSS
W19	A_GNT0#	AA19	VSS	AC19	A_AD[7]
W20	VSS	AA20	A_CBE3#	AC20	A_AD[5]
W21	A_REQ0#	AA21	A_AD[21]	AC21	VSS
W22	A_REQ1#	AA22	VSS	AC22	A_AD[2]
W23	VSS	AA23	A_AD[18]	AC23	A_AD[0]
W24	A_AD[16]	AA24	A_CBE2#	AC24	A_REQ64#
Y1	B_CBE2#	AB1	B_ACK64#	AD1	VSS
Y2	B_AD[17]	AB2	VSS	AD2	B_AD[1]
Y3	VSS	AB3	B_AD[20]	AD3	B_AD[2]
Y4	B_AD[21]	AB4	B_AD[3]	AD4	VSS
Y5	B_AD[22]	AB5	VSS	AD5	B_AD[6]
Y6	VCC15	AB6	B_REQ1#	AD6	B_AD[7]
Y7	B_AD[26]	AB7	B_AD[8]	AD7	VSS
Y8	B_AD[27]	AB8	VCC33	AD8	B_AD[10]
Y9	VCC33	AB9	B_AD[11]	AD9	B_AD[12]
Y10	B_AD[30]	AB10	B_AD[13]	AD10	VSS
Y11	B_GNT2#	AB11	VSS	AD11	B_AD[15]
Y12	VSS	AB12	B_CBE1#	AD12	
Y13	A_GNT3#	AB13	A_PAR	AD13	
Y14	A_GNT2#	AB14	VCC33	AD14	A_AD[14]
Y15	VCC33	AB15	A_AD[12]	AD15	A_AD[13]
Y16	A_AD[28]	AB16	A_AD[29]	AD16	VSS
Y17	A_AD[27]	AB17	VSS	AD17	A_AD[10]
Y18	VSS	AB18	A_AD[8]	AD18	A_CBE0#
Y19	A_AD[23]	AB19	A_AD[24]	AD19	VCC33
Y20	A_AD[22]	AB20	VCC15	AD20	A_AD[6]
Y21	VCC33	AB21	A_AD[3]	AD21	A_AD[4]
Y22	A_AD[19]	AB22	A_AD[20]	AD22	VSS
Y23	A_AD[17]	AB23	VSS	AD23	A_AD[1]
Y24	VCC33	AB24	A_ACK64#	AD24	VSS

4.4 Signal List, sorted by Signal Name

Table 32. Signal List, sorted by Signal Name (Sheet 1 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
V20	A_133EN	J23	A_AD[46]	A23	A_NC2
AB24	A_ACK64#	J21	A_AD[47]	D24	A_NC3
AC23	A_AD[0]	H23	A_AD[48]	F23	A_NC4
AD23	A_AD[1]	H22	A_AD[49]	G21	A_NC5
AC22	A_AD[2]	R20	A_AD[50]	D22	A_NC6
AB21	A_AD[3]	R18	A_AD[51]	G22	A_NC7
AD21	A_AD[4]	P19	A_AD[52]	E22	A_NC8
AC20	A_AD[5]	P17	A_AD[53]	F21	A_NC9
AD20	A_AD[6]	N19	A_AD[54]	E21	A_NC10
AC19	A_AD[7]	N17	A_AD[55]	R21	A_LOCK#
AB18	A_AD[8]	M18	A_AD[56]	T18	A_M66EN
AC17	A_AD[9]	M17	A_AD[57]	AB13	A_PAR
AD17	A_AD[10]	L19	A_AD[58]	J20	A_PAR64
AC16	A_AD[11]	L17	A_AD[59]	E17	A_PCIXCAP
AB15	A_AD[12]	K18	A_AD[60]	P20	A_PERR#
AD15	A_AD[13]	K17	A_AD[61]	V21	A_PME#
AD14	A_AD[14]	K19	A_AD[62]	W21	A_REQ0#
AC13	A_AD[15]	J17	A_AD[63]	W22	A_REQ1#
W24	A_AD[16]	AD18	A_CBE0#	V18	A_REQ2#
Y23	A_AD[17]	AC14	A_CBE1#	N18	A_REQ3#
AA23	A_AD[18]	AA24	A_CBE2#	L22	A_REQ4#
Y22	A_AD[19]	AA20	A_CBE3#	W13	A_REQ5#
AB22	A_AD[20]	H17	A_CBE4#	AC24	A_REQ64#
AA21	A_AD[21]	J18	A_CBE5#	AA17	A_RST#
Y20	A_AD[22]	H19	A_CBE6#	T19	A_SERR#
Y19	A_AD[23]	H20	A_CBE7#	U19	A_STOP#
AB19	A_AD[24]	U13	A_CLKIN	C18	A_STRAP0
W18	A_AD[25]	V14	A_CLKO[0]	D18	A_STRAP1
AA18	A_AD[26]	W16	A_CLKO[1]	B22	A_STRAP2
Y17	A_AD[27]	V17	A_CLKO[2]	C19	A_STRAP3
Y16	A_AD[28]	U17	A_CLKO[3]	A21	A_STRAP4
AB16	A_AD[29]	U14	A_CLKO[4]	D19	A_STRAP5
W15	A_AD[30]	U16	A_CLKO[5]	F19	A_STRAP6
AA15	A_AD[31]	V15	A_CLKO[6]	F22	A_TEST1
T22	A_AD[32]	U20	A_DEVSEL#	B23	A_TEST2
T21	A_AD[33]	V23	A_FRAME#	U22	A_TRDY#
R24	A_AD[34]	W19	A_GNT0#	P2	B_133EN
R23	A_AD[35]	J24	A_GNT1#	AB1	B_ACK64#
P23	A_AD[36]	Y14	A_GNT2#	AC2	B_AD[0]
P22	A_AD[37]	Y13	A_GNT3#	AD2	B_AD[1]
N22	A_AD[38]	AA14	A_GNT4#	AD3	B_AD[2]
N21	A_AD[39]	U23	A_GNT5#	AB4	B_AD[3]
M23	A_AD[40]	V24	A_IRDY#	AC4	B_AD[4]
M21	A_AD[41]	G24	A_INTA#	AC5	B_AD[5]
L23	A_AD[42]	F24	A_INTB#	AD5	B_AD[6]
L20	A_AD[43]	D23	A_INTC#	AD6	B_AD[7]
K24	A_AD[44]	C24	A_INTD#	AB7	B_AD[8]
K22	A_AD[45]	B24	A_NC1	AC7	B_AD[9]

Table 32. Signal List, sorted by Signal Name (Sheet 2 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AD8	B_AD[10]	K6	B_AD[58]	H7	B_PAR64
AB9	B_AD[11]	K7	B_AD[59]	D7	B_PCIXCAP
AD9	B_AD[12]	J6	B_AD[60]	U2	B_PERR#
AB10	B_AD[13]	J7	B_AD[61]	R5	B_PME#
AC10	B_AD[14]	H5	B_AD[62]	L4	B_REQ0#
AD11	B_AD[15]	H8	B_AD[63]	AB6	B_REQ1#
W1	B_AD[16]	AC8	B_CBE0#	T6	B_REQ2#
Y2	B_AD[17]	AB12	B_CBE1#	T1	B_REQ3#
AA2	B_AD[18]	Y1	B_CBE2#	V5	B_REQ4#
AA3	B_AD[19]	AA5	B_CBE3#	AA12	B_REQ5#
AB3	B_AD[20]	G9	B_CBE4#	AC1	B_REQ64#
Y4	B_AD[21]	H9	B_CBE5#	N8	B_RST#
Y5	B_AD[22]	G6	B_CBE6#	V2	B_SERR#
W6	B_AD[23]	G7	B_CBE7#	V3	B_STOP#
AA6	B_AD[24]	U10	B_CLKIN	A19	B_STRAP0
W7	B_AD[25]	W10	B_CLKO[0]	B3	B_STRAP1
Y7	B_AD[26]	V9	B_CLKO[1]	B19	B_STRAP2
Y8	B_AD[27]	V8	B_CLKO[2]	U11	B_STRAP3
AA8	B_AD[28]	T7	B_CLKO[3]	E6	B_STRAP4
W9	B_AD[29]	V6	B_CLKO[4]	A2	B_STRAP5
Y10	B_AD[30]	U7	B_CLKO[5]	B5	B_STRAP6
AA9	B_AD[31]	U8	B_CLKO[6]	C3	B_TEST1
R2	B_AD[32]	T3	B_DEVSEL#	D1	B_TEST2
R3	B_AD[33]	U4	B_FRAME#	W4	B_TRDY#
P1	B_AD[34]	J5	B_GNT0#	B8	CFGRETRY
P4	B_AD[35]	K1	B_GNT1#	E18	CFGRST#
P5	B_AD[36]	Y11	B_GNT2#	F18	NC1
N3	B_AD[37]	AA11	B_GNT3#	A5	NC2
N4	B_AD[38]	W12	B_GNT4#	A22	NC3
M2	B_AD[39]	L8	B_GNT5#	C4	NC4
M3	B_AD[40]	U5	B_IRDY#	D6	NC5
L1	B_AD[41]	F2	B_INTA#	E19	NC6
L2	B_AD[42]	G1	B_INTB#	F6	NC7
K3	B_AD[43]	F3	B_INTC#	F8	NC8
K4	B_AD[44]	C1	B_INTD#	F7	NC9
J2	B_AD[45]	B2	B_NC1	T4	NC10
J3	B_AD[46]	E4	B_NC2	G18	NC11
H4	B_AD[47]	D2	B_NC3	G19	NC12
H1	B_AD[48]	E1	B_NC4	K21	NC13
H2	B_AD[49]	G3	B_NC5	M8	NC14
P7	B_AD[50]	D3	B_NC6	M20	NC15
P8	B_AD[51]	B1	B_NC7	R6	NC16
N6	B_AD[52]	G4	B_NC8	T24	NC17
N7	B_AD[53]	E3	B_NC9	C6	NC18
M5	B_AD[54]	F4	B_NC10	B6	NC19
M6	B_AD[55]	W3	B_LOCK#	E16	PE_RCOMP[0]
L5	B_AD[56]	U1	B_M66EN	B17	PE_RCOMP[1]
L7	B_AD[57]	AC11	B_PAR	E14	PERN[0]

Table 32. Signal List, sorted by Signal Name (Sheet 3 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A15	PERN[1]	A18	SMBUS[3]	F1	VCC33
C13	PERN[2]	D20	SMBUS[5]	H3	VCC33
G12	PERN[3]	B7	TCK	H18	VCC33
C10	PERN[4]	E9	TDI	H21	VCC33
C9	PERN[5]	A6	TDO	H24	VCC33
E12	PERN[6]	E7	TMS	L6	VCC33
G10	PERN[7]	F9	TRST#	M19	VCC33
E15	PERP[0]	J16	VCC15	R7	VCC33
A16	PERP[1]	K9	VCC15	T5	VCC33
D13	PERP[2]	K11	VCC15	T17	VCC33
H12	PERP[3]	K13	VCC15	T20	VCC33
C11	PERP[4]	K15	VCC15	T23	VCC33
B9	PERP[5]	L3	VCC15	U9	VCC33
D12	PERP[6]	L10	VCC15	V4	VCC33
F10	PERP[7]	L12	VCC15	W2	VCC33
F17	PERST#	L14	VCC15	W11	VCC33
F13	PETN[0]	L16	VCC15	Y9	VCC33
D15	PETN[1]	M9	VCC15	Y15	VCC33
B14	PETN[2]	M11	VCC15	Y21	VCC33
H13	PETN[3]	M13	VCC15	Y24	VCC33
B11	PETN[4]	M15	VCC15	AA1	VCC33
A9	PETN[5]	M22	VCC15	AB8	VCC33
D9	PETN[6]	N10	VCC15	AB14	VCC33
F11	PETN[7]	N12	VCC15	AC6	VCC33
F14	PETP[0]	N14	VCC15	AD19	VCC33
D16	PETP[1]	N16	VCC15	J8	VCCAPCI1
B15	PETP[2]	P9	VCC15	R8	VCCAPCI2
G13	PETP[3]	P11	VCC15	R17	VCCAPCI3
B12	PETP[4]	P13	VCC15	G15	VCCAPE
A10	PETP[5]	P15	VCC15	C14	VCCBGPE
D10	PETP[6]	R10	VCC15	A14	VCCPE
E11	PETP[7]	R12	VCC15	C12	VCCPE
V11	RCOMP	R14	VCC15	C15	VCCPE
C17	REFCLKN	R16	VCC15	F12	VCCPE
C16	REFCLKP	T9	VCC15	H11	VCCPE
C21	RESERVED1	T11	VCC15	H15	VCCPE
B21	RESERVED2	T13	VCC15	J10	VCCPE
D21	RESERVED3	T15	VCC15	J12	VCCPE
F20	RESERVED4	V12	VCC15	J14	VCCPE
A3	RESERVED5	V16	VCC15	A4	VSS
B4	RESERVED6	Y6	VCC15	A8	VSS
D4	RESERVED7	AB20	VCC15	A17	VSS
F5	RESERVED8	AC3	VCC15	A20	VSS
H16	RSTIN#	A7	VCC33	A24	VSS
C7	SMBCLK	B18	VCC33	B10	VSS
D8	SMBDAT	C22	VCC33	B13	VSS
G16	SMBUS[1]	D5	VCC33	B16	VSS
B20	SMBUS[2]	E24	VCC33	C2	VSS

Table 32. Signal List, sorted by Signal Name (Sheet 4 of 4)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
C5	VSS	L21	VSS	V10	VSS
C8	VSS	L24	VSS	V13	VSS
C20	VSS	M4	VSS	V19	VSS
C23	VSS	M7	VSS	V22	VSS
D11	VSS	M10	VSS	W5	VSS
D14	VSS	M12	VSS	W8	VSS
D17	VSS	M14	VSS	W14	VSS
E2	VSS	M16	VSS	W17	VSS
E5	VSS	N2	VSS	W20	VSS
E8	VSS	N5	VSS	W23	VSS
E10	VSS	N9	VSS	Y3	VSS
E13	VSS	N11	VSS	Y12	VSS
E20	VSS	N13	VSS	Y18	VSS
E23	VSS	N15	VSS	AA4	VSS
F15	VSS	N20	VSS	AA7	VSS
G2	VSS	N23	VSS	AA10	VSS
G5	VSS	P3	VSS	AA13	VSS
G8	VSS	P6	VSS	AA16	VSS
G11	VSS	P10	VSS	AA19	VSS
G14	VSS	P12	VSS	AA22	VSS
G17	VSS	P14	VSS	AB2	VSS
G20	VSS	P16	VSS	AB5	VSS
G23	VSS	P18	VSS	AB11	VSS
H6	VSS	P21	VSS	AB17	VSS
H10	VSS	P24	VSS	AB23	VSS
H14	VSS	R1	VSS	AC9	VSS
J1	VSS	R4	VSS	AC12	VSS
J4	VSS	R9	VSS	AC15	VSS
J9	VSS	R11	VSS	AC18	VSS
J11	VSS	R13	VSS	AC21	VSS
J13	VSS	R15	VSS	AD1	VSS
J15	VSS	R19	VSS	AD4	VSS
J19	VSS	R22	VSS	AD7	VSS
J22	VSS	T2	VSS	AD10	VSS
K2	VSS	T8	VSS	AD16	VSS
K5	VSS	T10	VSS	AD22	VSS
K8	VSS	T12	VSS	AD24	VSS
K10	VSS	T14	VSS	F16	VSSAPE
K12	VSS	T16	VSS	A13	VSSBGPE
K14	VSS	U3	VSS	A1	
K16	VSS	U6	VSS	A11	
K20	VSS	U12	VSS	A12	
K23	VSS	U15	VSS	M1	
L9	VSS	U18	VSS	M24	
L11	VSS	U21	VSS	N1	
L13	VSS	U24	VSS	N24	
L15	VSS	V1	VSS	AD12	
L18	VSS	V7	VSS	AD13	

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