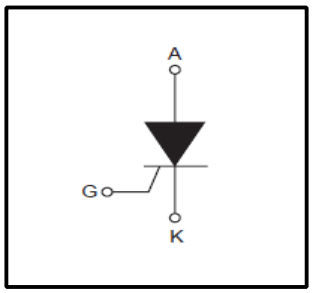
WCP8C60S

Silicon Controlled Rectifiers

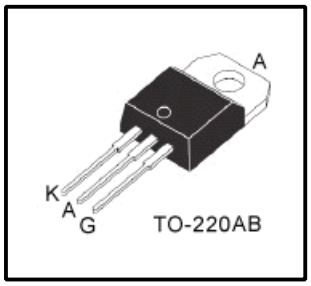
Features

- Sensitive gate trigger current:I_{GT}=200uA maximum
- Low On-State Voltage :V_{TM}=1.2(typ.) @ I_{TM})
- Low reverse and forward blocking current: I_{DRM}/I_{RRM}=2mA@TC=125℃
- Low holding current :I_H=5mA maximum



General Description

Sensitive gate triggering SCR is suitable for the application where gate current limited such as microcontrollers, logic integrated circuits,small motor control, gate driver for large SCR,sensing and detecting circuits.general purpose switching and phase control applications



Absolute Maximum Ratings (T_J= 25°C unless otherwise specified)

Symbol	Parameter		Value	Units
V_{DRM}/V_{RRM}	Repetitive Peak Off-State Voltage	(Note(1)	600	V
$I_{T(AV)}$	Average On-State Current(180° Conduction Angle)	T_l =85 °C	5	A
$I_{T(RMS)}$	R.M.S On-State Current(180° Conduction Angle)	T_l =85 °C	8	A
I_{TSM}	Non Repetitive Surge Peak on-state Current	tp=8.3ms	73	A
		tp=10ms	70	
I^2t	I^2t Valuefor Fusing	tp=8.3ms	24.5	A^2s
di/dt	Critical rate of rise of on-state current I_{TM}=2A;IG=10mA; dI_G/dt=100A/μs	T_J=125 °C	50	A/μs
$P_{G(AV)}$	Average Gate Power Dissipation	T_J=125 °C	1	W
I_{FGM}	Peak Gate Current	T_J=125 °C	4	A
V_{RGM}	Reverse Peak Gate Voltage	T_J=125 °C	5	V
T_J	Junction Temperature		-40~125	°C
T_{STG}	Storage Temperature		-40~150	°C

Note1: Although not recommended,off-state Voltages up to 800V may be applied without damage,but the thyristor may switch to the on-stage.The rate of rise of current should not exceed15A/μs.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta Jc}$	Thermal Resistance Junction to Case	-	-	20	℃/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	-	-	70	℃/W

Electrical Characteristics (T_J=25℃ ,R_{GK}=1KΩ unless otherwise specified)

Symbol	Characteristics		Value			Units
			Min	**Typ**	**Max**	
I_{DRM}/I_{RRM}	Off-state leakage current ($V_{AK}=V_{DRM}/V_{RRM}$)	T_C=25℃	-	-	5	μA
		T_C=125℃			2	mA
V_{TM}	Forward "On"voltage (I_{TM}=16A tp=380μs) (Note2.1)		-	1.2	1.6	V
I_{GT}	Gate Trigger Current(continuous dc) (V_{AK}=12Vdc,R_L=140Ω) (Note2.2)		15	-	200	mA
V_{GT}	Gate Trigger Voltage (continuous dc) (V_{AK}=12Vdc,R_L=140Ω) (Note2.2)		-	-	0.8	V
V_{GD}	Gate threshold Voltage (V_D=12V_{DRM} RL=3.3KΩ R_{GK}=220Ω) (Note2.1)		0.1	-	-	V
dv/dt	Critical Rate of Rise Off-State Voltage (V_D=0.67V_{DRM}; R_{GK}=220Ω)	T_J=125℃	5	-	-	V/μs
I_H	Holding Current(V_D=12V;I_{GT}=0.5mA)		-	2	5	mA
I_L	Latching Current(V_D=12V;I_{GT}=0.5mA)		-	2	6	mA
Rd	Dynamic resistance	T_J=125℃	-	-	46	mΩ

***Notes:**

2.1 Pulse Width ≤1.0ms,Duty cycle≤1%

2.2 R_{GK} Current is not Included in measurement.

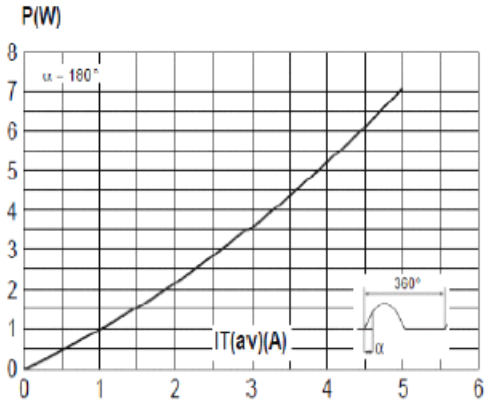


Fig.1*Maximum average power dissipation versus average on-state current*

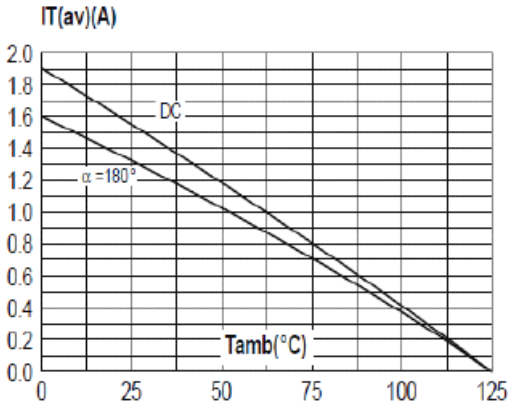


Fig .2 *Average and D.C.on-state current versus ambient temperature (device mounted on FR4 with recommended pad layont*

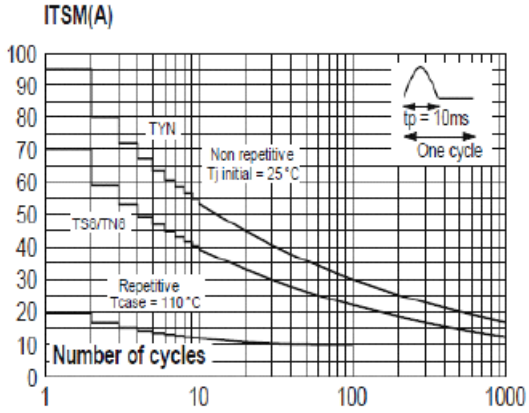


Fig. 3*Surge peak on-state current versus Number of cycles.*

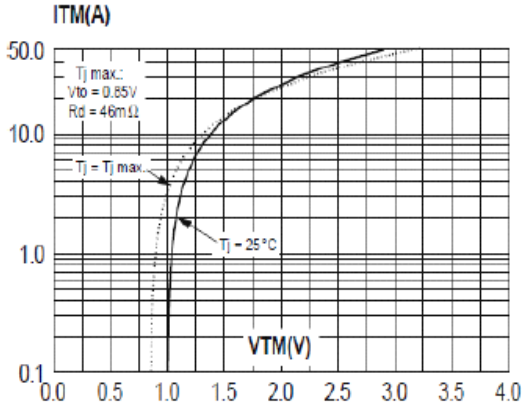


Fig. 4*On-state Characteristics (maximum values)*

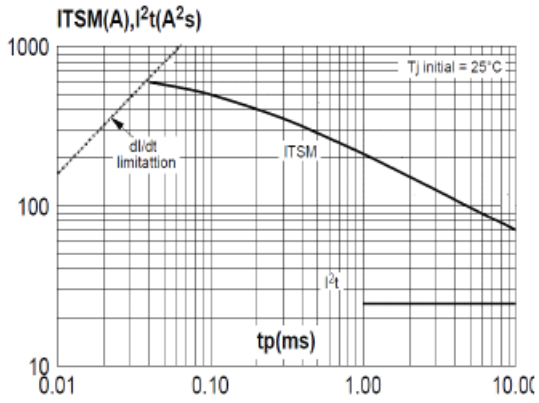


Fig.5*Non-repetitive surge peak on-state current for a sinusoidal pulse with width Tp<10ms and corresponding value of I²t*

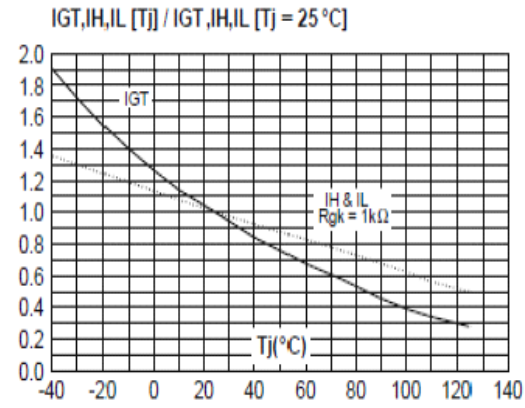


Fig.6*Relative variation of gate trigger current and holding versus junction temperature*

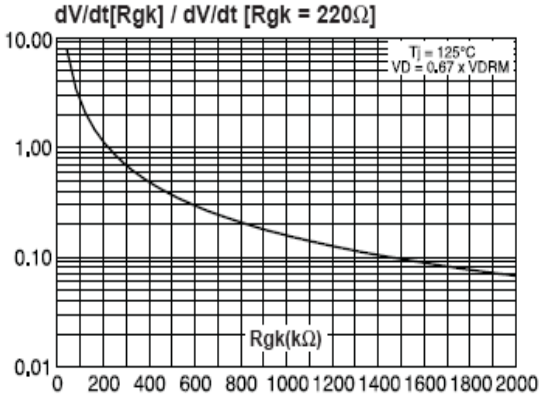


Fig.7*Relative variation of dv/dt immunity versus gate-cathode resistance (typical values)*

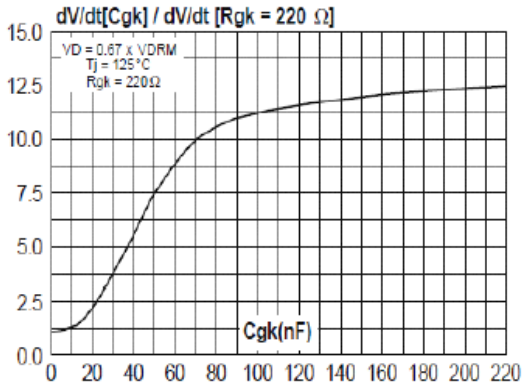


Fig.8*Relative variation of dv/dt immunity versus gate-cathode capacitance (typical values)*

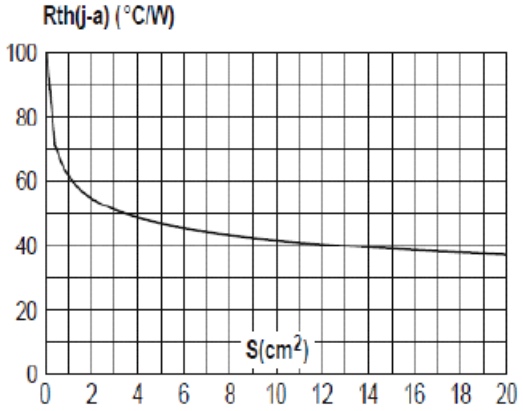


Fig.8*Thermal Resistance junction to ambient Versus copper surface under tab (Epoxy printedCircuit board FR4,copper thickness:35mm)*

TO-220AB Package Dimension

Unit: mm