4.5 V 至 14 V 输入大电流同步降压转换器

查询样品: **TPS56221**

特性

- **4.5 V** 至 **14 V** 输入电压范围
- 整合功率块技术
- 输出电流高达 **25 A**
- **300 kHz**、**500 kHz** 与 **1 MHz** 固定频率选项
- 高侧与低侧 **MOSFET** $\mathbf{R_{DS(on)}}$ 传感
- 可编程软启动
- 误差精度为 **1%** 的 **600 mV** 参考电压
- 前馈电压模式控制
- 支持预偏置输出
- 热关断
- **22** 引脚 **5** 毫米 **x 6** 毫米 **PQFN PowerPAD™** 封装

应用

- 负载点 **(POL)** 电源模块
- 针对电信与网络应用的高密度 **DC-DC** 转换器

说明

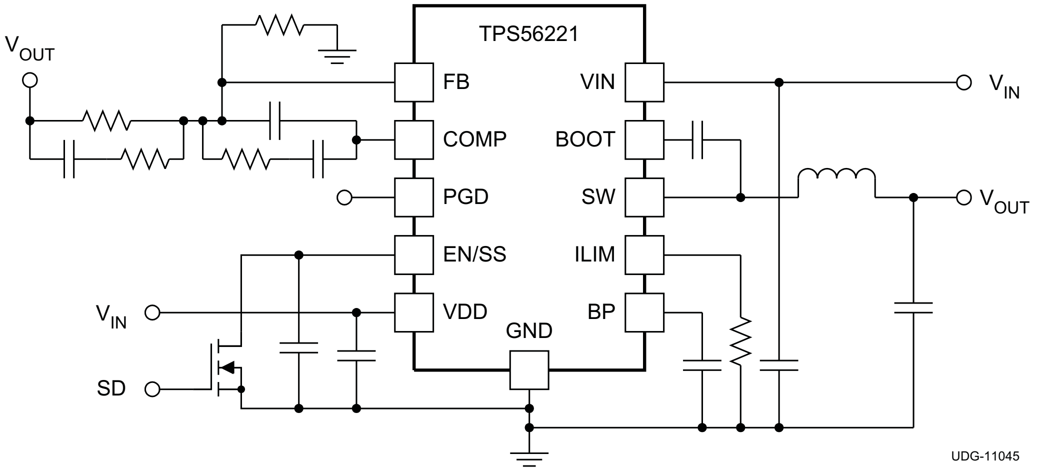
TPS56121 是一款工作电源电压在 4.5 V 与 14 V 之间的高效率大电流同步降压转换器。该器件可在高达 15 A 的负载下产生低至 0.6 V 的输出电压。集成型 NexFET™功率 MOSFET可带来小型化与易用性优势。

该器件可通过电压前馈补偿实施电压模式控制，能够在输入电压变化时立即做出响应。

TPS56121 采用热增强型 22 引脚 PQFN (DQP) PowerPAD ™封装。

该器件支持高度的设计灵活性，可提供各种用户可编程功能，其中包括软启动、过流保护 (OCP) 级以及环路补偿。 OCP 级可通过由 ILIM 引脚连接至电路接地的单个外部电阻器进行编程。 在初始上电排序过程中，该器件可进入校准环节，测量 ILIM 引脚电压，并设置内部l OCP 电压级。 在工作中，可在通电时通过将可编程 OCP 电压级与整个低侧 FET 的电压压降进行比较来判断是否为过流状况。 然后，其可在消除故障后进入关断 / 重启环节。

SIMPLIFIED APPLICATION



PowerPAD, NexFET are trademarks of Texas Instruments.

English Data Sheet: SLUSAH5

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ORDERABLE NUMBER
-40°C to 150°C	Plastic QFN (DQP)	22	Tape-and-reel	250	TPS56221DQPT
				2500	TPS56221DQPR

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	TYP	
Voltage Range	VDD, VIN	–0.3	16.5	V
	SW	–3	25	
	SW (< 100 ns pulse width, 10 µJ)	-5		
	BOOT	–0.3	30	
	BOOT-SW (differential from BOOT to SW)	–0.3	7	
	COMP, PGOOD, FB, BP, EN/SS, ILIM	–0.3	7	
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CBM) QSS 009-147 (JESD22-C101B.01)		1.5	
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS56221	UNITS
		PQFN	
		22 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	34.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	22.9	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	5.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	VIN Input voltage	4.5		14	V
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE						
V_{FB}	FB input voltage	T_J = 25°C, 4.5 V ≤ V_{VDD} ≤ 14 V	597	600	603	mV
		–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{VDD} ≤ 14 V	594	600	606	
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		14	V
$IVDD_{SD}$	Shutdown supply current	$V_{EN/SS}$ = 0.2 V		80	120	µA
$IVDD_{Q}$	Quiescent, non-switching	Let EN/SS float, V_{FB} = 1 V		2.5	5.0	mA
V_{UVLO}	UVLO ON Voltage		4.0		4.3	V
$V_{UVLO(HYS)}$	UVLO hysteresis		500		700	mV
ENABLE/SOFT-START						
V_{IH}	High-level input voltage, EN/SS		0.55	0.70	1.00	V
V_{IL}	Low-level input voltage, EN/SS		0.27	0.30	0.33	V
I_{SS}	Soft-start source current		8	10	12	µA
V_{SS}	Soft-start voltage level – Start of ramp		0.4	0.8	1.3	V
BP REGULATOR						
V_{BP}	Output voltage	I_{BP} = 10 mA	6.2	6.5	6.8	V
V_{DO}	Regulator dropout voltage, $V_{VDD} – V_{BP}$	I_{BP} = 25 mA, V_{VDD} = 4.5 V		70	125	mV
OSCILLATOR						
f_{SW}	Switching Frequency	R_{COMP} = 40.2 kΩ, 4.5 V ≤ V_{VDD} ≤ 14 V	270	300	330	kHz
		R_{COMP} = open, 4.5 V ≤ V_{VDD} ≤ 14 V	450	500	550	kHz
		R_{COMP} = 13.3 kΩ, 4.5 V ≤ V_{VDD} ≤ 14 V	0.8	0.95	1.1	MHz
V_{RAMP} (1)	Ramp amplitude		V_{VDD}/6.6	V_{VDD}/6	V_{VDD}/5.4	V
PWM						
D_{MAX} (1)	Maximum duty cycle	f_{sw} = 300 kHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	93%			
		f_{sw} = 500 kHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	90%			
		f_{sw} = 1 MHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	85%			
$t_{ON(min)}$ (1)	Minimum controllable pulse width				100	ns
ERROR AMPLIFIER						
GBWP (1)	Gain bandwidth product		10	24		MHz
A_OL (1)	Open loop gain		60			dB
I_{IB}	Input bias current (current out of FB pin)	V_{FB} = 0.6 V			75	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1.5			mA
I_{EAOM}	Output sink current	V_{FB} = 1 V	1.5			mA

(1) Ensured by design. Not production tested

PRODUCT PREVIEW

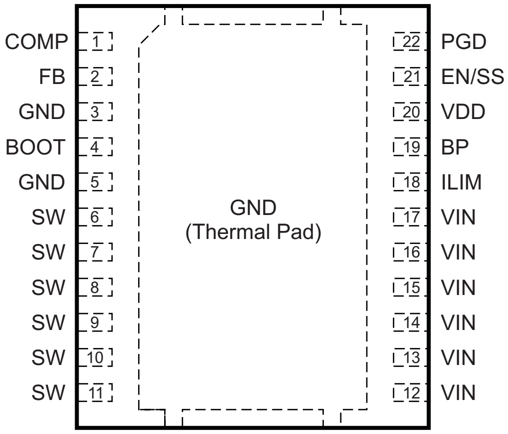
ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD						
V_{OV}	Feedback upper voltage limit for PGOOD		655	675	700	mV
V_{UV}	Feedback lower voltage limit for PGOOD		500	525	550	
$V_{PGD\text{-}HYST}$	PGOOD hysteresis voltage at FB			30	45	
R_{PGD}	PGOOD pull down resistance	V_{FB} = 0 V, I_{FB} = 5 mA		30	70	Ω
I_{PGDLK}	PGOOD leakage current	550 mV < V_{FB} < 655 mV, V_{PGOOD} = 5 V		10	20	µA
OUTPUT STAGE						
R_{HI}	High-side device resistance	T_J = 25°C, (V_{BOOT}– V_{SW}) = 5.5 V		4.5	6.5	mΩ
R_{LO}	Low side device resistance	T_J = 25°C		1.9	2.7	
OVERCURRENT PROTECTION (OCP)						
$t_{PSSC(min)}$ (2)	Minimum pulse time during short circuit			250		ns
t_{BLNKH} (2)	Switch leading-edge blanking pulse time (high-side detection)			150		
I_{OCH}	OC threshold for high-side FET	T_J = 25°C, (V_{BOOT}– V_{SW}) = 5.5 V	45	54	65	A
I_{ILIM}	ILIM current source	T_J = 25°C		10.0		µA
V_{OCLPRO}(2)	Programmable OC range for low side FET	T_J = 25°C	12		100	mV
t_{OFF}	OC retry cycles on EN/SS pin			4		Cycle
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.8		V
THERMAL SHUTDOWN						
T_{JSD} (2)	Junction shutdown temperature			145		ºC
T_{JSDH} (2)	Hysteresis			20		ºC

(2) Ensured by design. Not production tested

DEVICE INFORMATION

DQP PACKAGE
PQFN-22
(TOP VIEW)



Note: The thermal pad is also an electrical ground connection.

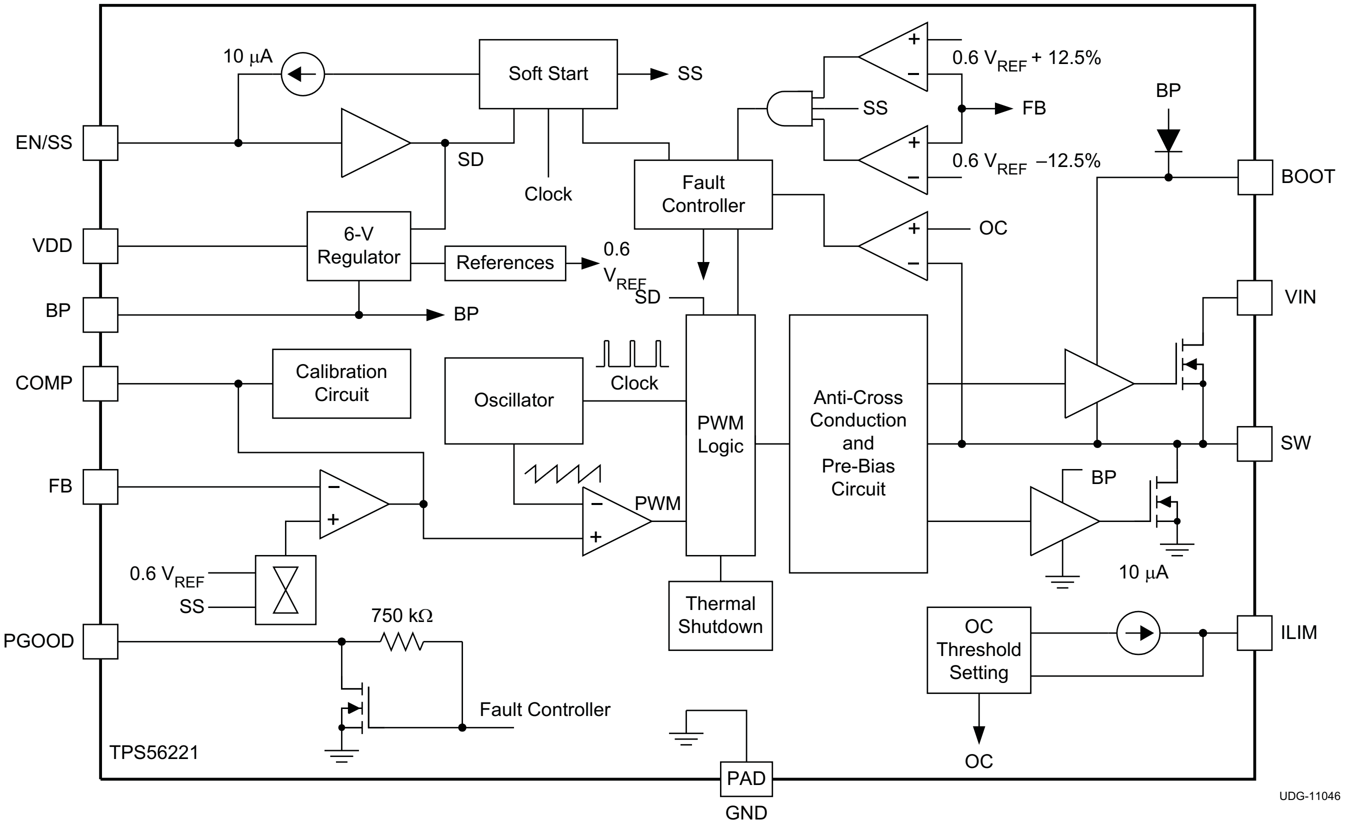
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	**NO.**		
BOOT	4	O	Gate drive voltage for the high-side FET. A 100-nF capacitor (typical) must be connected between this pin and the SW pin. To reduce a voltage spike at SW, a BOOT resistance between 5 Ω to 10 Ω may be placed in series with the BOOT capacitor to slow down start-up of the high-side FET.
BP	19	O	Output bypass for the internal regulator. Connect a low-ESR bypass ceramic capacitor of 1 μF or greater from this pin to GND.
COMP	1	O	Output of the error amplifier and connection node for loop feedback components. Optionally, a 40.2 kΩ resistor from this pin to GND sets switching frequency to 300KHz instead of the default value of 500KHz; while a 13.3 kΩ resistor from this pin to GND sets switching frequency to 1 MHz.
EN/SS	21	I	Logic-level input starts or stops the controller via an external user command. Allowing this pin to float turns the controller on. Pulling this pin low disables the controller. This is also the soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 10 μA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier after a 0.8 V (typical) level shift downwards. Output regulation is controlled by the internal level shifted voltage ramp until that voltage reaches the internal reference voltage of 600 mV. The voltage ramp of this pin reaches 1.4 V (typical).
FB	2	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage.
GND	3	–	Ground reference for the device
	5		
GND	Thermal Pad	–	Ground reference for the device. This is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first is to provide an electrical ground connection for the device. The second is to provide a low thermal impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.
ILIM	18	I	A resistor connected from this pin to GND sets the overcurrent threshold for the device (the low-side FET).
PGD	22	O	Open drain power good output.
SW	6	I	Sense line for the adaptive anti-cross conduction circuitry. Acts as the common connection for the flying high-side FET driver.
	7		
	8		
	9		
	10		
	11		
VDD	20	I	Power input to the controller. A low-ESR bypass ceramic capacitor of 1 μF should be connected from this pin close to GND.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
VIN	12	I	Power input to the high-side FET.
	13		
	14		
	15		
	16		
	17		

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

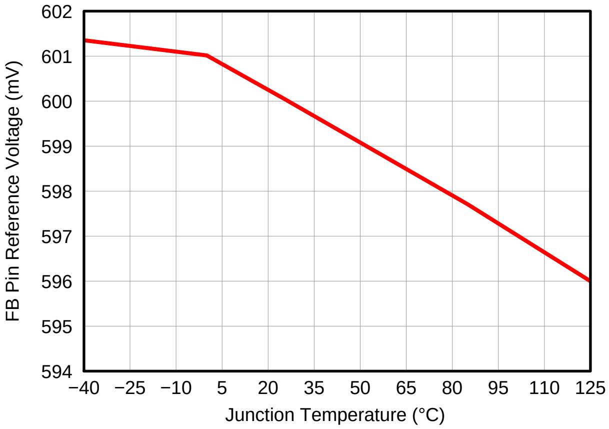


Figure 1. Reference Voltage vs. Junction Temperature

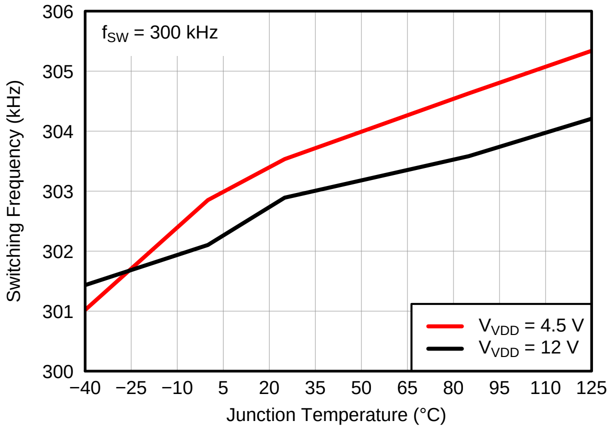


Figure 2. Switching Frequency vs. Junction Temperature (300 kHz)

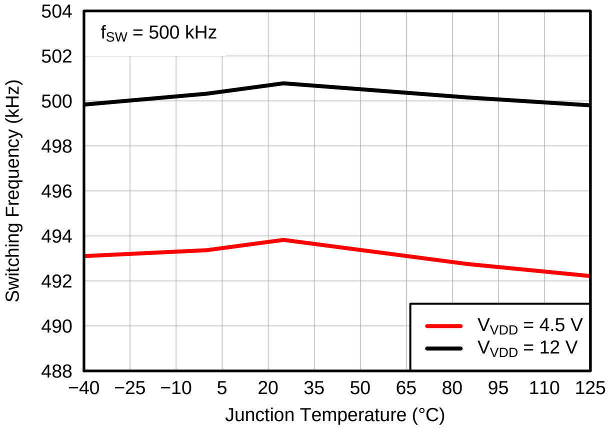


Figure 3. Switching Frequency vs. Junction Temperature (500 kHz)

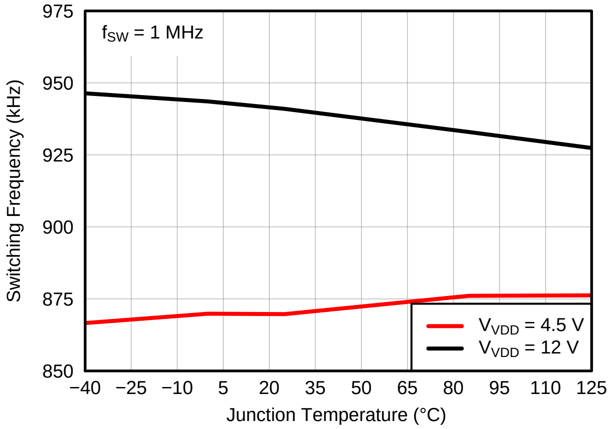


Figure 4. Switching Frequency vs. Junction Temperature (1 MHz)

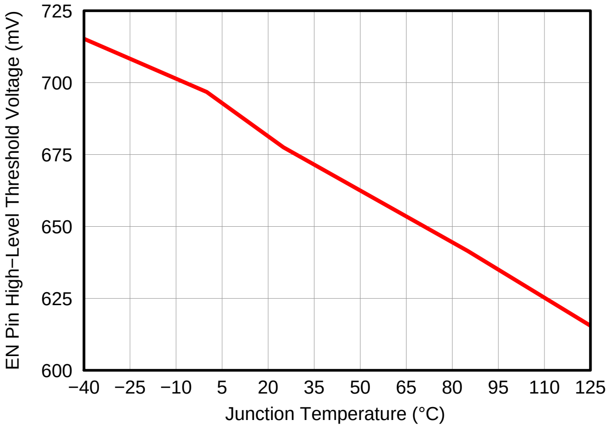


Figure 5. EN Pin High-Level Threshold Voltage vs. Junction Temperature

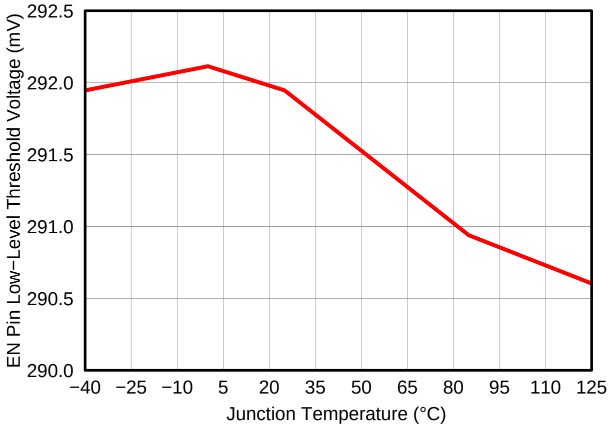


Figure 6. EN Pin Low-Level Threshold Voltage vs. Junction Temperature

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

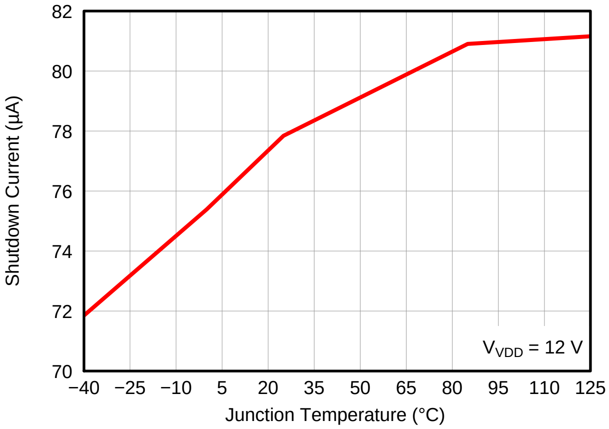


Figure 7. Shutdown Current vs. Junction Temperature

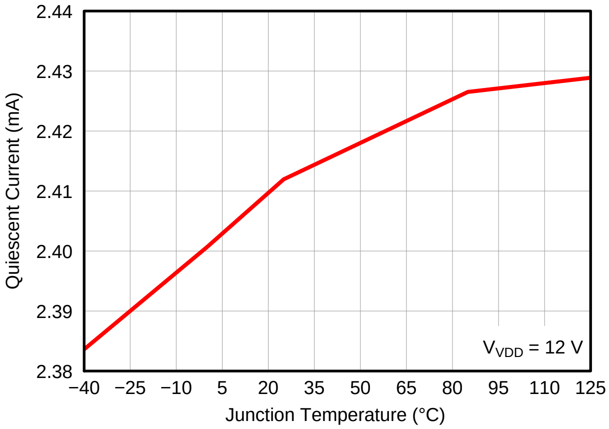


Figure 8. Quiescent Current vs. Junction Temperature

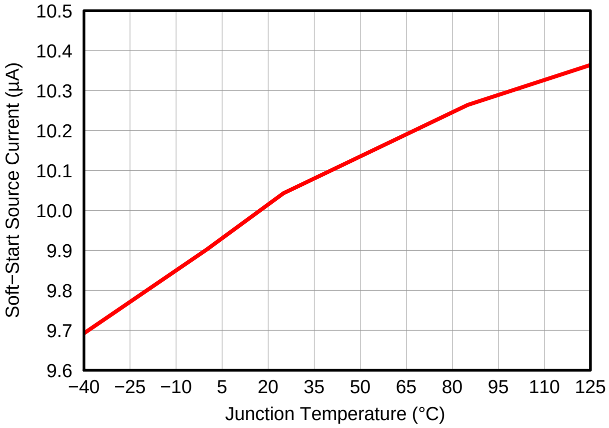


Figure 9. Soft-Start Source vs. Junction Temperature

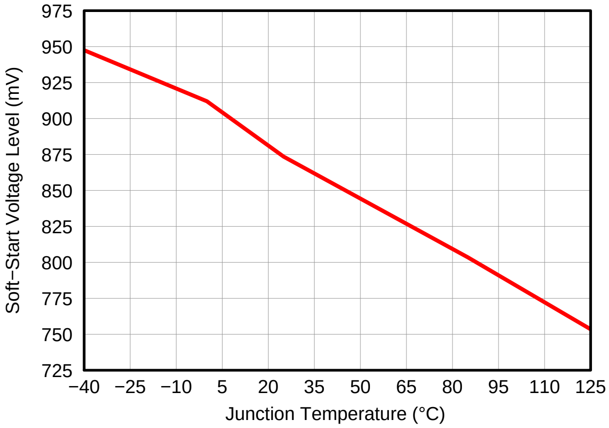


Figure 10. Soft-Start Voltage Level vs. Junction Temperature

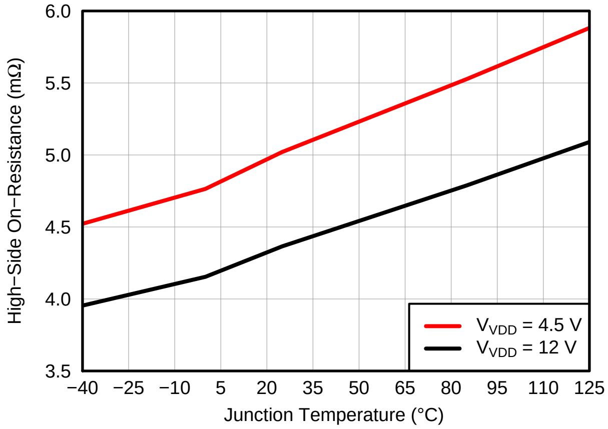


Figure 11. High-Side On Resistance vs. Junction Temperature

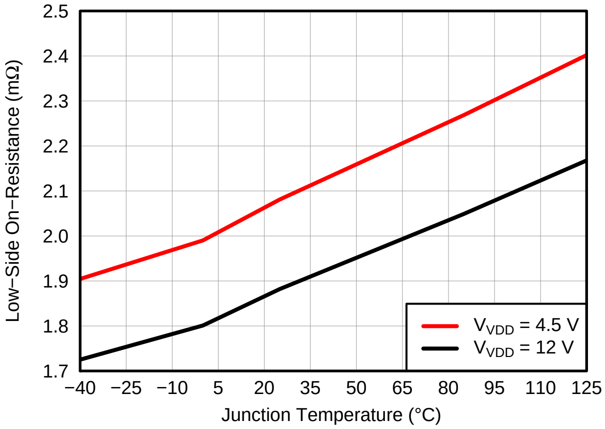


Figure 12. Low-Side On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

The efficiency curve shown in Figure 15 is measured with a 0.5-μH output inductor and a maximum DCR of 0.75 mΩ. The efficiency curve shown in Figure 16 is measured with a 0.3-μH output inductor and a maximum DCR of 0.54 mΩ. The power derating curves shown in Figure 17 and Figure 18 are measured on a 4" × 3.25", 0.062" thick FR4 board with 6 layers and 1 oz. copper.

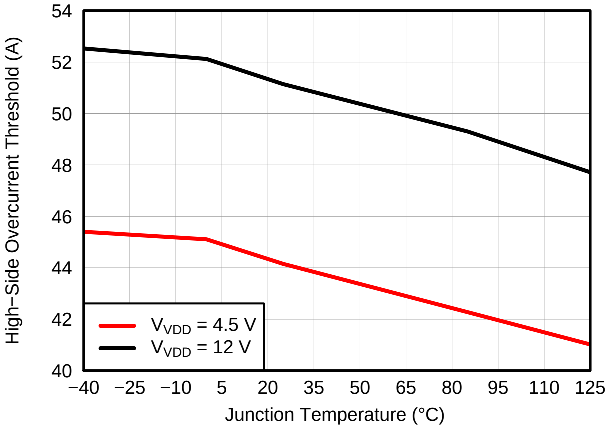


Figure 13. High-Side Overcurrent Threshold vs. Junction Temperature

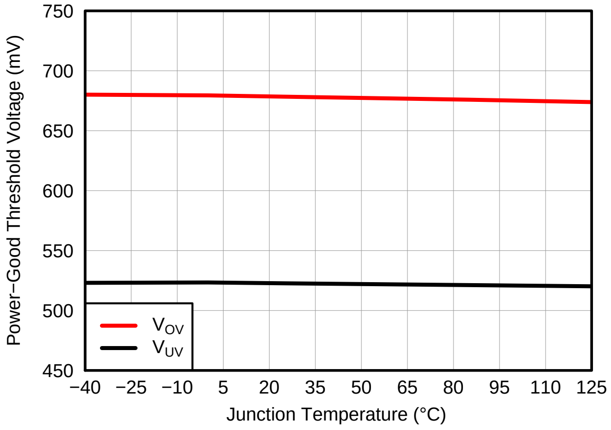


Figure 14. Power Good Threshold Voltage vs. Junction Temperature

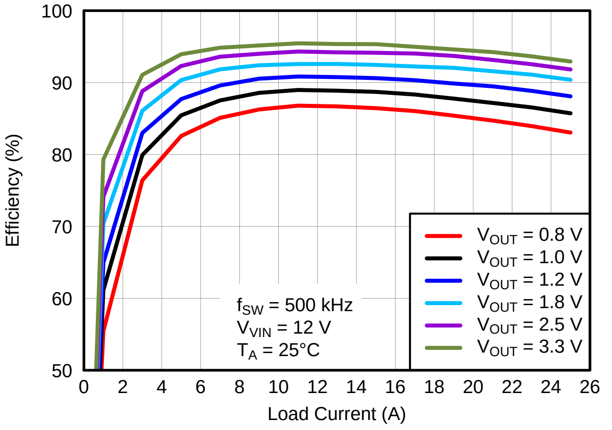


Figure 15. Efficiency vs. Load Current (V_{VIN} = 12 V)

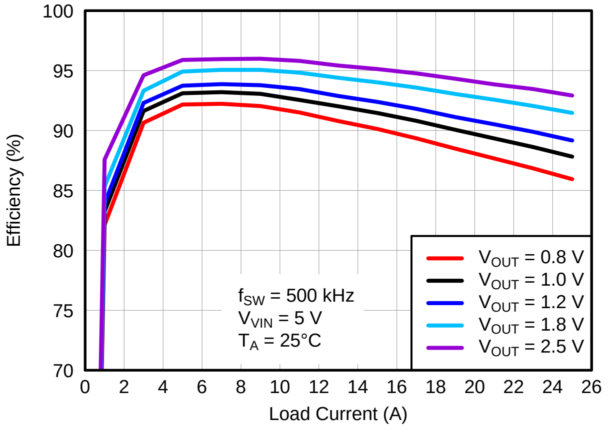


Figure 16. Efficiency vs. Load Current (V_{VIN} = 5 V)

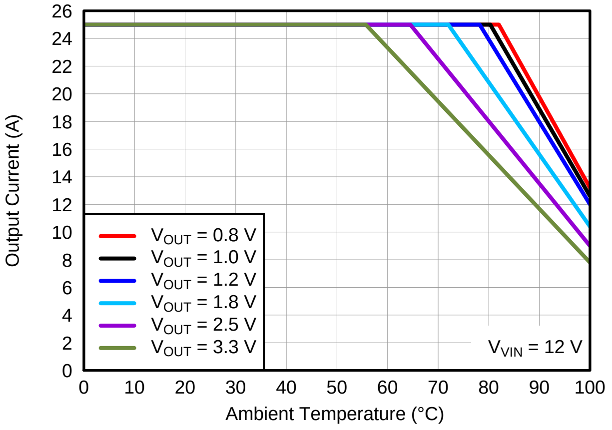


Figure 17. Output Current vs. Ambient Temperature (V_{VIN} = 12 V)

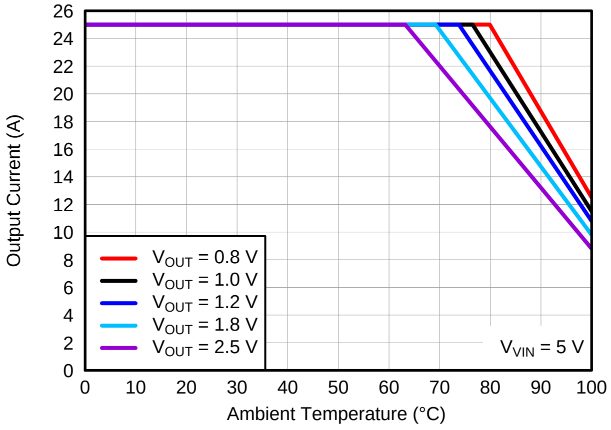


Figure 18. Output Current vs. Ambient Temperature (V_{VIN} = 5 V)

APPLICATION INFORMATION

Introduction

The TPS56221 is a 25-A high performance synchronous buck converter with two integrated N-channel NexFET™ power MOSFETs. The device implements a voltage-mode control with voltage feed-forward compensation that responds instantly to input voltage change. Pre-bias capability eliminates concerns about damaging sensitive loads.

Voltage Reference

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 1% tolerance on the reference voltage allows the user to design a very accurate power supply.

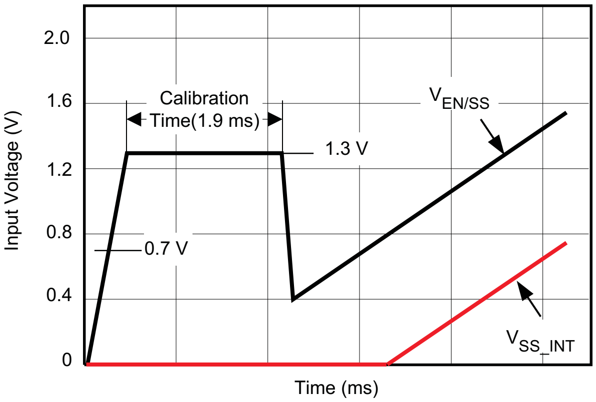


Figure 19. Startup Sequence and Timing

Enable Functionality, Startup Sequence and Timing

After input power is applied, an internal 40-μA current source begins to charge the soft-start capacitor connected from EN/SS to GND. When the voltage across that capacitor increases to 0.7 V, it enables the internal BP regulator followed by a calibration. Total calibration time is approximately 1.9 ms. See Figure 19. During the calibration, the device performs the following two functions.

COMP Pin Impedance Sensing

The device samples the impedance at the COMP pin and determines the appropriate operating switching frequency. If there is no resistor connected from the COMP pin to GND, the switching frequency is set to the default value of 500 kHz. If a resistor of 40.2 kΩ ± 10% is connected from the COMP pin to GND, the switching frequency is set to 300 kHz. Alternatively, if a resistor of 13.3 K ± 10% is connected from the COMP pin to GND, the switching frequency is set to 1 MHz.

After a 1.1-ms time period, the COMP pin is then brought low for 0.8 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when it is allowed to start switching.

Overcurrent Protection (OCP) setting

The device sources 10 μA (typical) to the resistor connected from the ILIM pin to GND. The voltage developed across that resistor multiplied by a factor of 2 is then sampled and latched off internally as the OCP trip level for the low-side FET until one cycles the input or toggles the EN/SS.

The voltage at EN/SS is internally clamped to 1.3 V before and/or during calibration to minimize the discharging time once calibration is complete. The discharging current is from an internal current source of 140 µA and it pulls the voltage down to 0.4 V. It then initiates the soft-start by charging up the capacitor using an internal current source of 10 µA. The resulting voltage ramp on this pin is used as a second non-inverting input to the error amplifier after an 800 mV (typical) downward level-shift; therefore, the actual soft-start does not take place until the voltage at this pin reaches 800 mV.

If the EN/SS pin is left floating, the controller starts automatically. EN/SS must be pulled down to less than 270 mV to ensure that the chip is in shutdown mode.

Soft-Start Time

The soft-start time of the TPS56221 is user programmable by selecting a single capacitor. The EN/SS pin sources 10 µA to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 10 µA to charge the capacitor through a 600 mV range. There is some initial lag due to calibration and an offset (800 mV) from the actual EN/SS pin voltage to the voltage applied to the error amplifier.

The soft-start is accomplished in a closed-loop, meaning that the error amplifier controls the output voltage at all times during the soft-start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset EN/SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin to. As the voltage on the EN/SS pin ramps up past approximately 1.4 V (800 mV offset voltage plus the 600 mV reference voltage), the 600-mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitance required for a given soft-start ramp time for the output voltage is calculated in Equation 1.

$$C_{SS} = \left(\frac{I_{SS}}{V_{FB}} \right) \times t_{SS}$$

where

- C_{SS} is the required capacitance on the EN/SS pin (nF)
- I_{SS} is the soft-start source current (10 µA)
- V_{FB} is the feedback reference voltage (0.6 V)
- t_{SS} is the desired soft-start ramp time (ms) (1)

Oscillator

The oscillator frequency is internally fixed at 500 KHz if there is no resistor connected from COMP pin to GND. Optionally, a 40.2-kΩ resistor from the COMP pin to GND sets the frequency to 300 KHz. Alternatively, a 13.3-kΩ resistor from COMP pin GND sets the frequency to 1 MHz.

Overcurrent Protection (OCP)

Programmable OCP level at ILIM is from 6 mV to 50 mV. With a scale factor of 2, the actual OC trip point across the low-side FET is in the range of 12 mV to 100 mV.

If the voltage drop across R_{OCSET} reaches 300 mV during calibration (No R_{OCSET} resistor included), it disables OC protection. Once disabled, there is no low-side or high-side current sensing.

OCP level for the high-side FET is fixed at 54 A (typical). The high-side OCP provides pulse-by-pulse current limiting.

OCP sensing for the low-side FET is a true inductor valley current detection, using sample and hold. Equation 2 can be used to calculate R_{OCSET}:

$$R_{OCSET} = \left(I_{OUT(max)} - \left(\frac{I_{P-P}}{2} \right) \right) \times 95 + 500$$

where

- $I_{P\text{-}P}$ is the peak-to-peak inductor current (A)
- $I_{OUT(max)}$ is the trip point for OCP (A)
- $R_{OC(set)}$ is the resistor used for setting the OCP level (Ω) (2)

An overcurrent (OC) condition is detected by sensing voltage drop across the low-side FET and across the high-side FET. If the voltage drop across either FET exceeds OC threshold, a count increments one count. If no OC condition is detected on either FET, the fault counter decrements by one counter. If three OC pulses are summed, a fault condition is declared which cycles the soft-start function in a hiccup mode. Hiccup mode is defined as four dummy soft-start timeouts followed by a real one if overcurrent condition is encountered during normal operation; or five dummy soft-start timeouts followed by a real one if overcurrent condition occurs from the beginning during start. This cycle continues indefinitely until the fault condition is removed.

Input Undervoltage Lockout (UVLO)

The TPS56221 has fixed input under-voltage lockout (UVLO). In order for the device to turn on, the following conditions must be met:

- the EN/SS pin voltage must be greater than V_{IH}
- the input voltage must exceed UVLO on voltage V_{UVLO}

The UVLO has a minimum of 500 mV hysteresis built-in.

Pre-Bias Startup

The TPS56221 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FB pin), if the output is pre-biased. Once the soft-start voltage exceeds the error amplifier input, the controller slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on time. It then increments the on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter.

This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage startup and ramp to regulation is smooth and controlled.

Power Good

The TPS56221 provides an indication that output is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is more than ±12.5% from nominal
- soft-start is active
- a short circuit condition has been detected

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off. Both high-side FET and low-side FET are kept off. When the junction cools to the required level (125°C typical), the PWM initiates soft start as during a normal power-up cycle.

DESIGN EXAMPLE

Introduction

This design example describes a 25-A, 12-V to 1.2-V design using the TPS56221 high-current integrated buck converter. The system specifications are listed in Table 1.

Table 1. Design Example Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8.0		14	V
$V_{IN(ripple)}$	Input ripple	I_{OUT} = 25 A			0.5	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 25 A	1.164	1.2	1.236	V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 25 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT}= 25 A			24	mV
V_{OVER}	Output overshoot	10 A ≤ I_{OUT} ≤ 20 A		50		mV
V_{UNDER}	Output undershoot	10 A ≤ I_{OUT} ≤ 20 A		50		mV
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0		25	A
t_{SS}	Softstart time	V_{IN} = 12 V		1.5		ms
I_{SCP}	Short circuit current trip point		30			A
η	Efficiency	V_{IN} = 12 V, I_{OUT} = 12.5 A		90		%
f_{SW}	Switching frequency			500		kHz
	Size				0.6	In^2

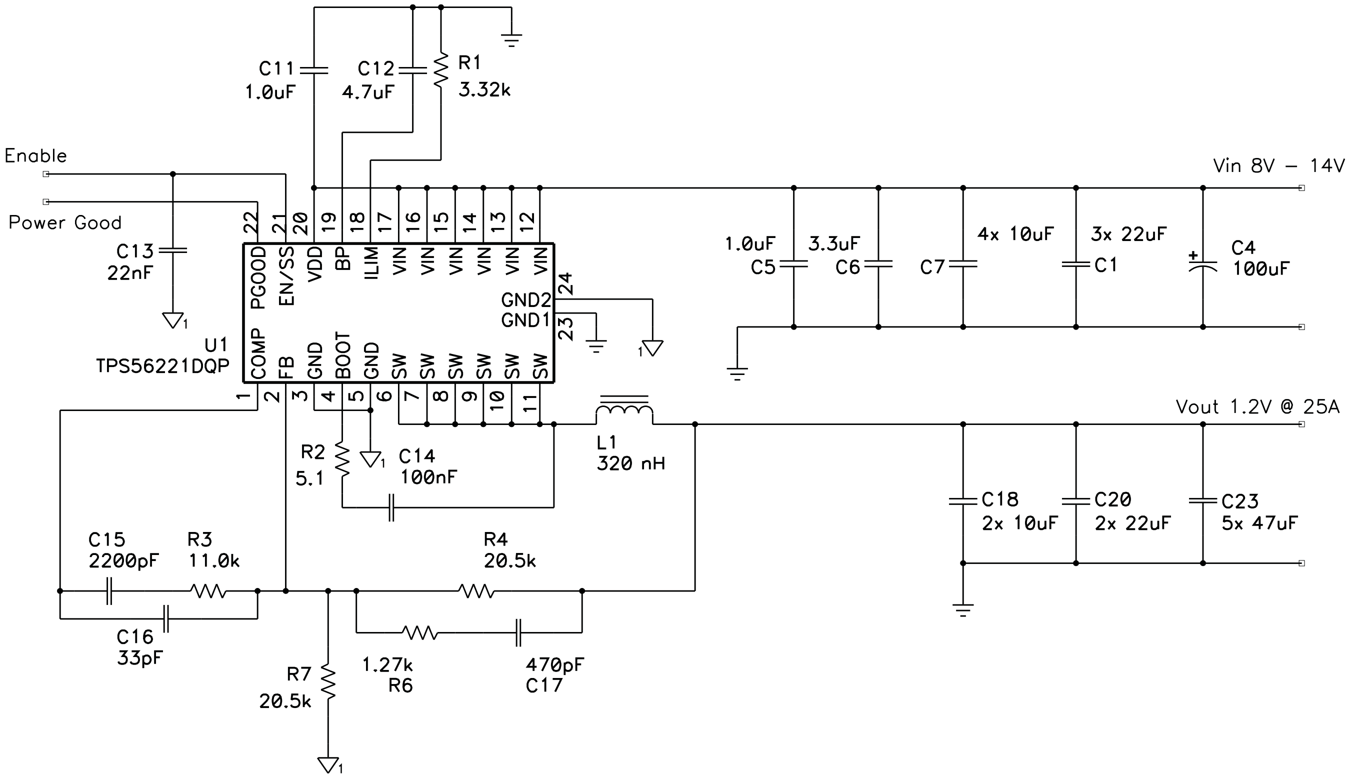


Figure 20. Design Example Schematic

Design Procedure

Switching Frequency Selection

To achieve a balance between small size and high efficiency for this design, use switching frequency of 500 kHz.

Inductor Selection (L1)

Synchronous buck power inductors are typically sized for between approximately 20% and 40% peak-to-peak ripple current (I_{RIPPLE}).

Using this target ripple current, the required inductor size can be calculated as shown in Equation 3.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14\,V - 1.2\,V}{0.3 \times 25\,A} \times \frac{1.2\,V}{14\,V} \times \frac{1}{500\,kHz} = 293\,nH \tag{3}$$

Selecting a standard 300-nH inductor value, I_{RIPPLE} =7.3A.

The RMS current through the inductor is approximated in Equation 4.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \left(\tfrac{1}{12} \times \left(I_{RIPPLE}\right)^2\right)} = \sqrt{\left(I_{OUT}\right)^2 + \left(\tfrac{1}{12} \times \left(I_{RIPPLE}\right)^2\right)} = \sqrt{(25)^2 + \left(\tfrac{1}{12} \times (7.3)^2\right)} = 25.09\,A \tag{4}$$

Output Capacitor Selection (C18, C20, C23)

The selection of the output capacitor is typically driven by the output transient response. Equation 5 and Equation 6 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

If $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot (Equation 5) to calculate minimum output capacitance. If $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot (Equation 6) to calculate minimum output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{\left(I_{TRAN}\right)^2 \times L}{V_{OUT} \times C_{OUT}} \tag{5}$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{\left(I_{TRAN}\right)^2 \times L}{\left(V_{IN} - V_{OUT}\right) \times C_{OUT}} \tag{6}$$

$$C_{OUT(min)} = \frac{\left(I_{TRAN(max)}\right)^2 \times L}{\left(V_{OUT}\right) \times V_{OVER}} = \frac{(10)^2 \times 300\,nH}{1.2 \times 50\,mV} = 500\,\mu F \tag{7}$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated inEquation 8.

$$ESR_{MAX} = \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(tot)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{24\,mV - \left(\frac{7.8\,A}{8 \times 500\,\mu F \times 500\,kHz}\right)}{7.8\,A} = 2.5\,m\Omega \tag{8}$$

In order to meet the low ESR and high capacitance requirements of this design, 5 100-μF, 1210 ceramic capacitors are selected. 3 22-μF, 1206 ceramic capacitors and 2 10-μF 0805 ceramic capacitors are added to reduce ESL and inductive ringing. The combination of multiple capacitor types and ceramic capacitors of different sizes provides a wider band to the filtering frequencies of the output capacitors.

Inductor Peak Current Rating

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 9.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.2\,V \times 586\,\mu F}{1.5\,ms} = 0.469\,A \tag{9}$$

$$I_{L(peak)} = I_{OUT(max)} + \left(\tfrac{1}{2} \times I_{RIPPLE}\right) + I_{CHARGE} = 25\,A + \left(\tfrac{1}{2} \times 7.8\,A\right) + 0.469\,A = 29.4\,A \tag{10}$$

Table 2. Inductor Requirements Summary

PARAMETER		VALUE	UNITS
L	Inductance	300	nH
$I_{L(rms)}$	RMS current (thermal rating)	25.08	A
$I_{L(peak)}$	Peak current (saturation rating)	29.4	A

Boot-Strap Capacitor (C14)

The bootstrap resistor slows the rising edge of the SW voltage to reduce ringing and improve EMI. Per the datasheet recommendation a 5.1? resistor is selected.

VDD Bypass Capacitor (C11)

Per the TPS56221 recommended pin terminations, VDD is bypassed to GND with a 1.0-μF capacitor.

Soft-Start Capacitor (C13)

The soft-start capacitor provides a constant ramp voltage to the error amplifier to provide controlled, smooth start-up. The soft-start capacitor is sized using Equation 11.

$$C_{SS} = \frac{I_{SS}}{V_{FB}} \times t_{SS} = \frac{10\,\mu A}{0.6\,V} \times 1.5\,ms = 25\,nF \approx 22\,nF \tag{11}$$

Current Limit (R1)

The TPS56221 uses the negative drop across the internal low-side FET at the end of the OFF-time to measure the valley of the inductor current. Allowing for a minimum of 30% over maximum load, the programming resistor is selected using Equation 12.

$$R_{OCSET} = 95 \times \left(1.3 \times I_{OUT(max)} - \left(\frac{I_{RIPPLE}}{2}\right)\right) + 500\ \Omega = 95 \times \left(1.3 \times 25\ A - \left(\frac{7.8\ A}{2}\right)\right) + 500\ \Omega = 3.23\ k\Omega \approx 3.32\ k\Omega \tag{12}$$

Feedback Divider (R4, R7)

The TPS56221 converter uses a full operational amplifier with an internally fixed 0.600-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 20.5 kΩ, The output voltage is programmed with a resistor divider given by Equation 13.

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{\left(V_{OUT} - V_{FB}\right)} = \frac{0.600\,V \times 20.5\,k\Omega}{1.2\,V - 0.600\,V} = 20.5\,k\Omega \approx 20.5\,k\Omega \tag{13}$$

PRODUCT PREVIEW

Compensation (C15, C16, C17, R3, R6)

Using the *TPS40k Loop Stability Tool* for 60 kHz of bandwidth and 60 degrees of phase margin with an R4 value of 20.5 kΩ, the following values are obtained.

- C17 = C_1 = 470 pF
- C15 = C_2 = 2200 pF
- C16 = C_3 = 33 pF
- R6 = R_2 = 1.27 kΩ
- R3 = R_3 = 11.0 kΩ

DESIGN EXAMPLE PERFORMANCE CHARACTERISTICS

Output voltage 12 V to 1.2V at 0-A to 25-A input current.

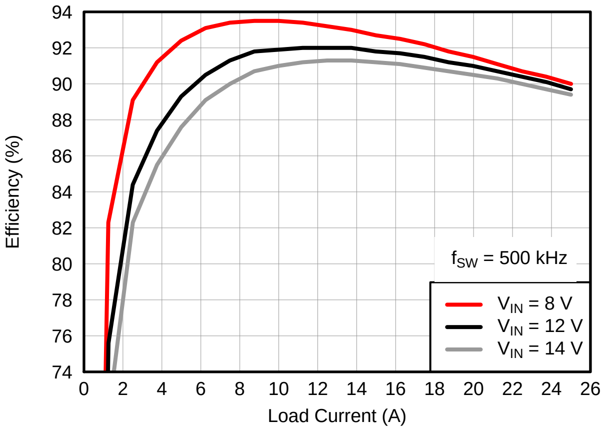


Figure 21. Efficiency vs Load Current

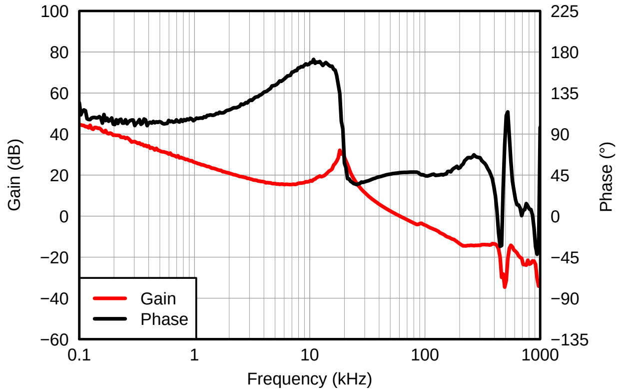


Figure 22. Loop Response 96 kHz Bandwidth, 64° Phase Margin

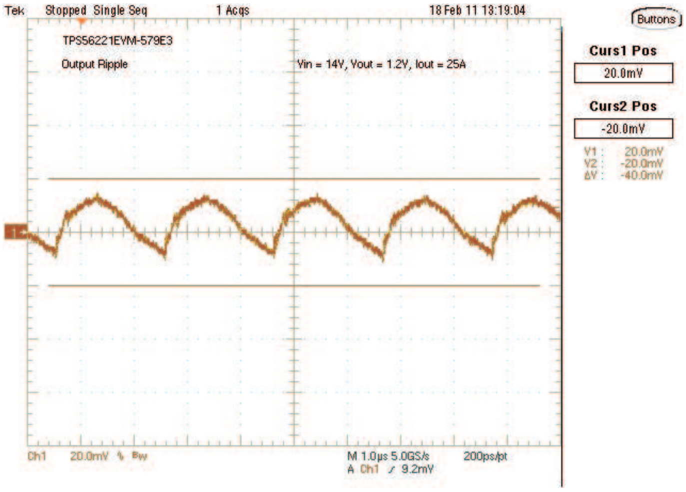


Figure 23. Output Ripple 20 mV/div, 1.0 μs/div, 20 MHz Bandwidth, AC Coupled

Table 3. List of Materials for TPS56221 Design Example

REFERENCE DESiGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
C1	3	22 μF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
C4	1	100 μF	Capacitor, Aluminum, 16VDC, ±20%	D8	EEEFP1C101AP	Panasonic
C5	1	1.0 μF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
C6	1	3.3 μF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
C7	4	10 μF	Capacitor, Ceramic, 25V, X7R, 20%	1206	Std	Std
C11	1	1.0 μF	Capacitor, Ceramic, 25V, X5R, 20%	0805	Std	Std
C12	1	4.7 μF	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
C13	1	22 μF	Capacitor, Ceramic, 16V, X7R, 20%	0402	Std	Std
C14	1	100 μF	Capacitor, Ceramic, 16V, X7R, 20%	0402	Std	Std
C15	1	2200 pF	Capacitor, Ceramic, 25V, X7R, 10%	0402	Std	Std
C16	1	33 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
C17	1	470 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
C18	2	10 μF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
C20	2	22 μF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
C23	5	47 μF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Vishay
L1	1	320 nH	IND, SMT Power ±15%	0.394 x 0.476 inch	PA2202-321NL	Pulse
R1	1	3.32 kΩ	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R2	1	5.1 Ω	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R3	1	11.0 kΩ	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R4	1	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R6	1	1.27 kΩ	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R7	1	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0402	Std	Std
U1	1	TPS56221DQP	25 A, 600 kHz, synchronous buck converter	QFN-22 6 × 5 mm	TPS56221DQP	TI

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPS56221DQPR	ACTIVE	SON	DQP	22	2500	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	
TPS56221DQPT	ACTIVE	SON	DQP	22	250	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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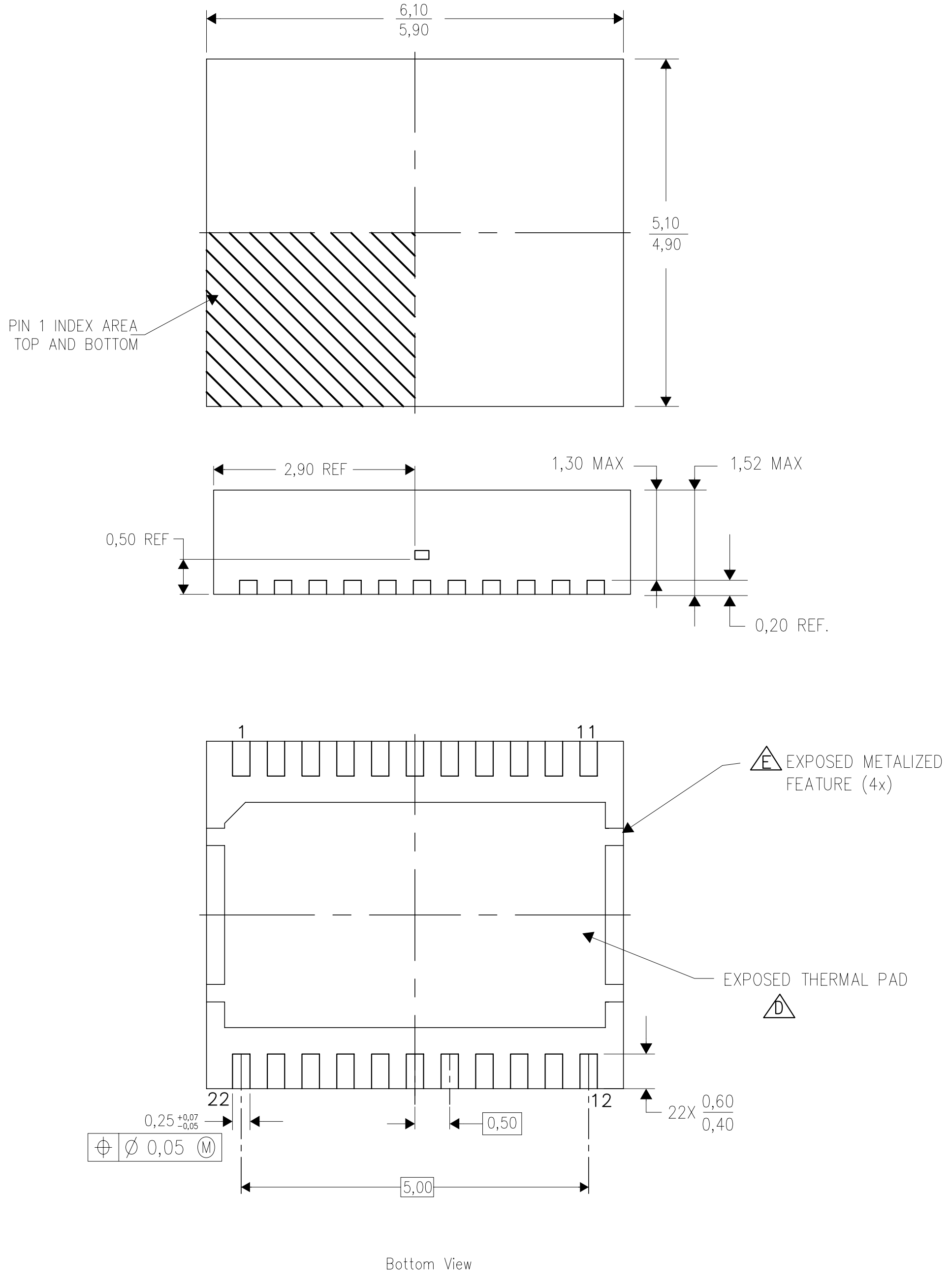
DQP (R-PSON-N22) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No−Lead (SON) package configuration.
- D The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E Metalized features are supplier options and may not be on the package.

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