SM802108

ClockWorks™ 10GbE & GbE (156.25MHz, 125MHz) Ultra-Low Jitter, LVPECL Frequency Synthesizer

General Description

The SM802108 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for GbE and 10GbE Ethernet clock signals. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes two LVPECL output clocks at 156.25MHz and another two at 125MHz. The SM802108 accepts a 25 MHz crystal or LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

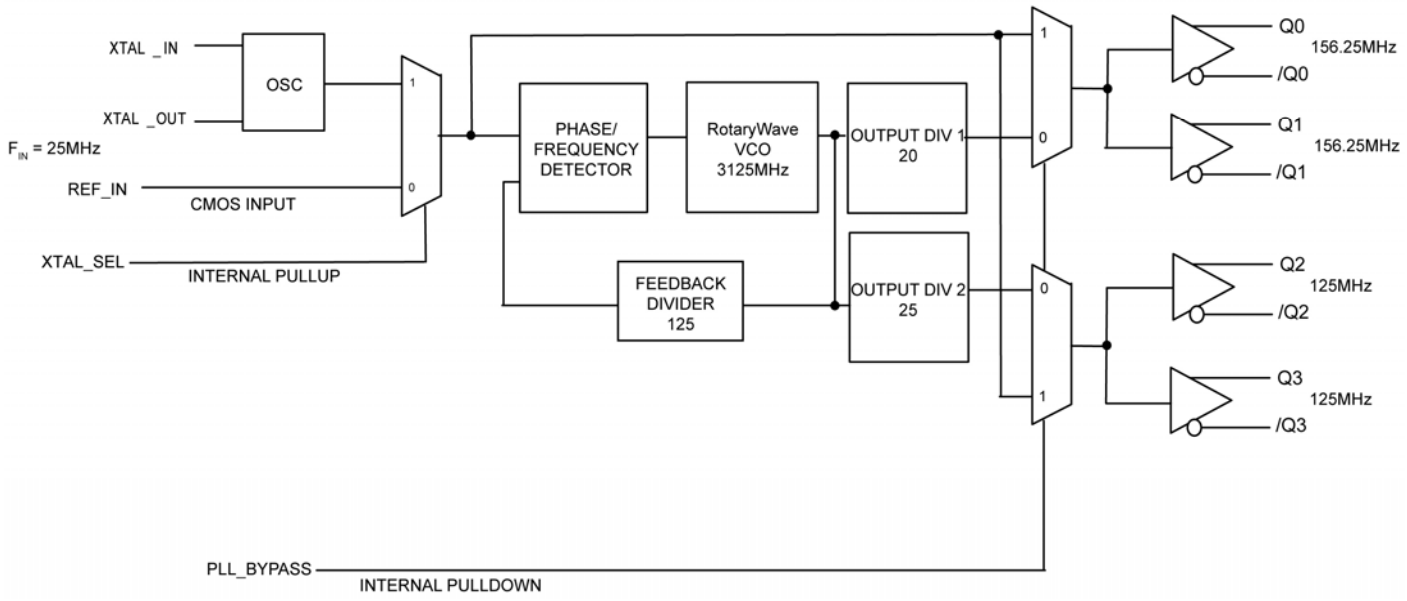
Features

- Generates two LVPECL clock outputs at 156.25MHz and two LVPECL clock outputs at 125MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 156.25MHz (1.875MHz to 20MHz): 110fs (typical) at 3.3V
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- 10Gigabit Ethernet
- Gigabit Ethernet

Block Diagram



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RotaryWave is a registered trademark of Multigig, Inc.

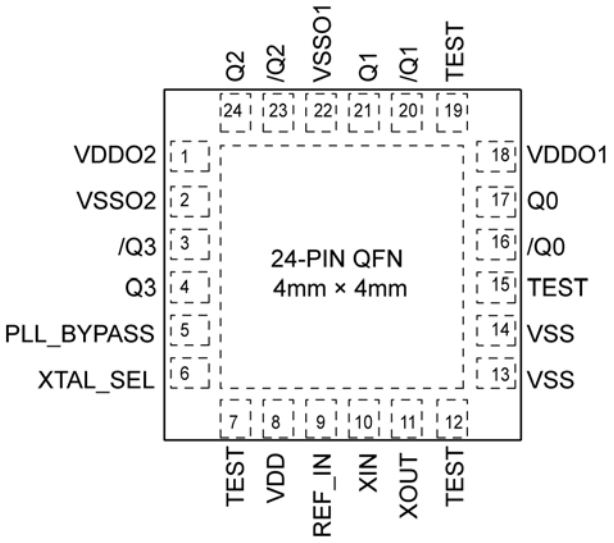
Ordering Information

Part Number	Marking	Shipping	Junction Temperature Range	Package
SM802108UMG	802108	Tube	–40°C to +85°C	24-Pin QFN
SM802108UMGR	802108	Tape and Reel	–40°C to +85°C	24-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



24-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
16, 17 20, 21	/Q0, Q0 /Q1, Q1	O, (DIF)	LVPECL	Differential Clock Outputs from Bank 1 156.25MHz
23, 24 3, 4	/Q2, Q2 /Q3, Q3	O, (DIF)	LVPECL	Differential Clock Outputs from Bank 2 125MHz
1	VDDO2	PWR		Power Supply for Output Bank 2
2	VSSO2	PWR		Power Supply Ground for Output Bank 2
5	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock or Crystal 45KΩ pull-down
6	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Input Reference Source 0 = REF_IN, 1 = XTAL, 45KΩ pull-up

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
7, 12, 15, 19	TEST			Factory Test Pins, Do not connect anything to these pins.
8	VDD	PWR		Core Power Supply
9	REF_IN	I, (SE)	LVCMOS	Reference Clock Input
10	XIN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed. See Fig. 5.
11	XOUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed. See Fig. 5.
13, 14	VSS	PWR		Core Power Supply Ground
18	VDDO1	PWR		Power Supply for Output Bank 1
22	VSSO1	PWR		Power Supply Ground for Output Bank 1

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible. Do not place switching signals or noisy supplies under the crystal.

Truth Table

PLL_BYPASS	XTAL_SEL	INPUT	OUTPUT
0	–	–	PLL
1	–	–	XTAL/REF_IN
–	0	REF_IN	–
–	1	XTAL	–

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Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, V_{DDOx}) ..... +4.6V
Input Voltage (V_{IN}). ..... –0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20sec.) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}, V_{DDOx}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 50°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 30°C/W

DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDOx}	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, V_{DDOx}	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO}	Outputs open; REF_IN source, XTAL_SEL = 0		130	165	mA
I_{DD}	Supply current V_{DD} + V_{DDO}	Outputs open; CRYSTAL source, XTAL_SEL = 1		145	185	mA

LVPECL DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		V_{DDO} – 1.145	V_{DDO} – 0.97	V_{DDO} – 0.845	V
V_{OL}	Output Low Voltage		V_{DDO} – 1.945	V_{DDO} – 1.77	V_{DDO} – 1.645	V
V_{SWING}	Output Voltage Swing		0.6	0.8	1.0	V

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVCMOS (PLL_BYPASS, XTAL_SEL) DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IN}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–5			µA

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	XTAL_SEL = V_{IL}, V_{IN} = 0V to V_{DD}	–5		5	µA
I_{IN}	Input Current	XTAL_SEL = V_{IH}, V_{IN} = V_{DD}		20		µA

Crystal Characteristics

NDK NX2520SA

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load	Fundamental, Parallel Resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			3	7	pF
Correlation Drive Level			100	300	uW

AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

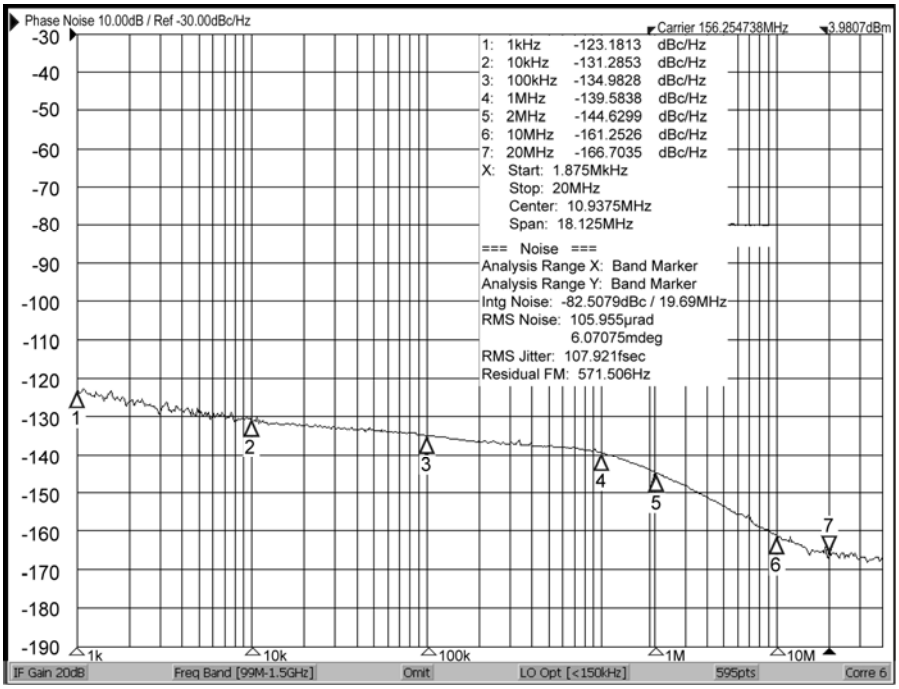
T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT1}	Output Frequency 1			156.25		MHz
F_{OUT2}	Output Frequency 2			125		
Ppm	Output ppm Variation	Crystal reference. Note 6	–50		50	ppm
F_{REF}	Reference Input Frequency			25		MHz
T_R/T_F	LVPECL Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle		48	50	52	%
T_{SKEW}	Output-to-Output Skew	Within bank. Note 7			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[8]	156.25MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz) 125MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)		110 250 110 250		fs
	Spurious Noise Components	6.25MHz 25MHz		-73 -58		dBc

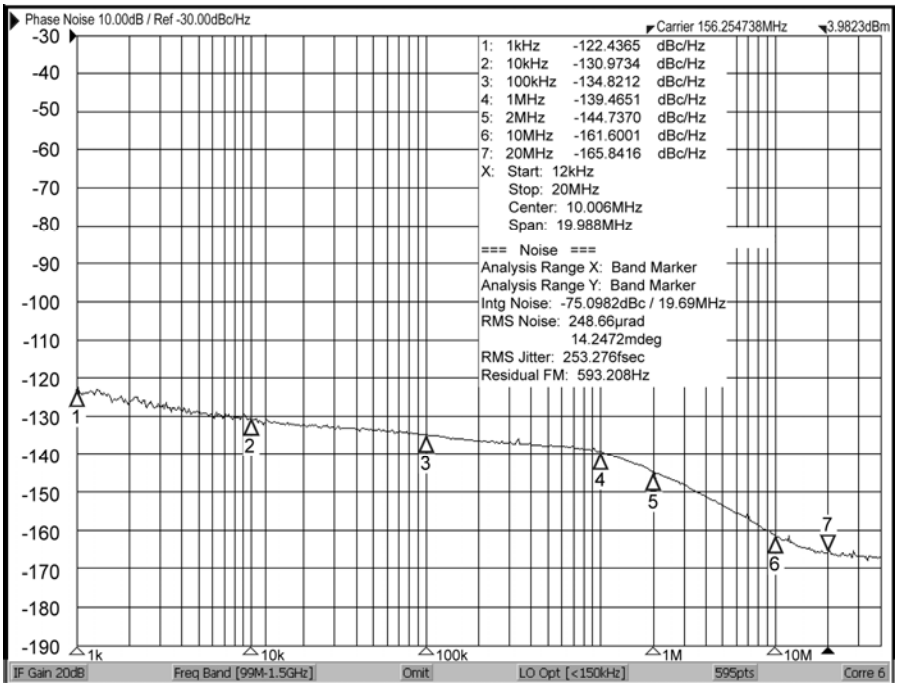
Notes:

5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
6. Crystal tolerance at room less than +/- 15ppm, over temp less than +/- 20ppm.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions and same frequency; Measured at the output differential crossing points.
8. Measured using 25MHz crystal as the input reference source.

Phase Noise Plots

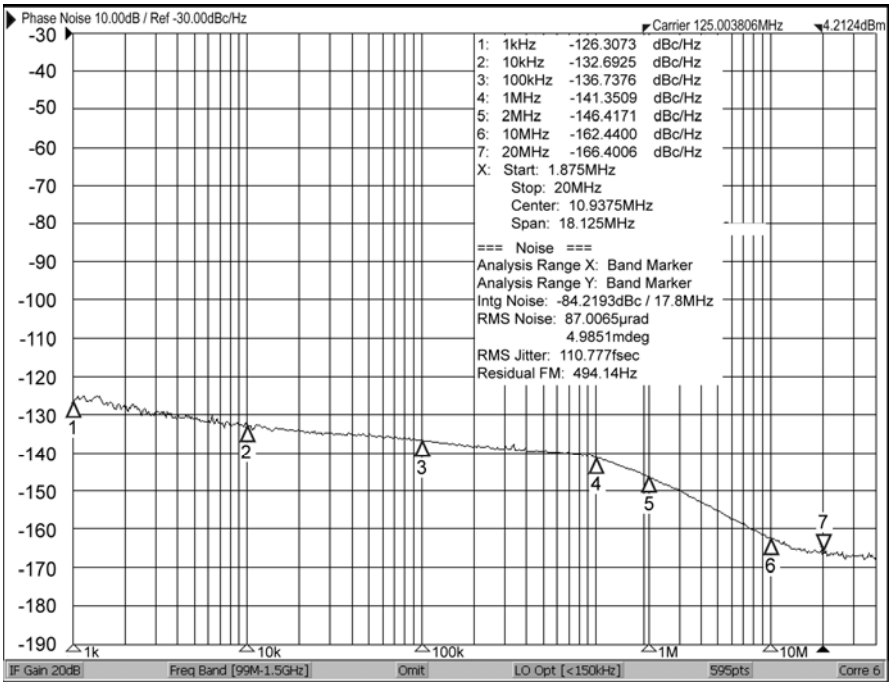


Phase Noise Plot: 156.25MHz, 1.875MHz – 20MHz 108fS

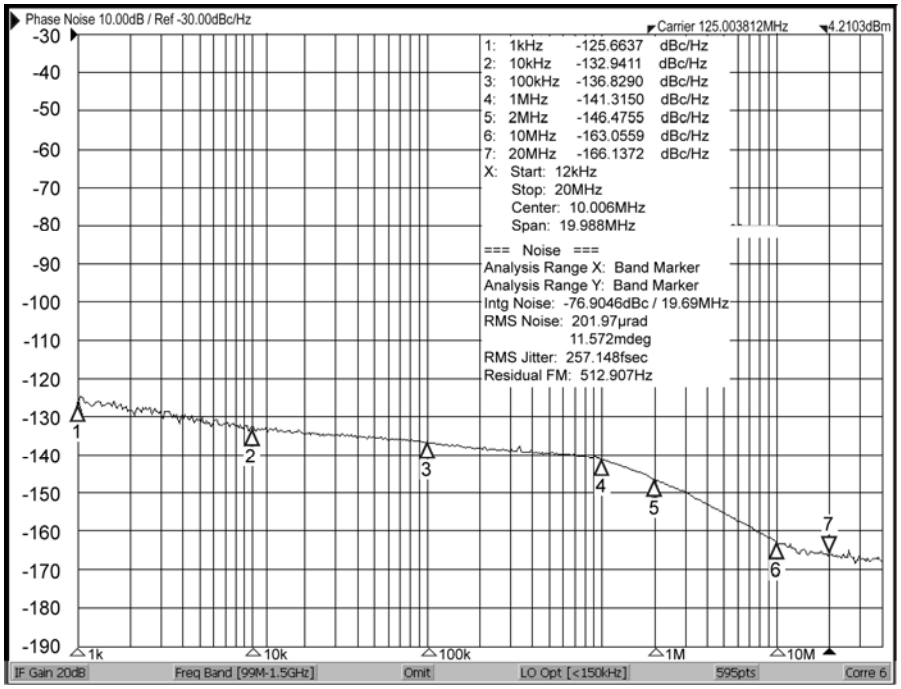


Phase Noise Plot: 156.25MHz, 12kHz – 20MHz 253fS

Phase Noise Plots (Continued)



Phase Noise Plot: 125MHz, 1.875MHz – 20MHz 111fS



Phase Noise Plot: 125MHz, 12kHz – 20MHz 257fS

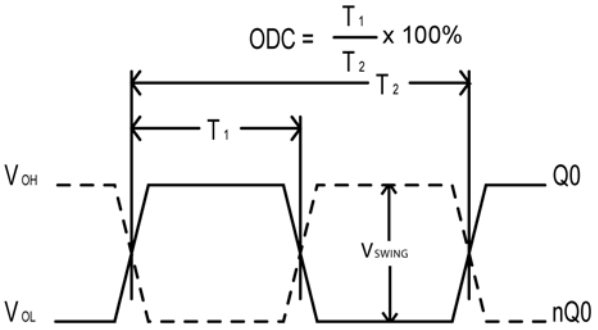


Figure 1. Duty Cycle TIming

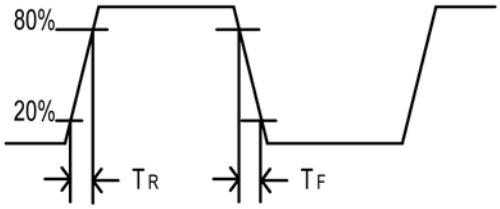


Figure 2. All Outputs Rise/Fall Time

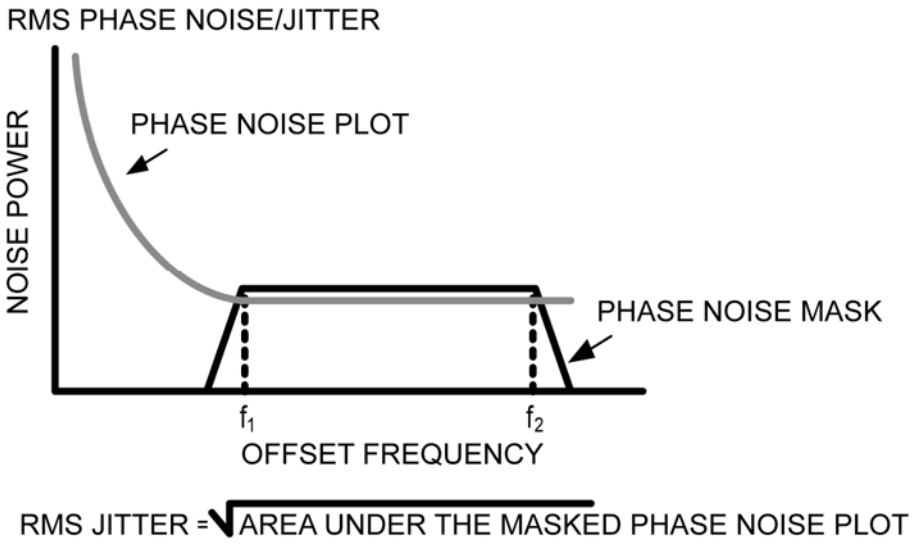


Figure 3. RMS Phase/Noise/Jitter

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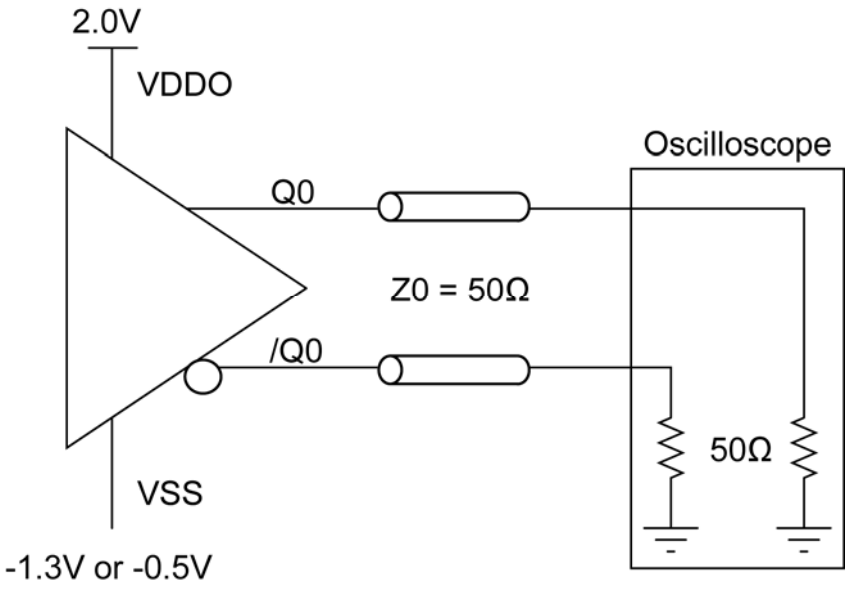


Figure 4. LVPECL Output Load and Test Circuit

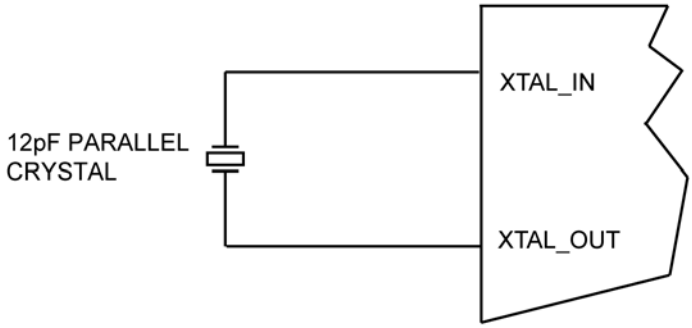
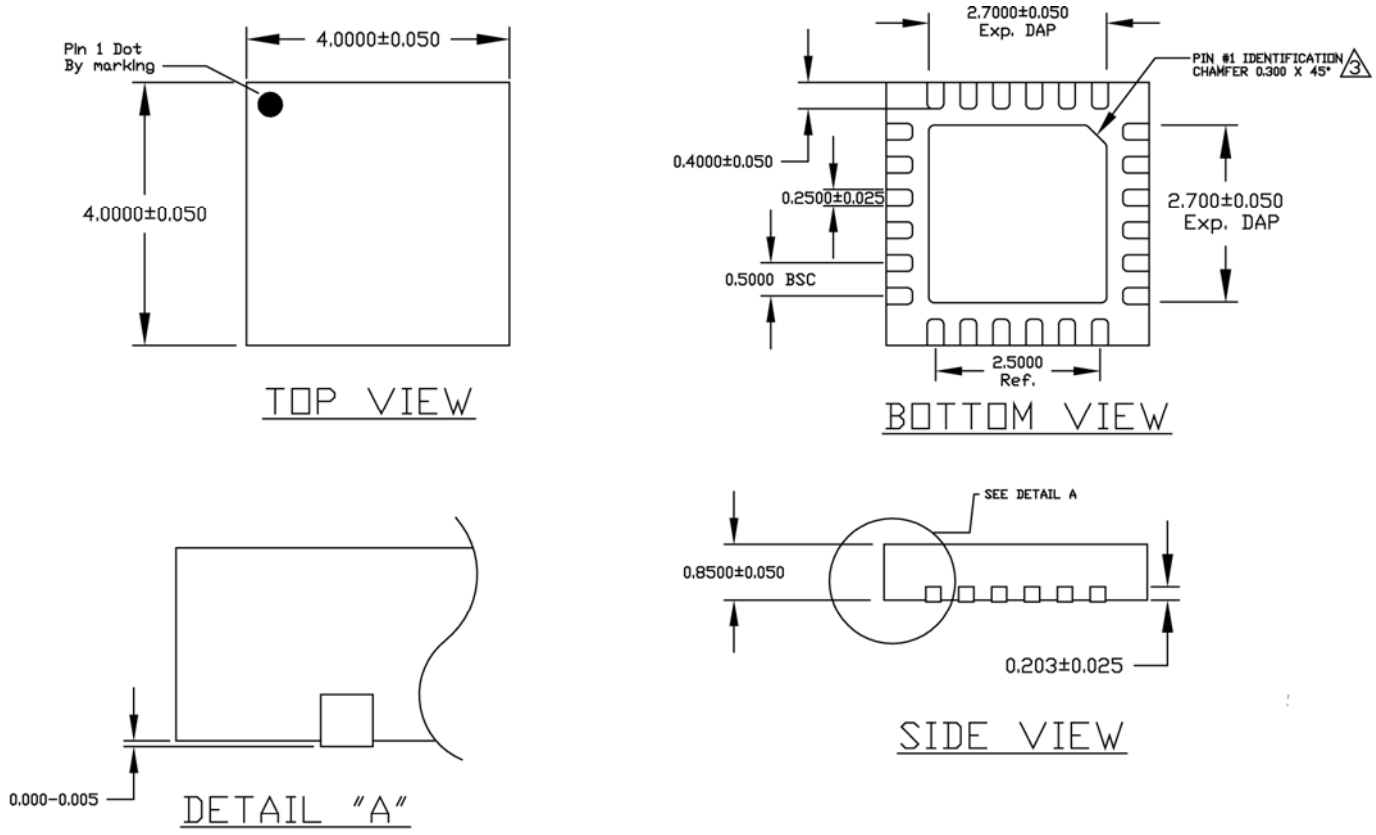


Figure 5. Crystal Input Interface

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

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