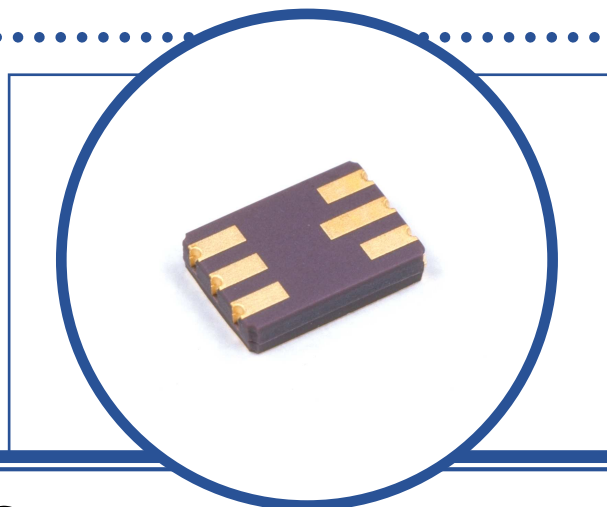


# SILICON EPITAXIAL DUAL NPN TRANSISTORS

## 2N3904DCSM

- Dual Silicon Planar NPN Transistors.
- Hermetic Ceramic Surface Mount Package.
- Designed For General Purpose and Switching Applications.
- Screening Options Available.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise stated)

		Each Side	Total Device
V <sub>CBO</sub>	Collector – Base Voltage	60V	
V <sub>CEO</sub>	Collector – Emitter Voltage	40V	
V <sub>EBO</sub>	Emitter – Base Voltage	6V	
I <sub>C</sub>	Continuous Collector Current	200mA	
P <sub>D</sub>	Total Power Dissipation at T <sub>A</sub> = 25°C Derate Above 25°C	500mW 2.86mW/°C	600mW <sup>(1)</sup> 3.43mW/°C
T <sub>J</sub>	Junction Temperature Range	-55 to +200°C	
T <sub>stg</sub>	Storage Temperature Range	-55 to +200°C	

### THERMAL PROPERTIES (Each Side)

Symbols	Parameters	Min.	Typ.	Max.	Units
R <sub>θJA</sub>	Thermal Resistance, Junction To Ambient			350	°C/W

#### Notes

(1) Total device power dissipation limited by package.

# SILICON EPITAXIAL DUAL NPN TRANSISTORS 2N3904DCSM

## ELECTRICAL CHARACTERISTICS (Each Side, $T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$I_{CBO}$	Collector-Cut-Off Current	$V_{CB} = 30\text{V}$ $I_E = 0$			30	nA
$I_{EBO}$	Emitter Cut-Off Current	$V_{EB} = 3\text{V}$ $I_C = 0$			30	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\mu\text{A}$	60			V
$V_{(BR)CEO}^{(2)}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0\text{mA}$	40			
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\mu\text{A}$	6			
$h_{FE}^{(2)}$	Forward-current transfer ratio	$I_C = 0.1\text{mA}$	$V_{CE} = 1.0\text{V}$	40		
		$I_C = 1.0\text{mA}$		70		
		$I_C = 10\text{mA}$		100	300	
		$I_C = 50\text{mA}$		60		
		$I_C = 100\text{mA}$		30		
$V_{BE(sat)}^{(2)}$	Base-Emitter Saturation Voltage	$I_C = 10\text{mA}$ $I_B = 1.0\text{mA}$	0.65		0.85	V
		$I_C = 50\text{mA}$ $I_B = 5\text{mA}$			0.95	
$V_{CE(sat)}^{(2)}$	Collector-Emitter Saturation Voltage	$I_C = 10\text{mA}$ $I_B = 1.0\text{mA}$			0.2	
		$I_C = 50\text{mA}$ $I_B = 5\text{mA}$			0.3	
$V_{BE(f)}^{(2)}$	Forward Base-Emitter Voltage	$I_B = 500\text{mA}$			1.45	
		$I_B = 200\text{mA}$ $T_A = 100^\circ\text{C}$			2	

## DYNAMIC CHARACTERISTICS

$f_T$	Transition Frequency	$I_C = 10\text{mA}$ $V_{CE} = 20\text{V}$ $f = 100\text{MHz}$	300			MHz
$h_{fe}$	Small-Signal Current Gain	$I_C = 1.0\text{mA}$ $V_{CE} = 10\text{V}$ $f = 1.0\text{KHz}$	100		400	
$C_{obo}$	Output Capacitance	$V_{CB} = 5\text{V}$ $I_E = 0$ $f = 1.0\text{MHz}$			4	pF
$C_{ibo}$	Input Capacitance	$V_{EB} = 0.5\text{V}$ $I_C = 0$ $f = 1.0\text{MHz}$			8	
$NF^{(3)}$	Noise Figure	$I_C = 100\mu\text{A}$ $V_{CE} = 5\text{V}$ $R_S = 1.0\text{K}\Omega$ $f = 10\text{Hz To } 15.7\text{KHz}$			5	dB
$t_d$	Delay Time	$V_{CC} = 3\text{V}$ $V_{BE} = 0.5\text{V}$			35	ns
$t_r$	Rise Time	$I_C = 10\text{mA}$ $I_{B1} = 1.0\text{mA}$			35	
$t_s$	Storage Time	$V_{CC} = 3\text{V}$ $I_C = 10\text{mA}$			200	
$t_f$	Fall Time	$I_{B1} = I_{B2} = 1.0\text{mA}$			50	

### Notes

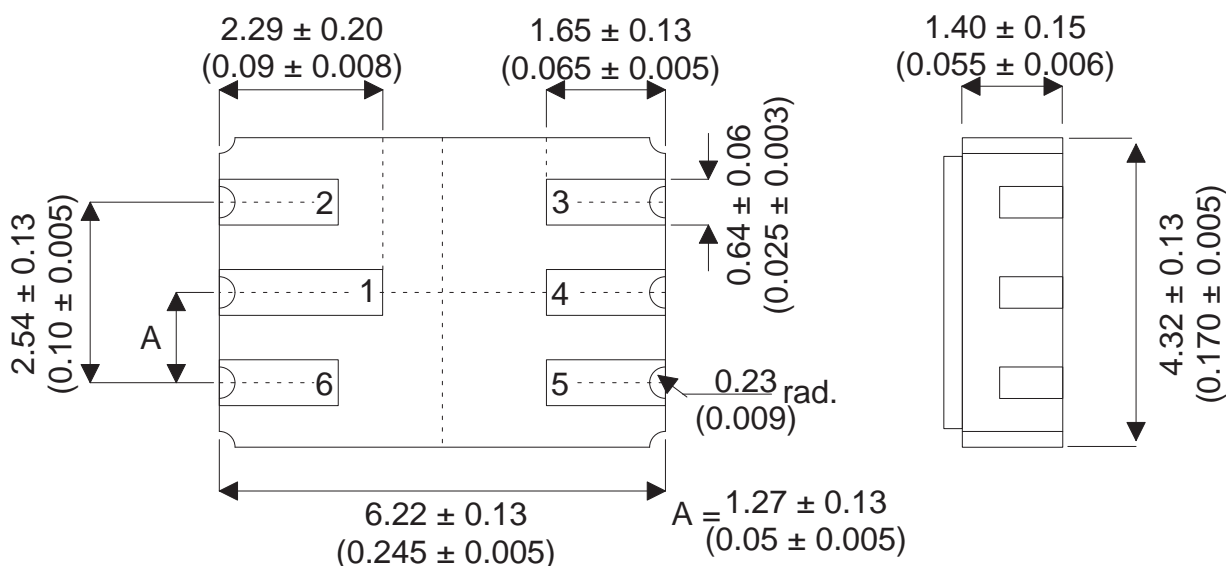
(2) Pulse Width  $\leq 300\mu\text{s}$ ,  $\delta \leq 2\%$

(3) By design only, not a production test.

# SILICON EPITAXIAL DUAL NPN TRANSISTORS 2N3904DCSM

## MECHANICAL DATA

Dimensions in mm (inches)



### LCC2 (MO-041BB)

#### Underside View

- |                     |                     |
|---------------------|---------------------|
| Pad 1 – Collector 1 | Pad 4 – Collector 2 |
| Pad 2 – Base 1      | Pad 5 – Emitter 2   |
| Pad 3 – Base 2      | Pad 6 – Emitter 1   |