W191

Skew Controlled SDRAM Buffer

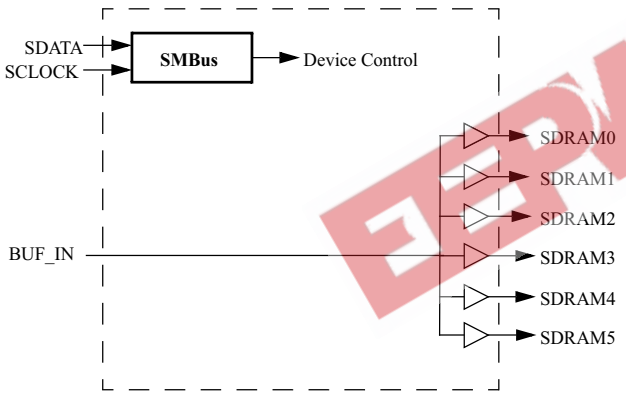
Features

- Six skew controlled CMOS outputs
- Output skew between any two outputs is less than 150 ps
- SMBus Serial configuration interface
- 2.5 ns to 5 ns propagation delay
- DC to 133 MHz operation (Commercial)
- DC to 100 MHz operation (Industrial)
- Single 3.3V supply voltage
- Low power CMOS design packaged in a 16-pin SSOP (Small Shrink Outline Package)

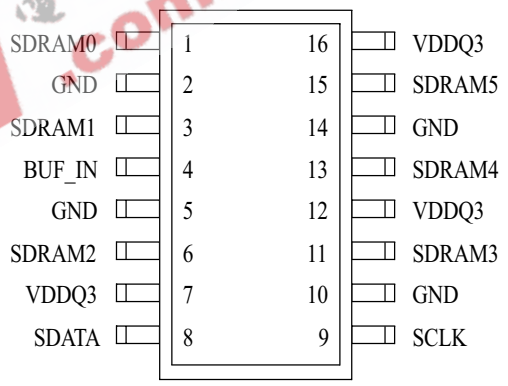
Key Specifications

Supply Voltages: ..... V_{DDQ3} = 3.3V ±5%
Operating Temperature: (Commercial) ..... 0°C to +70°C
Operating Temperature: (Industrial)..... –40°C to +85°C
Input Threshold:.....1.5V typical
Maximum Input Voltage: ..... V_{DDQ3} + 0.5V
Input Frequency: (Commercial) .....0 to 133 MHz
Input Frequency: (Industrial).....0 to 100 MHz
BUF_IN to SDRAM0:5 Propagation Delay:.....2.5 ns to 5 ns
Min. Output Edge Rate: 1.0V/ns
Max. Output Skew: ..... 150 ps
Output Duty Cycle:.....45/55% worst case
Output Impedance: .....15Ω typ.

Block Diagram



Pin Configuration[1]



Note:
1. Internal pull-up resistor of 250K on SDATA and SCLK.

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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
SDRAM0:5	1, 3, 6, 11, 13, 15	O	***SDRAM Outputs:*** Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 2.5 to 5 ns. All outputs are skew controlled to within ±150 ps of each other.
BUF_IN	4	I	***Clock Input:*** This clock input has an input threshold voltage of 1.5V (typ).
SDATA	8	I/O	***SMBus Data input:*** Data should be presented to this input as described in the SMBus section of this data sheet. Internal 250-kΩ pull-up resistor.
SCLOCK	9	I	***SMBus clock input:*** The SMBus Data clock should be presented to this input as described in the SMBus section of this data sheet. Internal 250-kΩ pull-up resistor.
VDDQ3	7, 12, 16	P	***Power Connection:*** Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	2, 5, 10, 14	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Overview

The W191 is a skew controlled fanout buffer optimized for interface with registered DIMMs.

Functional Description

Output Drivers

The W191 output buffers are CMOS type which deliver a rail-to-rail (GND to VDD) output voltage swing into a nominal capacitive load. Thus, output signaling is both TTL and CMOS level compatible. Nominal output buffer impedance is 15Ω.

Serial Control

Serial control data is written to the W191 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 1*

Writing Data Bytes

Each bit in the data bytes control a particular device function. Bits are written MSB (most significant bit) first, which is bit 7. *Table 1* gives the bit formats for registers located in Data Bytes 0-2.

Table 1. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W191 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W191 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W191, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W191, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communi-cation protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 2*	The data bits in these bytes set internal W191 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 2*.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Don't Care	
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Table 2. Data Bytes 0–2 Serial Configuration Map[2]

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
Data Byte 0 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	6	SDRAM2	Clock Output Disable	Low	Active
6	--	--	(Reserved)	--	--
5	--	--	(Reserved)	--	--
4	--	--	(Reserved)	--	--
3	--	--	(Reserved)	--	--
2	3	SDRAM1	Clock Output Disable	Low	Active
1	--	--	(Reserved)	--	--
0	1	SDRAM0	Clock Output Disable	--	--
Data Byte 1 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	--	--	Clock Output Disable	--	--
6	15	SDRAM5	Clock Output Disable	Low	Active
5	--	--	Clock Output Disable	--	--
4	--	--	(Reserved)	--	--
3	13	SDRAM4	Clock Output Disable	Low	Active
2	--	--	(Reserved)	--	--
1	--	--	(Reserved)	--	--
0	--	--	(Reserved)	--	--
Data Byte 2 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	11	SDRAM3	Clock Output Disable	Low	Active
6	--	--	(Reserved)	--	--
5	--	--	(Reserved)	--	--
4	--	--	(Reserved)	--	--
3	--	--	(Reserved)	--	--
2	--	--	(Reserved)	--	--
1	--	--	(Reserved)	--	--
0	--	--	(Reserved)	--	--

Note:
2. At power up all SDRAM outputs are enabled and active. Program Reserved bits to 0.

Absolute Maximum Ratings[3]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DDQ3}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to + 7.0	V
T_{STG}	Storage Temperature	–65 to + 150	°C
T_B	Ambient Temperature under Bias	–55 to + 125	°C
T_A	Operating Temperature (Commercial)	0 to + 70	°C
T_A	Operating Temperature (Industrial)	–40 to + 85	°C

DC Electrical Characteristics: T_A = 0°C to +70°C (Commercial), V_{DDQ3} = 3.3V ± 5%, T_A = –40°C to +85°C (Industrial), V_{DDQ3} = 3.3V ± 5% [4]

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	3.3V Supply Current	BUF_IN = 100 MHz		173		mA
I_{DD}	3.3V Supply Current in three-state	BUF_IN = 100 MHz		5		mA
Logic Inputs (BUF_IN, OE, SCLOCK, SDATA)						
V_{IL}	Input Low Voltage		GND–0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DDQ3}+0.5	V
I_{ILEAK}	Input Leakage Current, BUF_IN		–5		+5	µA
I_{ILEAK}	Input Leakage Current[5]		–20		+5	µA
Logic Outputs (SDRAM0:5)						
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	65	100	160	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	70	110	185	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance (Except BUF_IN)				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:
3. Multiple supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
4. Outputs loaded by 6" 60Ω transmission lines with 20 pF capacitors.
5. OE, SCLOCK, and SDATA logic pins have a 250-kΩ internal pull-up resistor (not CMOS level).

AC Electrical Characteristics: T_A = 0°C to +70°C (Commercial), V_{DDQ3} = 3.3V ± 5%, T_A = -40°C to +85°C (Industrial), V_{DDQ3} = 3.3V ± 5% (Lump Capacitance Test Load = 30pF)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency (Commercial)		0		133	MHz
f_{IN}	Input Frequency (Industrial)		0		100	MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.0		4.0	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.0		4.0	V/ns
t_{SR}	Output Skew, Rising Edges				150	ps
t_{SF}	Output Skew, Falling Edges				150	ps
t_{EN}	Output Enable Time		1.0		8.0	ns
t_{DIS}	Output Disable Time		1.0		8.0	ns
t_{PR}	Rising Edge Propagation Delay		2.5		5.0	ns
t_{PF}	Falling Edge Propagation Delay		2.5		5.0	ns
t_D	Duty Cycle	Measured at 1.5V	45		55	%
Z_o	AC Output Impedance			15		Ω

How To Use the Serial Data Interface

Electrical Requirements

Figure 1 illustrates electrical characteristics for the serial interface bus used with the W191. Devices send data over the bus with an open drain logic output that can (a) pull the bus line low, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W191 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

Signaling Requirements

As shown in *Figure 2*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock high pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “Start Bit” as shown in *Figure 3*. A “Stop Bit” signifies that a transmission has ended.

As stated previously, the W191 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 4*.

Sending Data to the W191

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

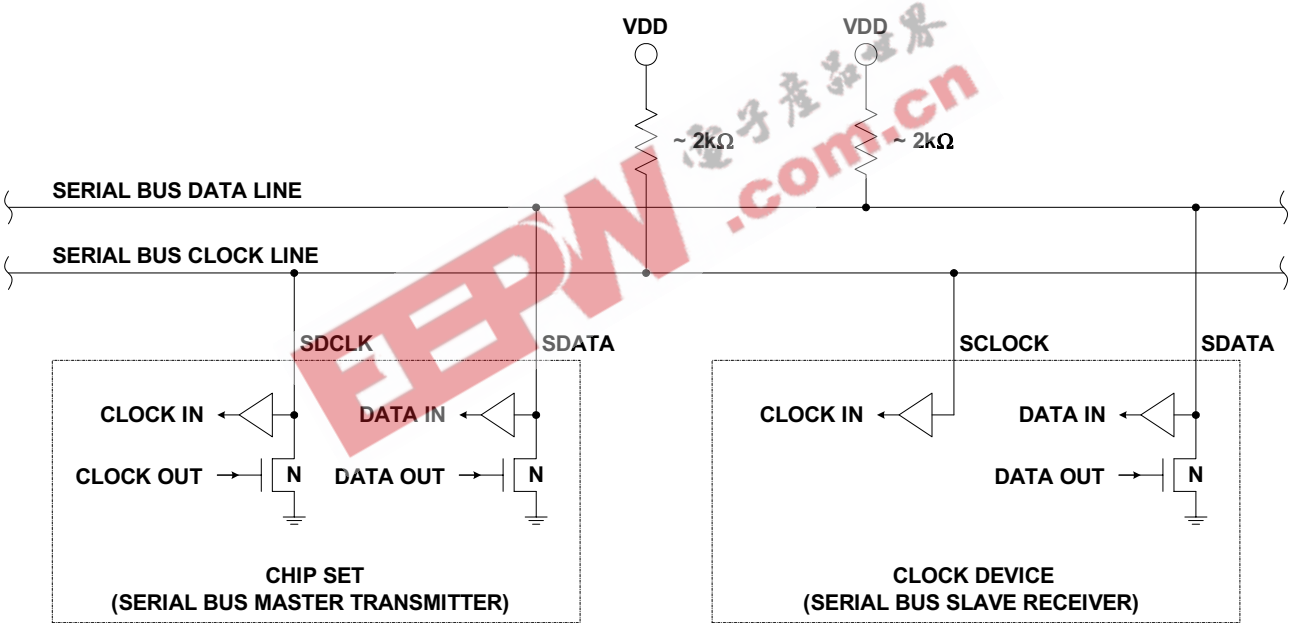


Figure 1. Serial Interface Bus Electrical Characteristics

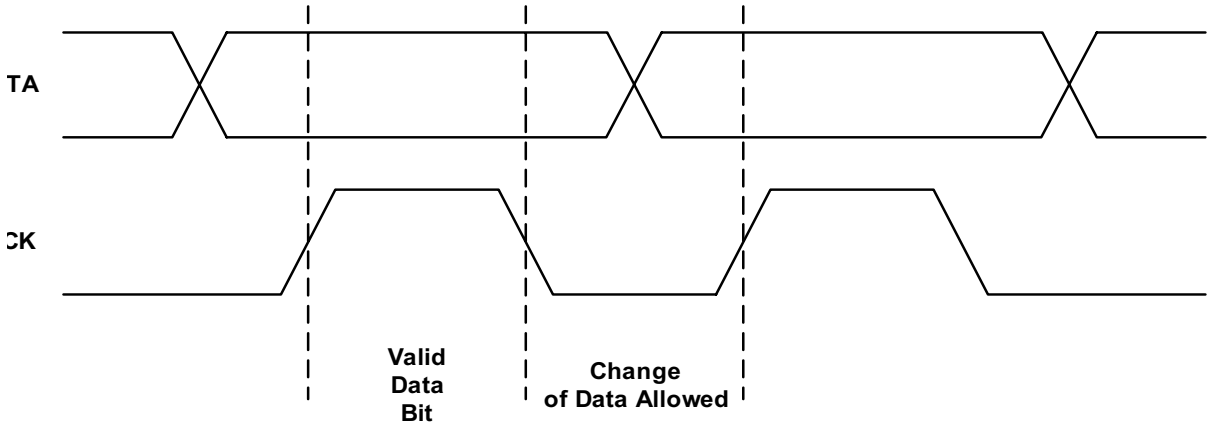


Figure 2. Serial Data Bus Valid Data Bit

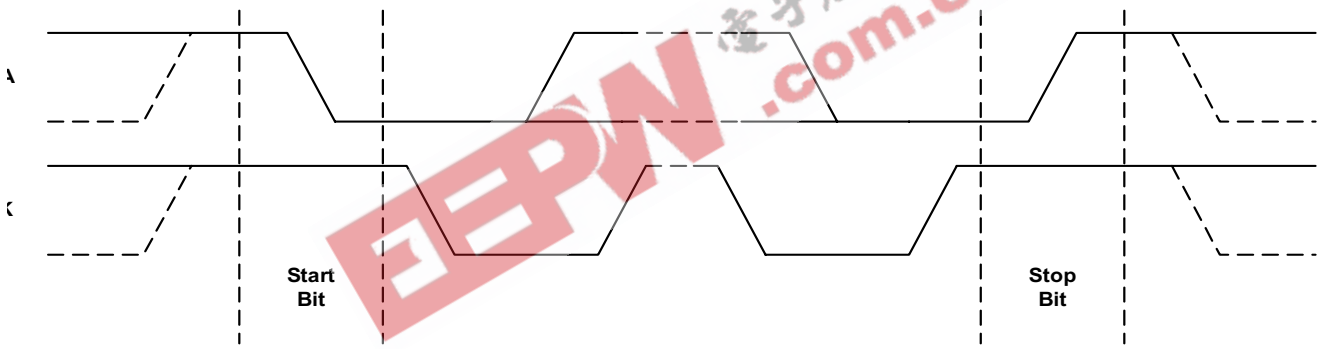


Figure 3. Serial Data Bus Start and Stop Bit

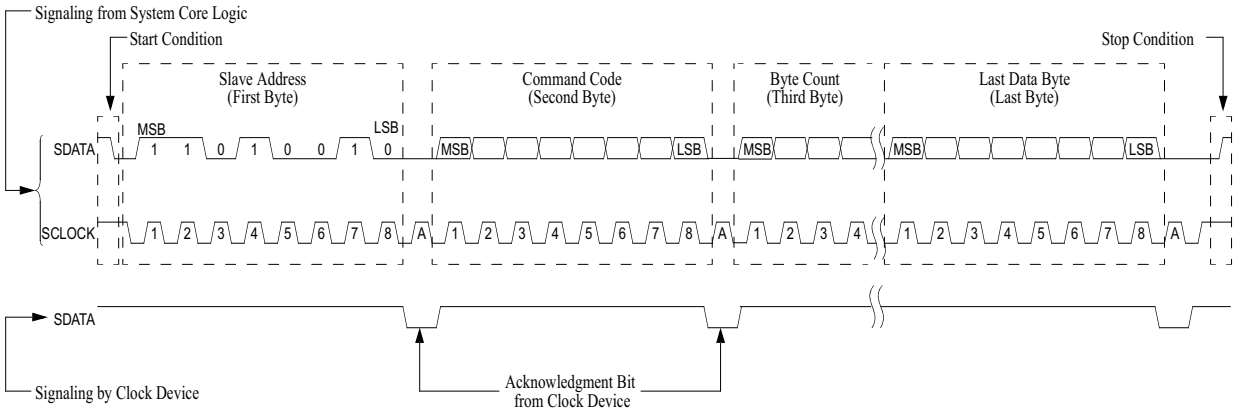


Figure 4. Serial Data Bus Write Sequence

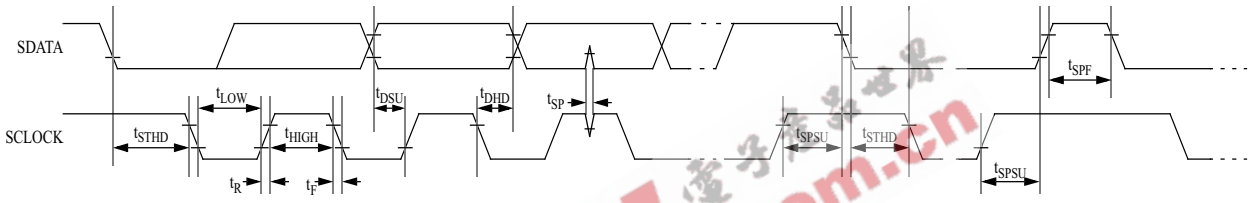


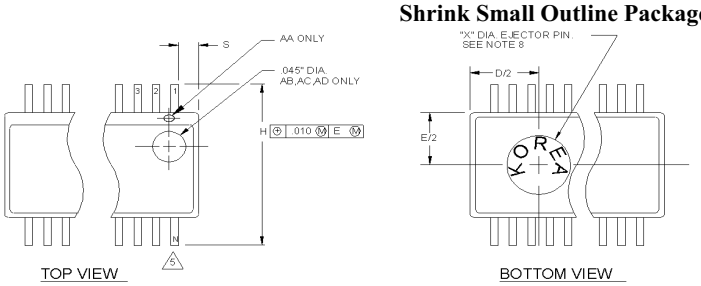
Figure 5. Serial Data Bus Timing Diagrams

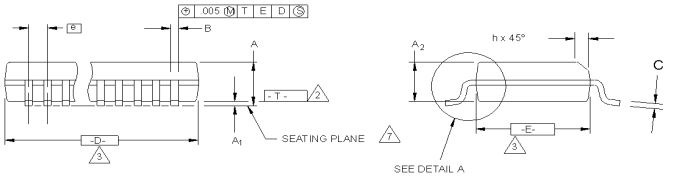
Ordering Information

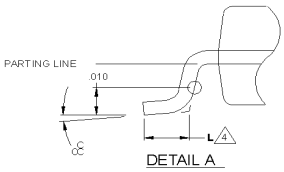
Ordering Code	Package Type	Temperature Range
W191HI	16 pin = SSOP (150 mil)	I = Industrial
W191H	16 pin = SSOP (150 mil)	Commercial

Package Diagrams

Shrink Small Outline Package (SSOP 150 inch)







NOTES:

1. DIMENSIONING & TOLERANCES PER ANSI Y14.5M - 1982.
2. "T" IS A REFERENCE DATUM.
3. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
4. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
8. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
9. CONTROLLING DIMENSION: INCHES.
10. MAXIMUM DIE THICKNESS ALLOWABLE WITHOUT DIE COAT IS .016.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.061	.064	.068	
A_1	.004	.006	.0098	
A_2	.055	.058	.061	
B	.008	.010	.012	
C	.0075	.008	.0098	
D	SEE VARIATIONS			3
E	.150	.155	.157	
e	.025 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			5
S	SEE VARIATIONS			
θC	0°	5°	8°	
X	.085	.093	.100	

NOTE	3						5
VARIATIONS	D			S			N
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
AA	.189	.194	.196	.0020	.0045	.0070	16
AB	.337	.342	.344	.0250	.0275	.0300	24
AC	.337	.342	.344	.0250	.0275	.0300	24
AD	.386	.391	.393	.0250	.0280	.0300	28

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	1.55	1.63	1.73	
A_1	0.127	0.15	0.25	
A_2	1.40	1.47	1.55	
B	0.20	0.25	0.31	
C	0.19	0.20	0.25	
D	SEE VARIATIONS			3
E	3.81	3.94	3.99	
e	0.635 BSC			
H	5.84	5.99	6.20	
h	0.25	0.33	0.41	
L	0.41	0.64	0.89	
N	SEE VARIATIONS			5
S	SEE VARIATIONS			
θC	0°	5°	8°	
X	2.16	2.36	2.54	

NOTE	3						5
VARIATIONS	D			S			N
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
AA	4.80	4.93	4.98	0.05	0.11	0.18	16
AB	8.56	8.69	8.74	1.27	1.33	1.40	20
AC	8.56	8.69	8.74	0.64	0.70	0.76	24
AD	9.80	9.93	9.98	0.64	0.71	0.76	28