Six Output Peak Reducing EMI Solution

Features

- **Cypress PREMIS™ family offering**
- **Generates an EMI optimized clocking signal at the output**
- **Selectable output frequency range**
- **Six 1.25%, 3.75%, or 0% down or center spread outputs**
- **One non-Spread output of Reference input**
- **Integrated loop filter components**
- **Operates with a 3.3V or 5V supply**
- **Low power CMOS design**
- **Available in 24-pin SSOP (Shrink Small Outline Package)**
- **Outputs may be selectively disabled**

Key Specifications

Supply Voltages: .... V_{DD} = 3.3V±5% or V_{DD} = 5V±10%

Frequency Range: .... 28 MHz ≤ F_{in} ≤ 75 MHz

Crystal Reference Range:................. 28 MHz ≤ F_{in} ≤ 40 MHz

Cycle to Cycle Jitter: .... 300 ps (max.)

Selectable Spread Percentage: ....1.25% or 3.75%

Output Duty Cycle: .... 40/60% (worst case)

Output Rise and Fall Time: .... 5 ns (max.)

Table 1. Modulation Width Selection

SS%	W185 Output	W185-5 Output
0	$F_{in} \geq F_{out} \geq F_{in}$ – 1.25%	F_{in} + 0.625% ≥ F_{in} ≥ – 0.625%
1	$F_{in} \geq F_{out} \geq F_{in}$ – 3.75%	F_{in} + 1.875% ≥ F_{in} ≥ –1.875%

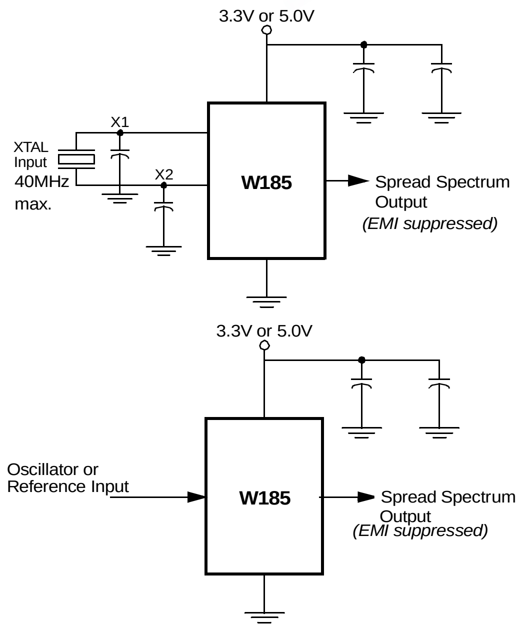
Table 2. Frequency Range Selection

FS2	FS1	Frequency Range
0	0	28 MHz ≤ F_{IN} ≤ 38 MHz
0	1	38 MHz ≤ F_{IN} ≤ 48 MHz
1	0	46 MHz ≤ F_{IN} ≤ 60 MHz
1	1	58 MHz ≤ F_{IN} ≤ 75 MHz

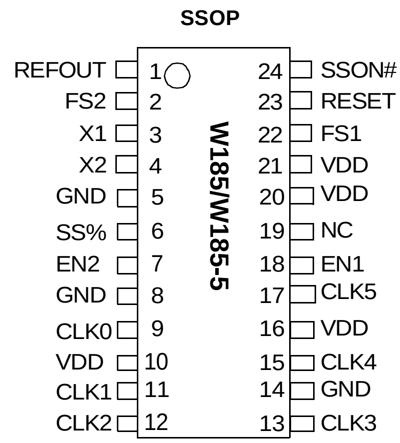
Table 3. Output Enable

EN1	EN2	CLK0:4	CLK5
0	0	Low	Low
0	1	Low	Active
1	0	Active	Low
1	1	Active	Active

Simplified Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CLK0:5	9, 11, 12, 13, 15, 17	O	***Modulated Frequency Outputs:*** Frequency modulated copies of the unmodulated input clock (SSON# asserted).
CLKIN or X1	3	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
NC or X2	4	I	***Crystal Connection:*** If using an external reference, this pin must be left unconnected.
SS%	6	I	***Modulation Width Selection:*** When Spread Spectrum feature is turned on, this pin is used to select the amount of variation and peak EMI reduction that is desired on the output signal. This pin has an internal pull-up resistor.
Reset	23	I	***Modulation Profile Restart:*** A rising edge on this input restarts the modulation pattern at the beginning of its defined path. This pin has an internal pull-down resistor.
REFOUT	1	O	***Non-Modulated Output:*** This pin provides a copy of the reference frequency. This output will not have the Spread Spectrum feature enabled regardless of the state of logic input SSON#.
EN1:2	18, 7	I	***Output Enable Select Pins:*** These pins control the activity of specific output buffers. See *Table 3* on page 1.
SSON#	24	I	***Spread Spectrum Control (Active LOW):*** Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
FS1:2	22, 2	I	***Frequency Selection Bit 1 and 2:*** These pins select the frequency of operation. Refer to *Table 1*. These pins have internal pull-up resistors.
VDD	10, 16, 20, 21	P	***Power Connection:*** Connected to 3.3V or 5V power supply.
GND	5, 8, 14	G	***Ground Connection:*** This should be connected to the common ground plane.
NC	19	NC	***No Connect:*** This pin should be left floating.

Overview

The W185 products are one series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low-frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram shows a simple implementation.

Functional Description

The W185 uses a Phase-Locked Loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. (Note: For the W184 the output frequency is nominally equal to the input frequency.) The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (FS1:2 pins), the frequency range can be set. Spreading percentage may be selected as either 1.25% or 3.75% (see *Table 1*).

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentage options are provided.

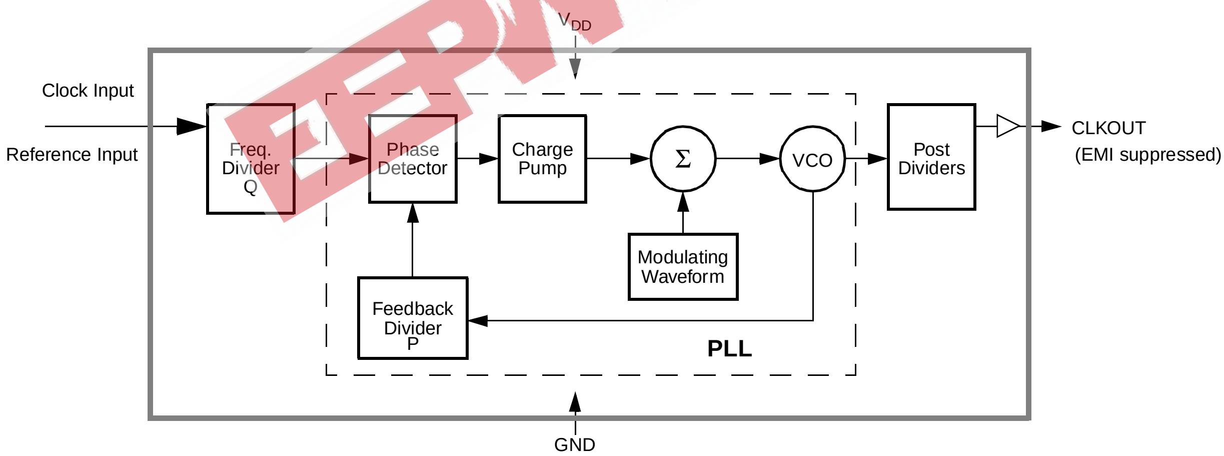


Figure 1. Functional Block Diagram

Spread Spectrum Frequency Timing Generation

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 2*.

As shown in *Figure 2*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*log_{10}(P) + 9*log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 3*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. *Figure 3* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

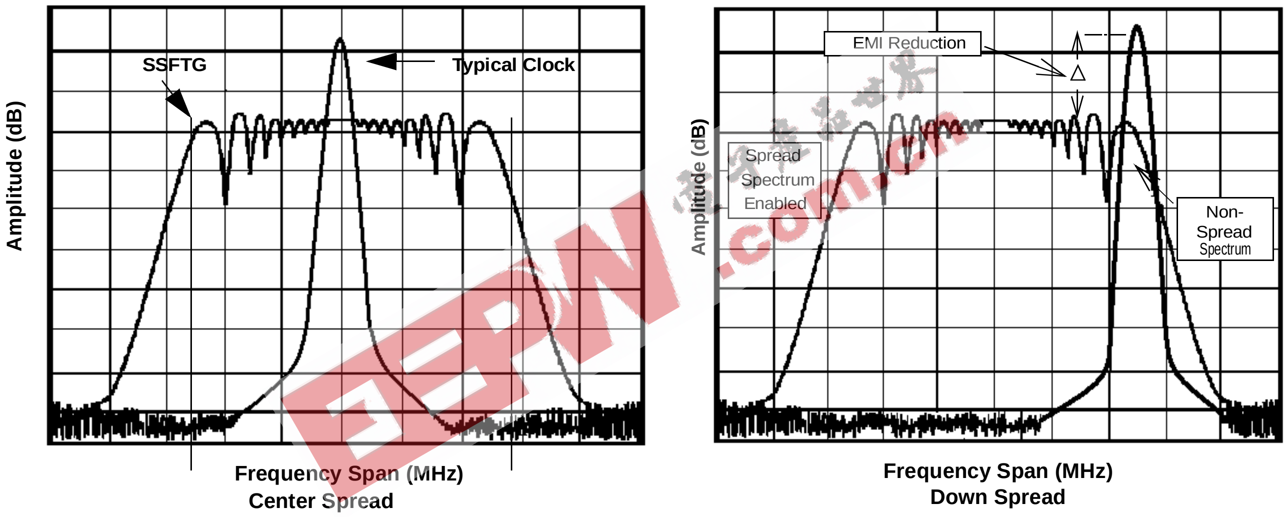


Figure 2. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

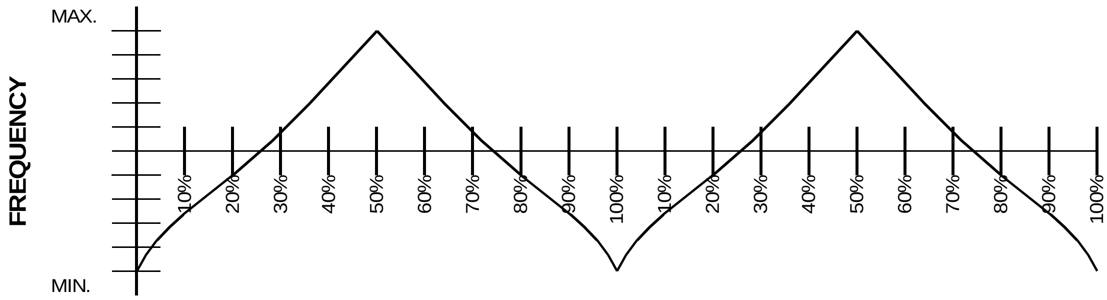


Figure 3. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 3.3V ±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			18	32	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 1	–50			µA
I_{IH}	Input High Current	Note 1			50	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V		15		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V		15		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			500		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

Note:

1. Inputs FS1:2 have a pull-up resistor; Input SSON# has a pull-down resistor.

DC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 5V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			30	50	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				$0.15V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 1	–100			µA
I_{IH}	Input High Current	Note 1			50	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 5V		24		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 5V		24		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			500		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±5% or 5V±10%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{OSC}	Internal Xtal Oscillator Frequency	Xtal connected to X1, X2	28		40	MHz
f_{IN}	Input Frequency	External reference	28		75	MHz
f_{OUT}	Output Frequency	Spread Off, FS2:1 per *Table 2*	28		75	MHz
t_R	Output Rise Time	15-pF load 0.8V–2.4V		2	5	ns
t_F	Output Fall Time	15-pF load 2.4 –0.8V		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			250	300	ps
EMI_{RED}	Harmonic Reduction	f_{out} = 40 MHz, third harmonic measured, reference board, 15-pF load	8			dB
t_{SK}	Output to Output Skew				300	ps

Application Information

Recommended Circuit Configuration

For optimum performance in system applications the power supply decoupling scheme shown in *Figure 4* should be used.

V_{DD} decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10-µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

Recommended Board Layout

Figure 5 shows a recommended 2-layer board layout.

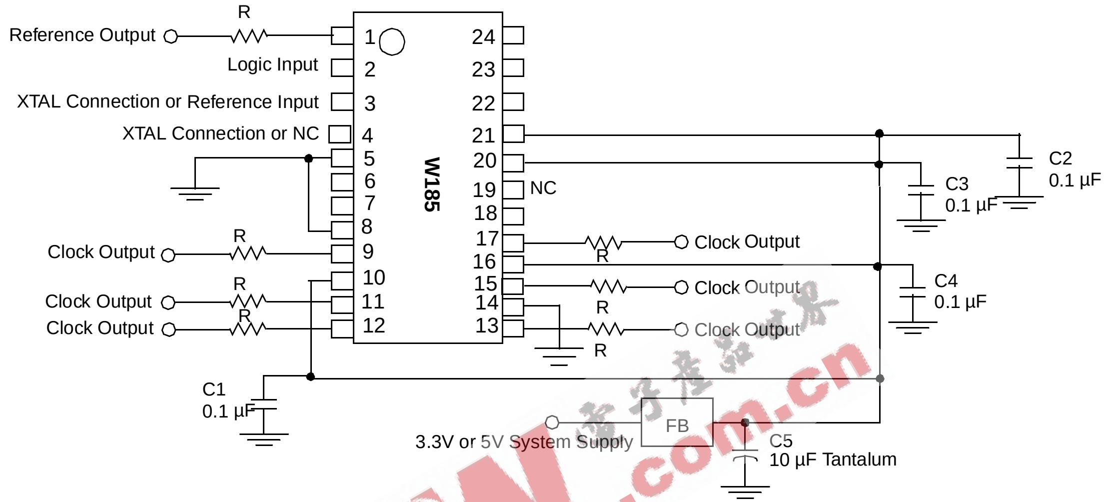


Figure 4. Recommended Circuit Configuration

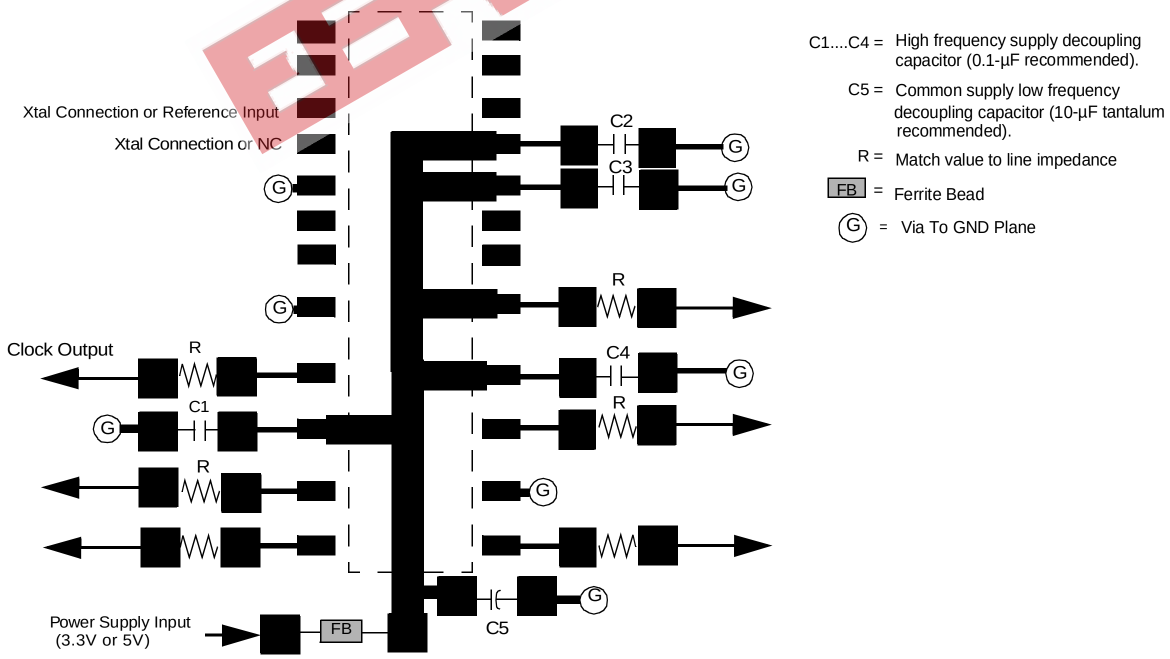


Figure 5. Recommended Board Layout (2-Layer Board)

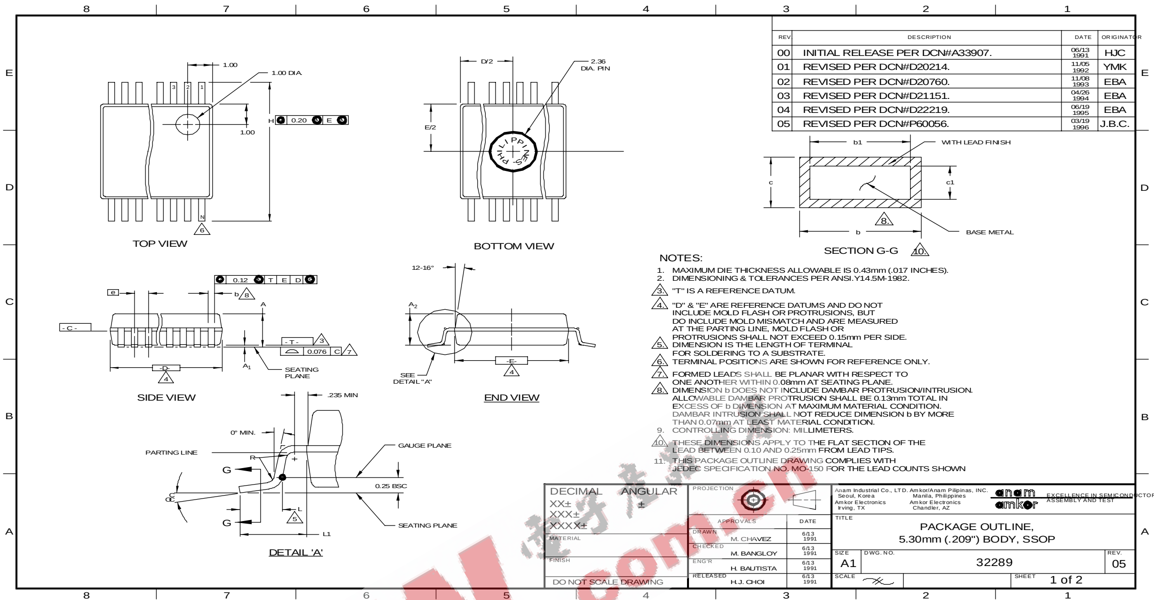
Ordering Information

Ordering Code	Package Name	Package Type
W185 W185-5	H	24-Pin SSOP (209-mil)

Document #: 38-00809-A

Package Diagram

24-Pin Shrink Small Outline Package (SSOP, 209-mil)



THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	1.73	1.86	1.99	
A_1	0.05	0.13	0.21	
A_2	1.68	1.73	1.78	
b	0.25	-	0.38	8,10
b1	0.25	0.30	0.33	10
c	0.09	-	0.20	10
c1	0.09	0.15	0.16	10
D	SEE VARIATIONS			4
E	5.20	5.30	5.38	4
e	0.65 BSC			
H	7.65	7.80	7.90	
L	0.63	0.75	0.95	5
L1	1.25 REF.			
N	SEE VARIATIONS			6
α	0°	4°	8°	
R	0.09	0.15		

NOTE VARIATIONS	4 D MIN.	NOM.	MAX.	6 N
AA	6.07	6.20	6.33	14
AB	6.07	6.20	6.33	16
AC	7.07	7.20	7.33	20
AD	8.07	8.20	8.33	24
AE	10.07	10.20	10.33	28
AF	10.07	10.20	10.33	30

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.068	.073	.078	
A_1	.002	.005	.008	
A_2	.066	.068	.070	
b	.010	-	.015	8,10
b1	.010	.012	.013	10
c	.004	-	.008	10
c1	.004	.006	.006	10
D	SEE VARIATIONS			4
E	.205	.209	.212	4
e	.0256 BSC			
H	.301	.307	.311	
L	.025	.030	.037	5
L1	.049 REF.			
N	SEE VARIATIONS			6
α	0°	4°	8°	
R	.004	.006		

NOTE VARIATIONS	4 D MIN.	NOM.	MAX.	6 N
AA	.239	.244	.249	14
AB	.239	.244	.249	16
AC	.278	.284	.289	20
AD	.318	.323	.328	24
AE	.397	.402	.407	28
AF	.397	.402	.407	30

TITLE: PACKAGE OUTLINE, 5.30mm (.209") BODY, SSOP
SIZE: A1 DWG. NO.: 32289 REV.: 05
SCALE: 8/1 SHEET: 2 of 2