



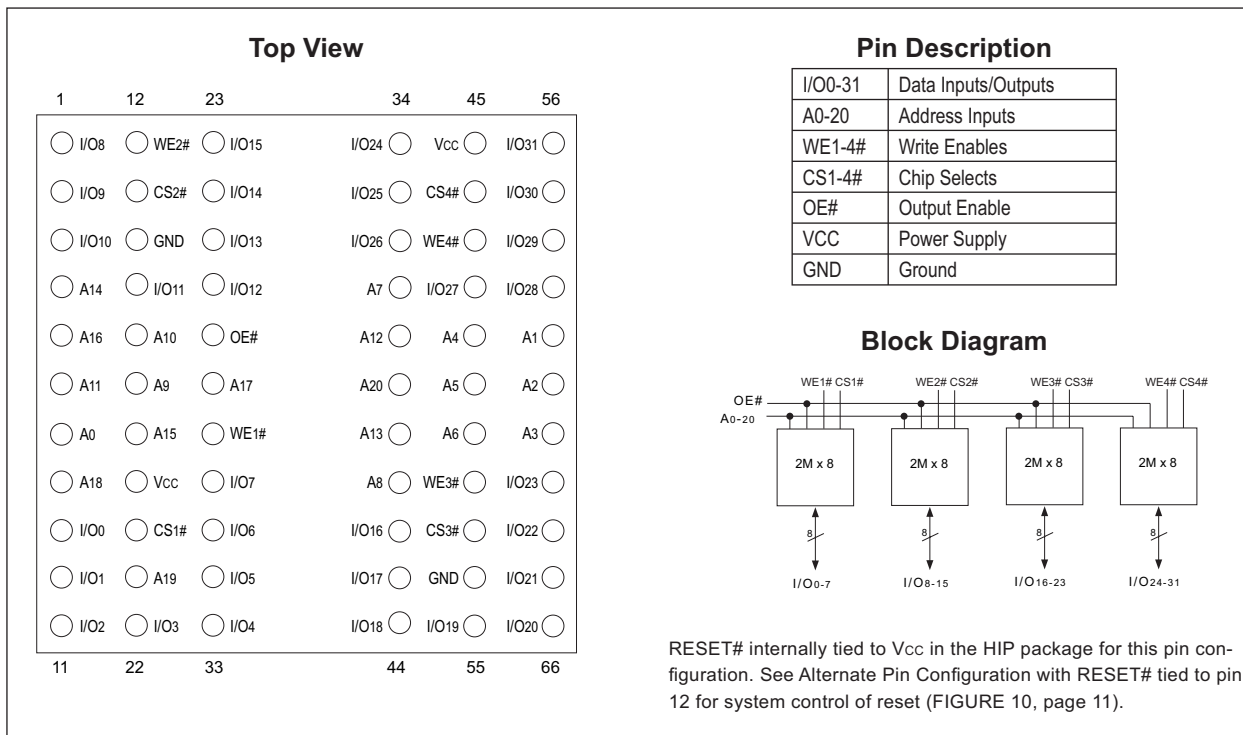
## 2Mx32 5V Flash Module

### FEATURES

- Access Time of 90, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.185" square, Hermetic Ceramic HIP (Package 401).
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880") square (Package 510) 3.56mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (FIGURE 3)
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx32
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity

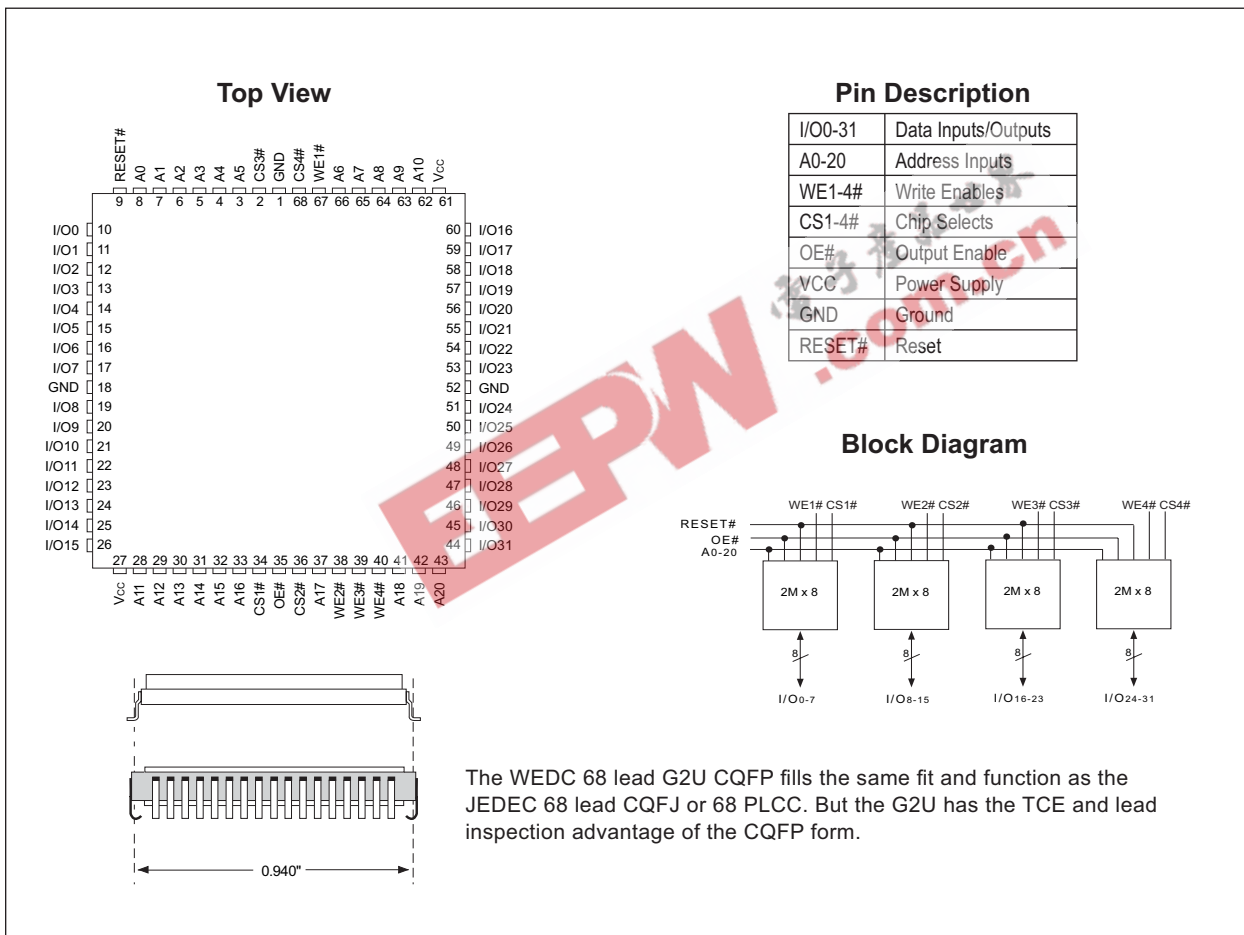
\* This product is subject to change without notice.  
 Note: For programming information refer to Flash Programming 16M5 Application Note.

**FIGURE 1 – PIN CONFIGURATION FOR WF2M32-XHX5**





**FIGURE 2 – PIN CONFIGURATION FOR WF2M32-XG2UX5**





**ABSOLUTE MAXIMUM RATINGS**

| Parameter                                      | Symbol           | Ratings      | Unit   |
|--|------------------|--------------|--------|
| Voltage on Any Pin Relative to V <sub>SS</sub> | V <sub>T</sub>   | -2.0 to +7.0 | V      |
| Power Dissipation                              | P <sub>T</sub>   | 8            | W      |
| Storage Temperature                            | T <sub>stg</sub> | -65 to +125  | °C     |
| Short Circuit Output Current                   | I <sub>OS</sub>  | 100          | mA     |
| Endurance – Write/Erase Cycles (Extended Temp) |                  | 100,000 min  | cycles |
| Data Retention                                 |                  | 20           | years  |

**CAPACITANCE**

T<sub>A</sub> = +25°C, f = 1.0MHz

| Parameter                       | Symbol           | Max | Unit |
|---------------------------------|------------------|-----|------|
| OE# capacitance                 | COE              | 50  | pF   |
| WE1-4# capacitance<br>HIP (PGA) | CWE              | 20  | pF   |
| HIP (Alternate pinout)          | CWE              | 50  | pF   |
| CQFP G4T                        | CWE              | 50  | pF   |
| CQFP G2U                        | CWE              | 20  | pF   |
| G2U (Alternate pinout)          | CWE              | 50  | pF   |
| CS1-4# capacitance              | C <sub>CS</sub>  | 20  | pF   |
| Data I/O capacitance            | C <sub>I/O</sub> | 20  | pF   |
| Address input capacitance       | C <sub>AD</sub>  | 50  | pF   |

This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

| Parameter                    | Symbol          | Min  | Typ | Max                   | Unit |
|------------------------------|-----------------|------|-----|-----------------------|------|
| Supply Voltage               | V <sub>CC</sub> | 4.5  | 5.0 | 5.5                   | V    |
| Ground                       | V <sub>SS</sub> | 0    | 0   | 0                     | V    |
| Input High Voltage           | V <sub>IH</sub> | 2.0  | -   | V <sub>CC</sub> + 0.5 | V    |
| Input Low Voltage            | V <sub>IL</sub> | -0.5 | -   | +0.8                  | V    |
| Operating Temperature (Mil.) | T <sub>A</sub>  | -55  | -   | +125                  | °C   |
| Operating Temperature (Ind.) | T <sub>A</sub>  | -40  | -   | +85                   | °C   |

**DC CHARACTERISTICS – CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter   | Symbol             | Conditions   | Min                  | Max  | Unit |
|---|--------------------|--|----------------------|------|------|
| Input Leakage Current                                   | I <sub>LI</sub>    | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>                          |                      | 10   | μA   |
| Output Leakage Current                                  | I <sub>LOx32</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>                          |                      | 10   | μA   |
| V <sub>CC</sub> Active Current for Read (1)             | I <sub>CC1</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz                                 |                      | 160  | mA   |
| V <sub>CC</sub> Active Current for Program or Erase (2) | I <sub>CC2</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>  |                      | 240  | mA   |
| V <sub>CC</sub> Standby Current                         | I <sub>CC3</sub>   | V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub> , f = 5MHz, RESET# = V <sub>CC</sub> ± 0.3V |                      | 8.0  | mA   |
| Output Low Voltage                                      | V <sub>OL</sub>    | I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> = 4.5   |                      | 0.45 | V    |
| Output High Voltage                                     | V <sub>OH</sub>    | I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5   | 0.85xV <sub>CC</sub> |      | V    |
| Low V <sub>CC</sub> Lock-Out Voltage                    | V <sub>LKO</sub>   |  | 3.2                  | 4.2  | V    |

NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE# CONTROLLED**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                                  | Symbol             |                  | -90 |     | -120 |     | -150 |     | Unit |
|--|--------------------|------------------|-----|-----|------|-----|------|-----|------|
|  |                    |                  | Min | Max | Min  | Max | Min  | Max |      |
| Write Cycle Time                           | t <sub>AVAV</sub>  | t <sub>WC</sub>  | 90  |     | 120  |     | 150  |     | ns   |
| Chip Select Setup Time                     | t <sub>ELWL</sub>  | t <sub>CS</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Write Enable Pulse Width                   | t <sub>WLWH</sub>  | t <sub>WP</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Address Setup Time                         | t <sub>AVWL</sub>  | t <sub>AS</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Data Setup Time                            | t <sub>DVWH</sub>  | t <sub>DS</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Data Hold Time                             | t <sub>WHDX</sub>  | t <sub>DH</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Address Hold Time                          | t <sub>WLAX</sub>  | t <sub>AH</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Write Enable Pulse Width High              | t <sub>WHWL</sub>  | t <sub>WPH</sub> | 20  |     | 20   |     | 20   |     | ns   |
| Duration of Byte Programming Operation (1) | t <sub>WHWH1</sub> |                  |     | 300 |      | 300 |      | 300 | μs   |
| Sector Erase (2)                           | t <sub>WHWH2</sub> |                  |     | 15  |      | 15  |      | 15  | sec  |
| Read Recovery Time before Write            | t <sub>GHWL</sub>  |                  | 0   |     | 0    |     | 0    |     | μs   |
| V <sub>CC</sub> Setup Time                 | t <sub>VCS</sub>   |                  | 50  |     | 50   |     | 50   |     | μs   |
| Chip Programming Time                      |                    |                  |     | 44  |      | 44  |      | 44  | sec  |
| Chip Erase Time (3)                        |                    |                  |     | 256 |      | 256 |      | 256 | sec  |
| Output Enable Hold Time (4)                | t <sub>OEHL</sub>  |                  | 10  |     | 10   |     | 10   |     | ns   |
| RESET# Pulse Width (5)                     | t <sub>RP</sub>    |                  | 500 |     | 500  |     | 500  |     | ns   |

NOTES:

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.
5. RESET# internally tied to V<sub>CC</sub> for the default pin configuration in the HIP package.

**AC CHARACTERISTICS – READ-ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter   | Symbol            |                    | -90 |     | -120 |     | -150 |     | Unit |
|---|-------------------|--------------------|-----|-----|------|-----|------|-----|------|
|   |                   |                    | Min | Max | Min  | Max | Min  | Max |      |
| Read Cycle Time   | t <sub>AVAV</sub> | t <sub>RC</sub>    | 90  |     | 120  |     | 150  |     | ns   |
| Address Access Time   | t <sub>AVQV</sub> | t <sub>ACC</sub>   |     | 90  |      | 120 |      | 150 | ns   |
| Chip Select Access Time   | t <sub>ELQV</sub> | t <sub>CE</sub>    |     | 90  |      | 120 |      | 150 | ns   |
| Output Enable to Output Valid                                     | t <sub>GLQV</sub> | t <sub>OE</sub>    |     | 40  |      | 50  |      | 55  | ns   |
| Chip Select High to Output High Z (1)                             | t <sub>EHQZ</sub> | t <sub>DF</sub>    |     | 20  |      | 30  |      | 35  | ns   |
| Output Enable High to Output High Z (1)                           | t <sub>GHQZ</sub> | t <sub>DF</sub>    |     | 20  |      | 30  |      | 35  | ns   |
| Output Hold from Addresses, CS# or OE# Change, whichever is First | t <sub>AXQX</sub> | t <sub>OH</sub>    | 0   |     | 0    |     | 0    |     | ns   |
| RST Low to Read Mode (1,2)  |                   | t <sub>Ready</sub> |     | 20  |      | 20  |      | 20  | μs   |

NOTES:

1. Guaranteed by design, not tested.
2. RESET# internally tied to V<sub>CC</sub> for the default pin configuration in the HIP package.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                                  | Symbol             |                  | -90 |     | -120 |     | -150 |     | Unit |
|--|--------------------|------------------|-----|-----|------|-----|------|-----|------|
|  |                    |                  | Min | Max | Min  | Max | Min  | Max |      |
| Write Cycle Time                           | t <sub>AVAV</sub>  | t <sub>wc</sub>  | 90  |     | 120  |     | 150  |     | ns   |
| Write Enable Setup Time                    | t <sub>wLEL</sub>  | t <sub>ws</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Chip Select Pulse Width                    | t <sub>eLEH</sub>  | t <sub>cp</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Address Setup Time                         | t <sub>aVEL</sub>  | t <sub>as</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Data Setup Time                            | t <sub>dVEH</sub>  | t <sub>ds</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Data Hold Time                             | t <sub>eHDX</sub>  | t <sub>dh</sub>  | 0   |     | 0    |     | 0    |     | ns   |
| Address Hold Time                          | t <sub>eLAX</sub>  | t <sub>ah</sub>  | 45  |     | 50   |     | 50   |     | ns   |
| Chip Select Pulse Width High               | t <sub>eHEL</sub>  | t <sub>cpH</sub> | 20  |     | 20   |     | 20   |     | ns   |
| Duration of Byte Programming Operation (1) | t <sub>wHWH1</sub> |                  |     | 300 |      | 300 |      | 300 | μs   |
| Sector Erase Time (2)                      | t <sub>wHWH2</sub> |                  |     | 15  |      | 15  |      | 15  | sec  |
| Read Recovery Time                         | t <sub>gHEL</sub>  |                  | 0   |     | 0    |     | 0    |     | μs   |
| Chip Programming Time                      |                    |                  |     | 44  |      | 44  |      | 44  | sec  |
| Chip Erase Time (3)                        |                    |                  |     | 256 |      | 256 |      | 256 | sec  |
| Output Enable Hold Time (4)                | t <sub>oEH</sub>   |                  | 10  |     | 10   |     | 10   |     | ns   |

NOTES:

1. Typical value for t<sub>wHWH1</sub> is 7μs.
2. Typical value for t<sub>wHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 3 – AC TEST CIRCUIT

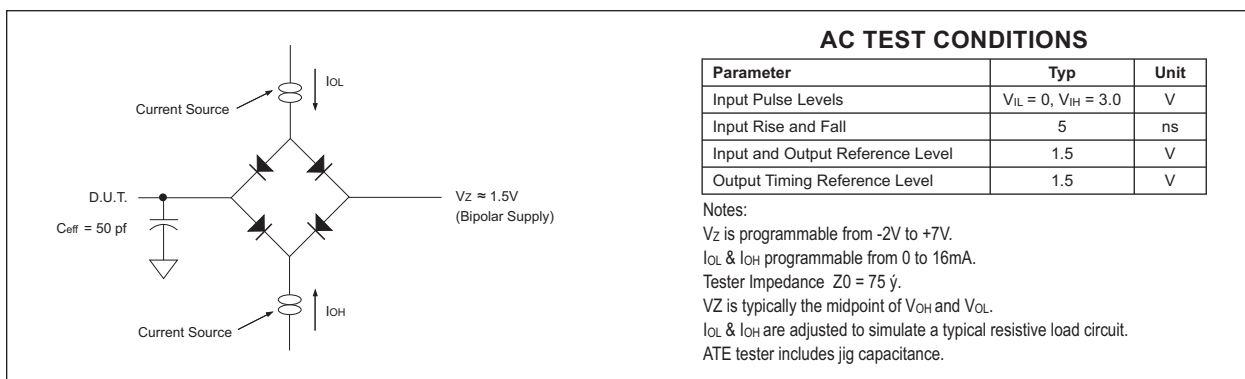


FIGURE 4 – RESET TIMING DIAGRAM

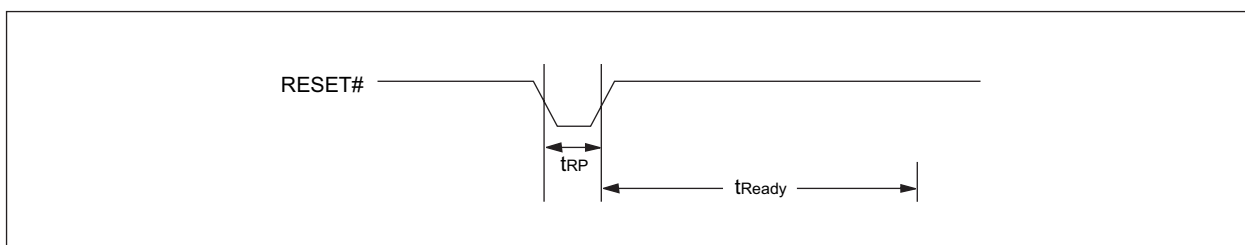




FIGURE 5 – AC WAVEFORMS FOR READ OPERATIONS

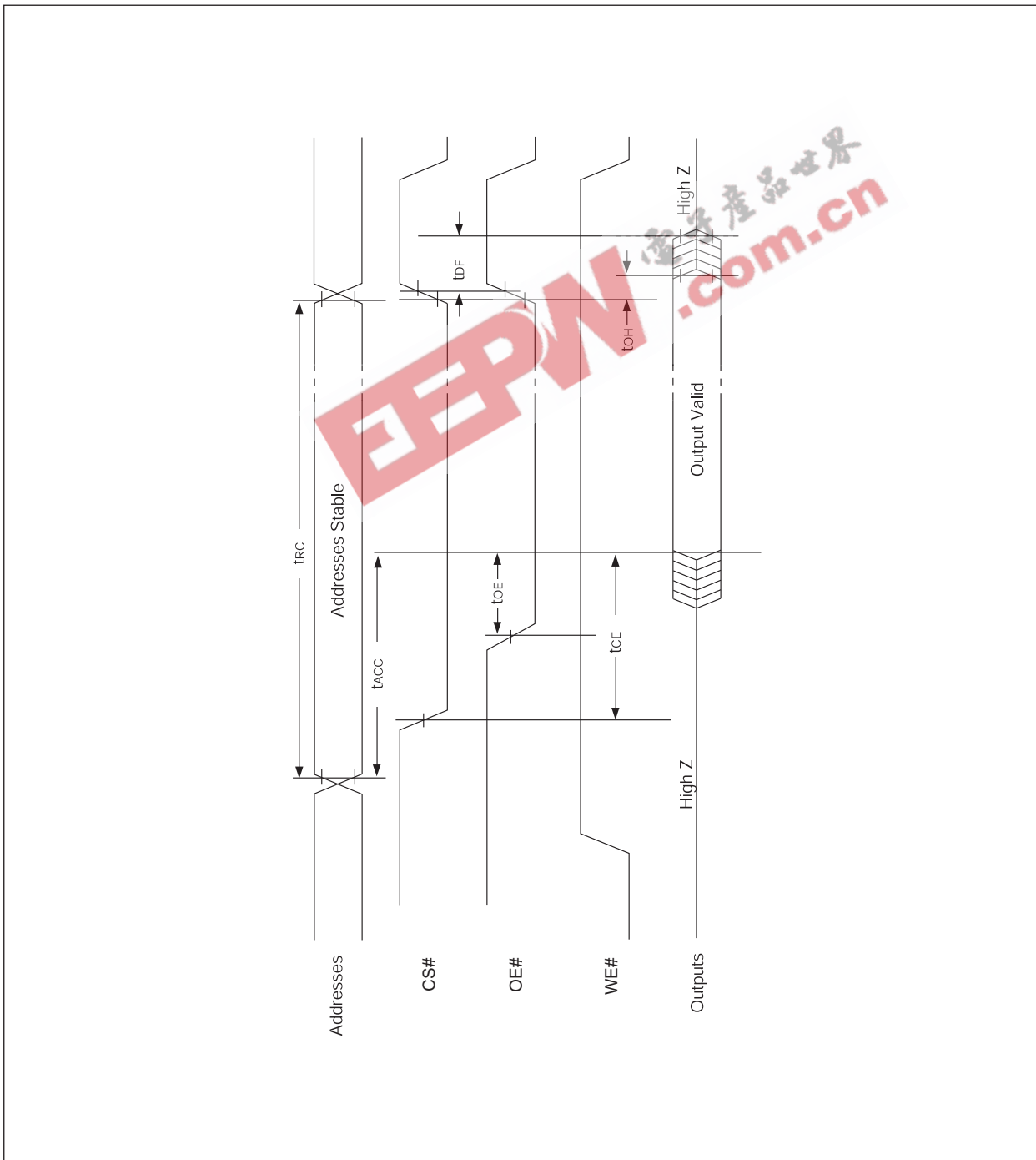
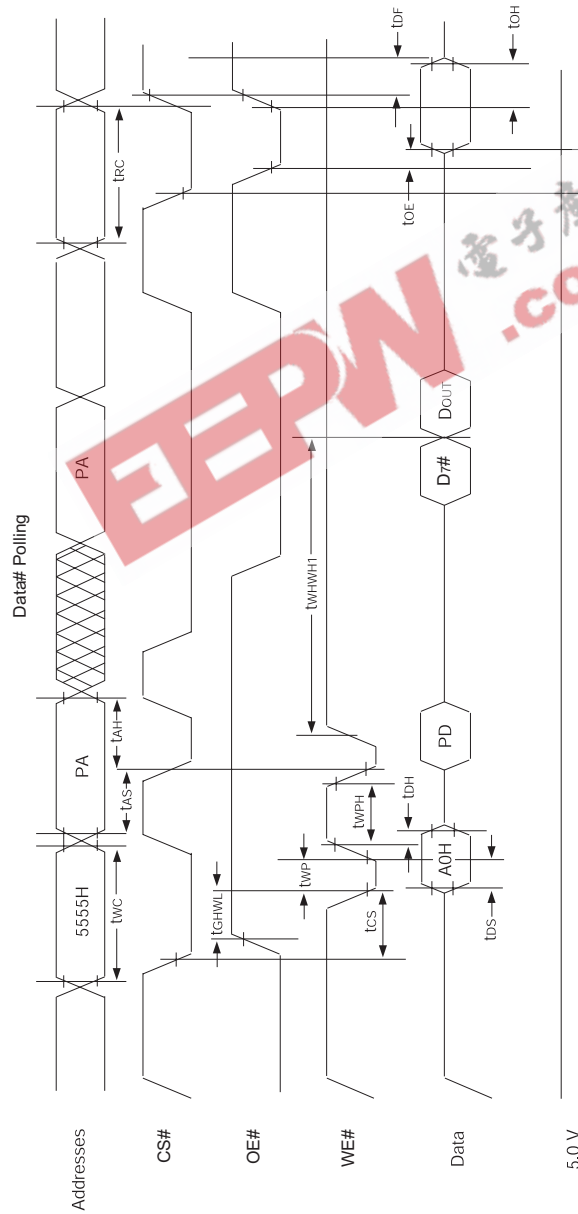




FIGURE 6 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED

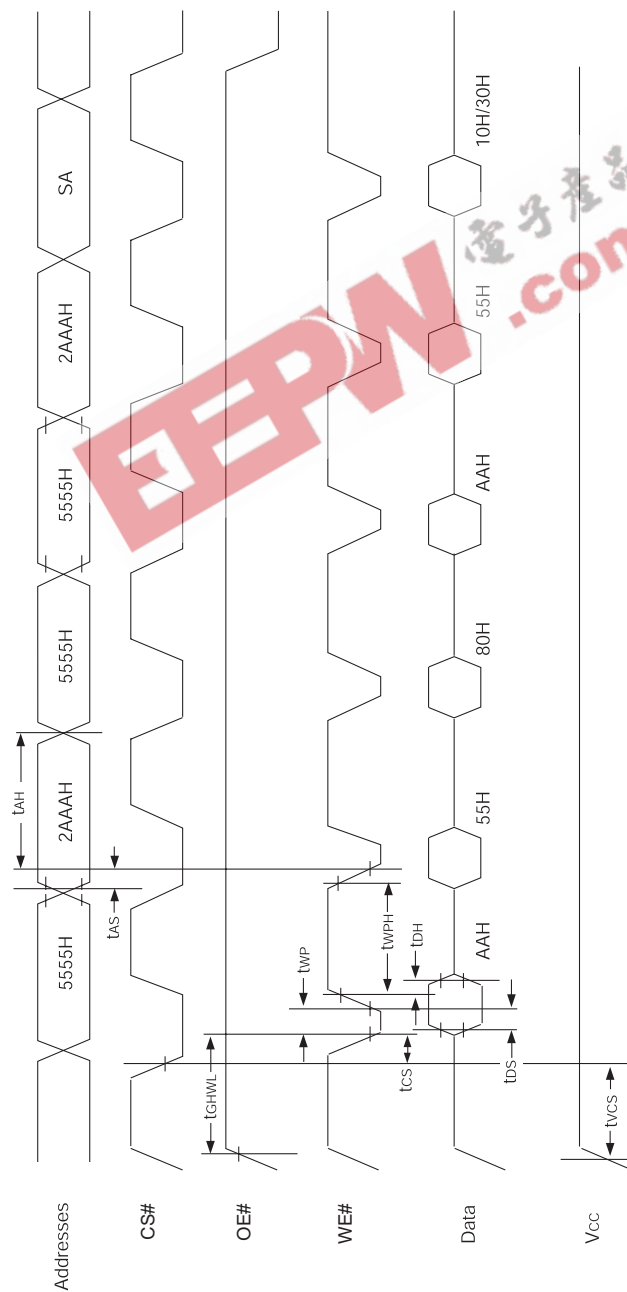


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIGURE 7 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:  
1. SA is the sector address for Sector Erase.





FIGURE 8 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

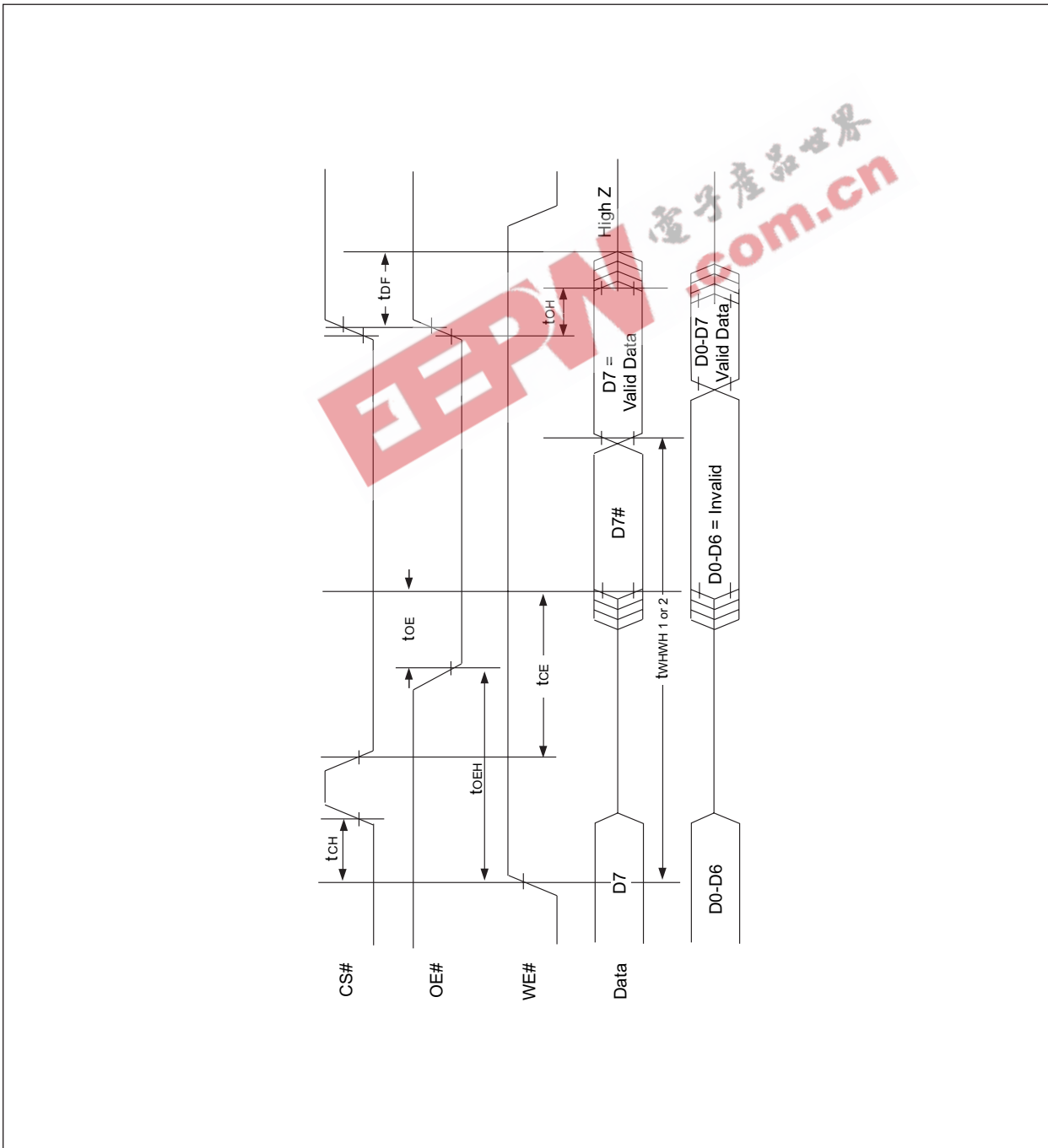
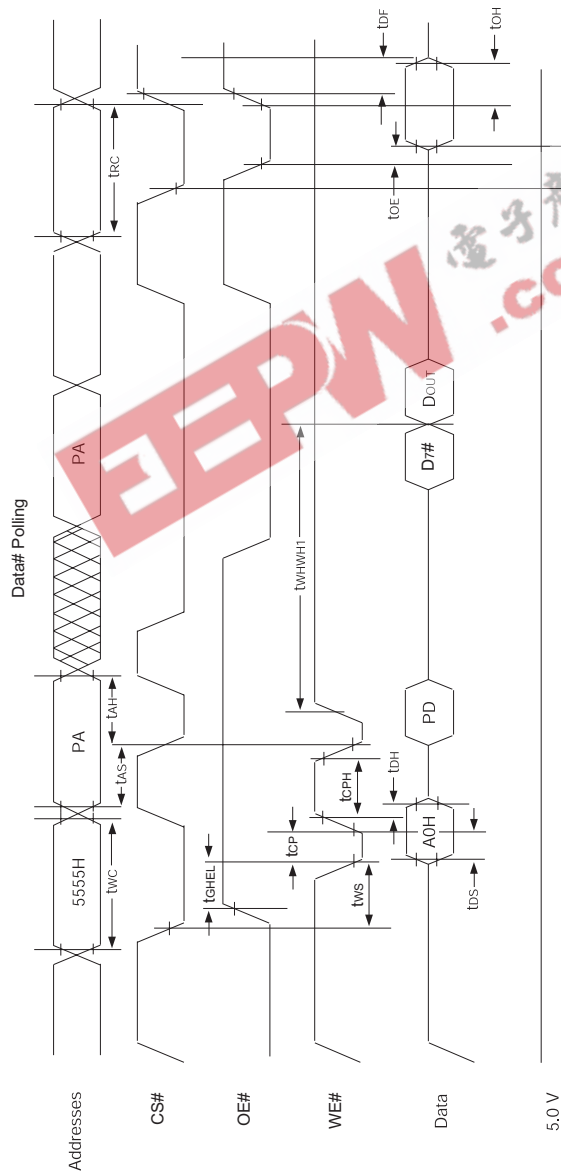




FIGURE 9 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



Notes:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. D<sub>OUT</sub> is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



FIGURE 10 – ALTERNATE PIN CONFIGURATION FOR WF2M32I-XHX5

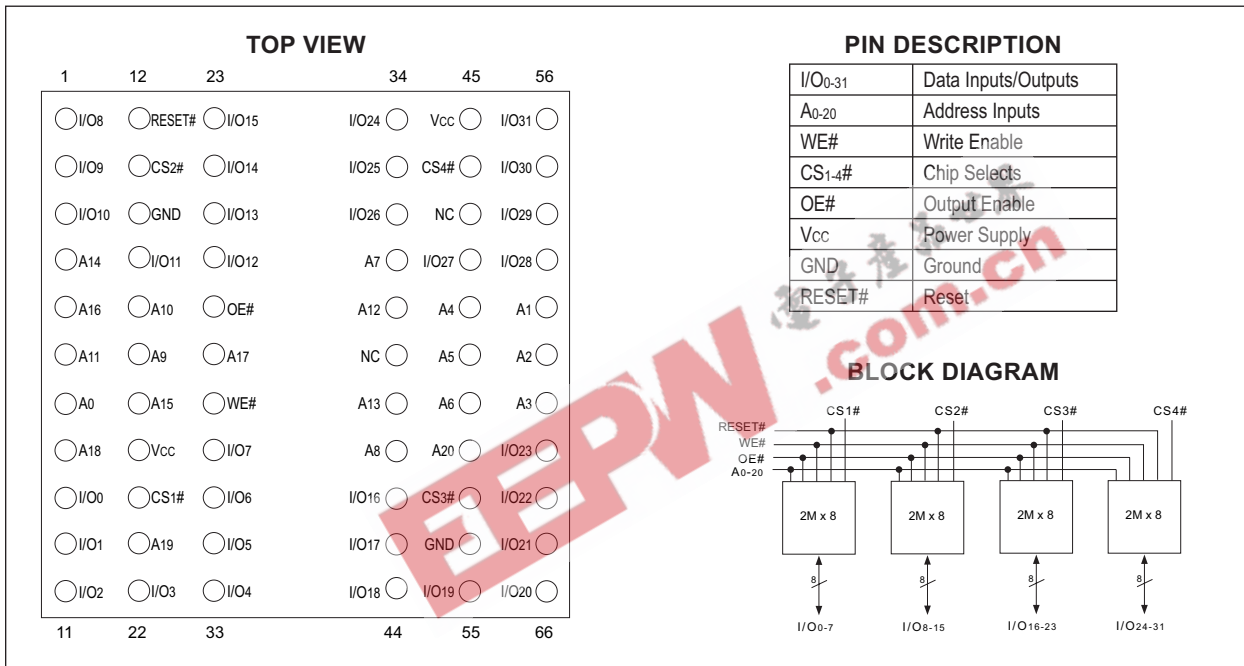
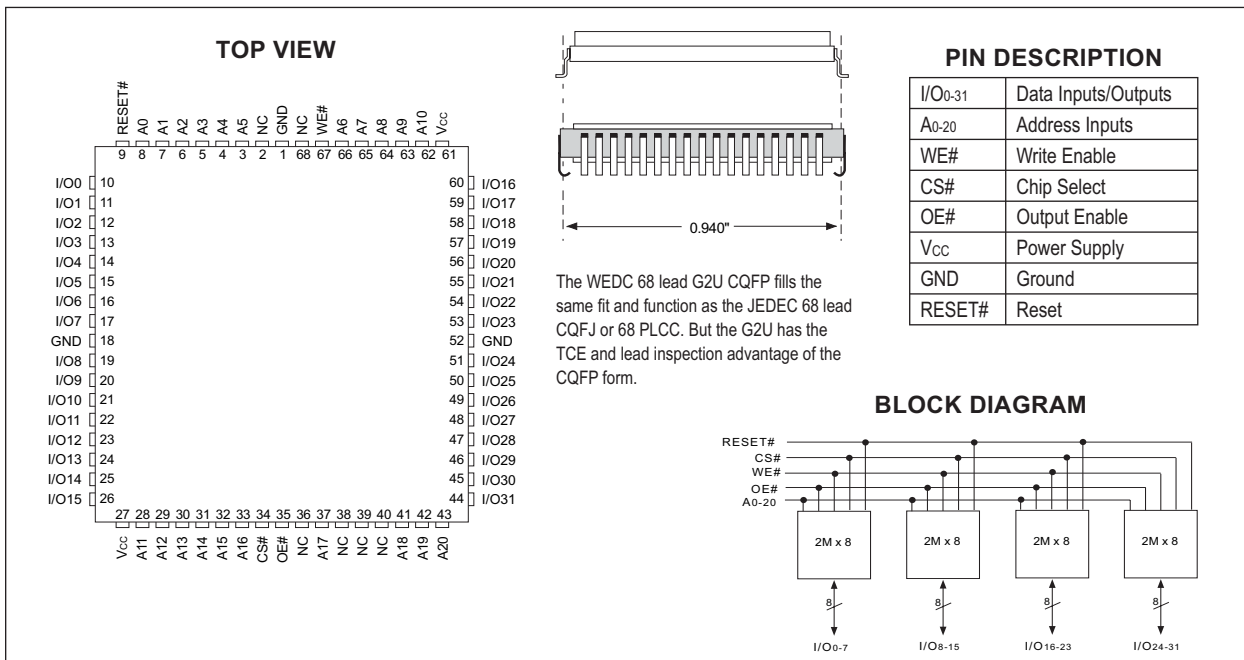
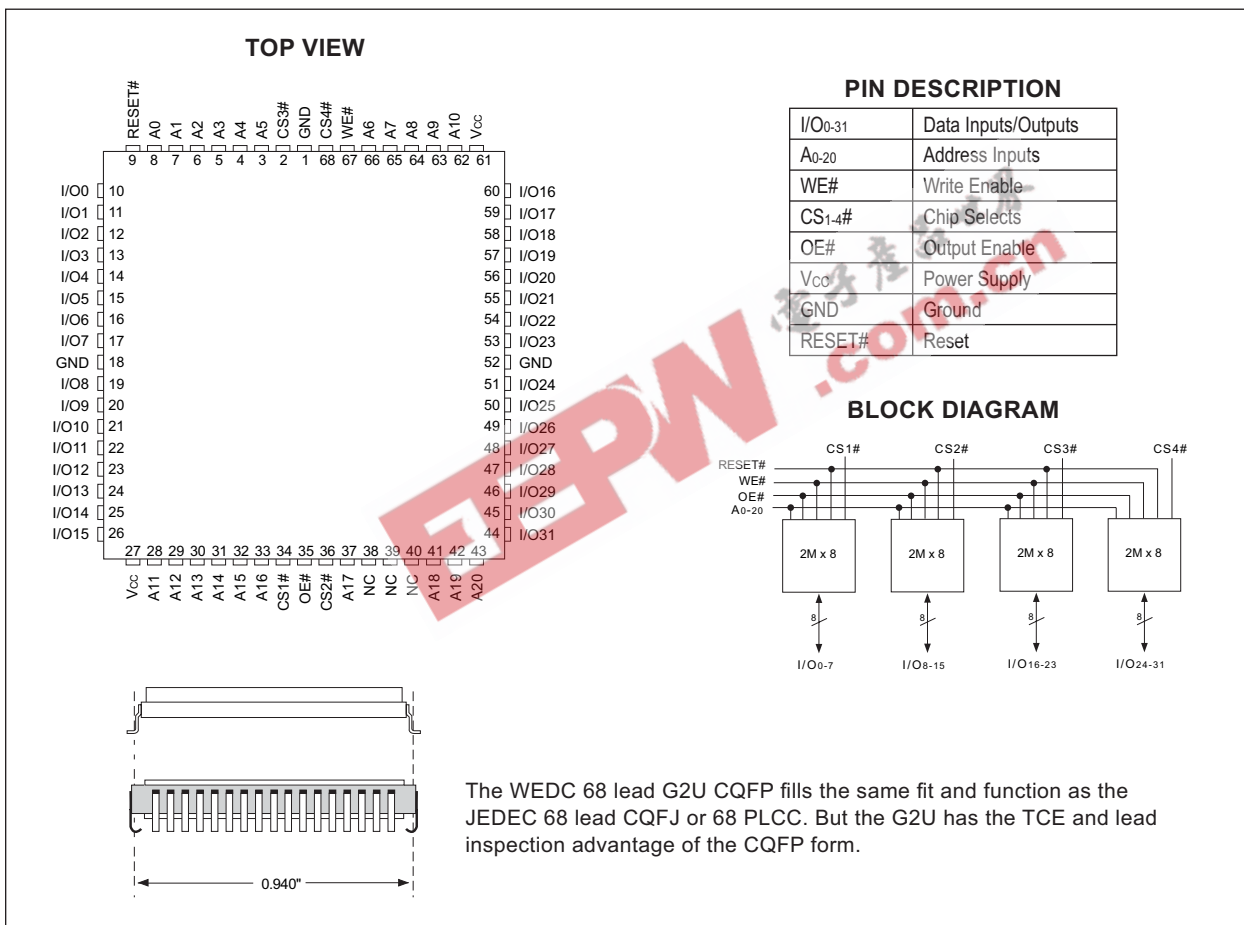


FIGURE 11 – ALTERNATE PIN CONFIGURATION FOR WF2M32U-XG2UX5



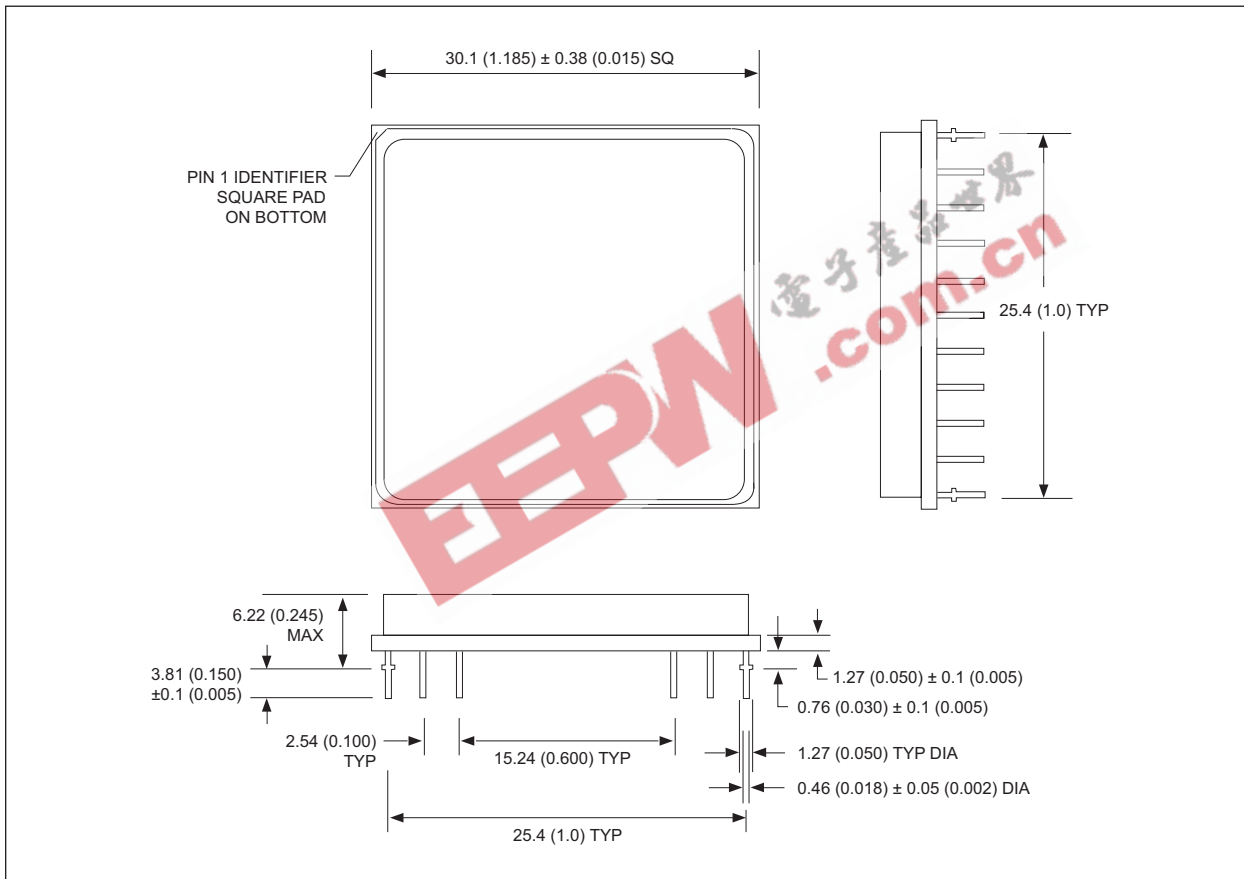


**FIGURE 12 – PIN CONFIGURATION FOR WF2M32I-XG2UX5**





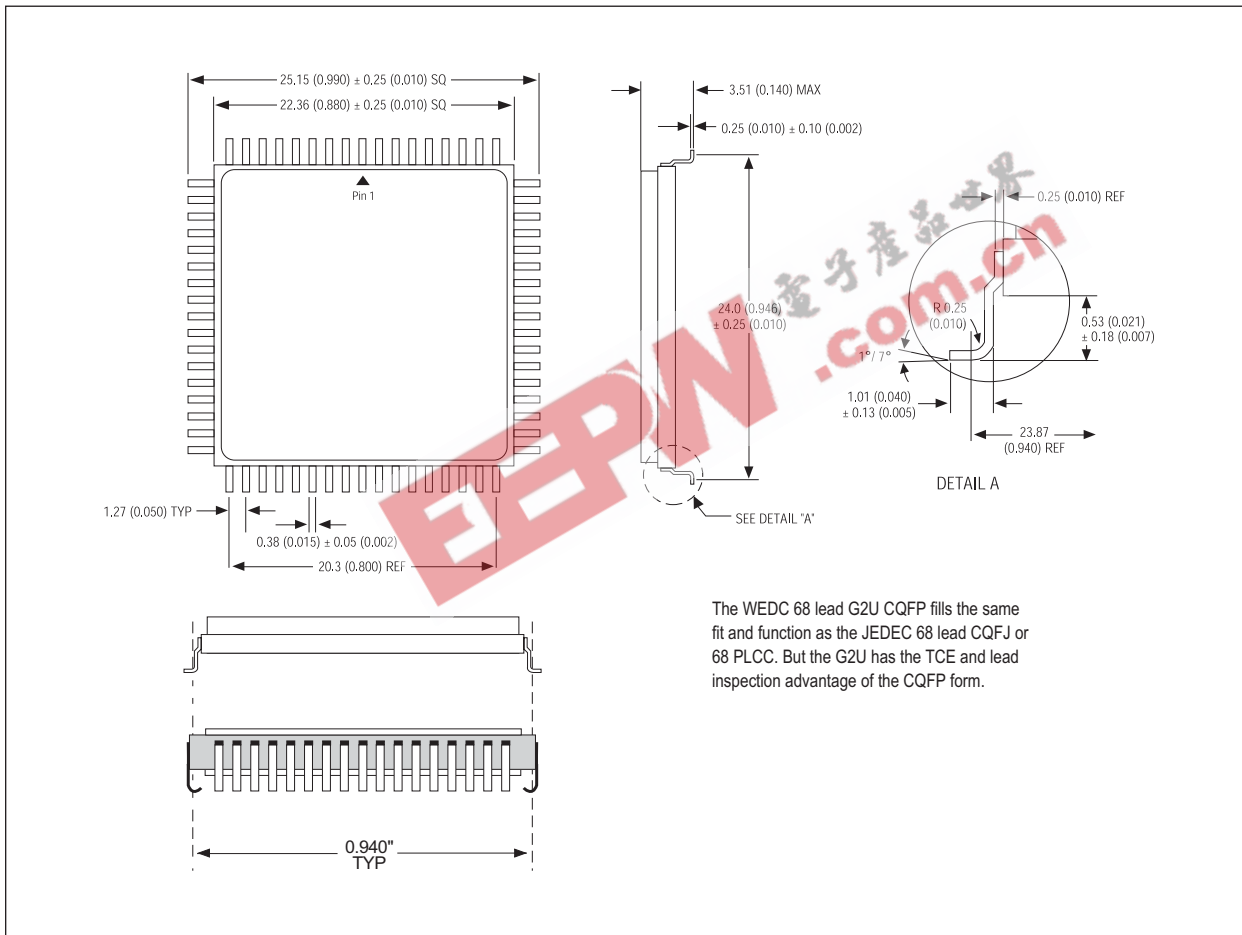
**PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

**W F 2M32 X - XXX X X 5 X**

**LEAD FINISH:**

- Blank = Gold plated leads
- A = Solder dip leads

**V<sub>PP</sub> PROGRAMMING VOLTAGE**

5 = 5 V

**DEVICE GRADE:**

- Q = Compliant -55°C to +125°C
- M = Military -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

- H = Ceramic Hex In line Package, HIP (Package 401)
- G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

**ACCESS TIME (ns)**

**IMPROVEMENT MARK**

- **For HIP Package**
  - Blank = 4CS# and 4WE#
  - I = 4CS# and 1WE#, RESET#
- **For G2U Package**
  - Blank = 4CS# and 4WE#
  - U = 1CS# and 1WE#
  - I = 4CS# and 1WE#, RESET#

**ORGANIZATION, 2M x 32**

User configurable as 4M x 16 or 8M x 8  
(Except WF2M32U-XG2UX which is 32 bit wide only.)

**Flash**

**WHITE ELECTRONIC DESIGNS CORP.**