



## 512Kx32 SRAM 3.3V MULTI-CHIP PACKAGE

### FEATURES

- Access Times of 12, 15, 17, 20ns
- Packaging
  - 143 PBGA, 16mm x 18mm, 288mm<sup>2</sup>
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ± 10% Power Supply
- Low Power Data Retention 'L' Option
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.

This product is subject to change without notice.

### PIN CONFIGURATION FOR WEDPS512K32V-XBX

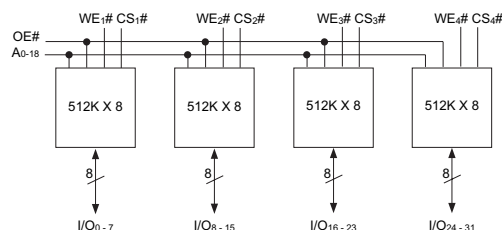
Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	-	A2	A1	A0	GND	GND	VCC	VCC	A18	A17	A16	GND
B	CS2#	A3	A4	D14	D15	NC	CS4#	D24	D25	OE#	A15	NC
C	D9	D8	NC	D12	D13	GND	VCC	D26	D27	WE4#	D31	D30
D	D10	D11	GND	GND	GND	GND	VCC	VCC	VCC	VCC	D28	D29
E	WE2#	GND	GND	GND	GND	GND	VCC	VCC	VCC	VCC	VCC	NC
F	GND	GND	GND	GND	GND	GND	VCC	VCC	VCC	VCC	VCC	VCC
G	VCC	VCC	VCC	VCC	VCC	VCC	GND	GND	GND	GND	GND	GND
H	CS1#	VCC	VCC	VCC	VCC	VCC	GND	GND	GND	GND	GND	NC
J	D1	D0	VCC	VCC	VCC	VCC	GND	GND	GND	GND	D23	D22
K	D2	D3	NC	D7	D5	VCC	GND	D17	D16	CS3#	D20	D21
L	WE1#	A6	A5	D6	D4	NC	WE3#	D19	D18	A14	A13	NC
M	GND	A7	A8	A9	vcc	vcc	GND	GND	A10	A11	A12	vcc

### Pin Description

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-18</sub>	Address Inputs
WE <sub>1-4#</sub>	Write Enables
CS <sub>1-4#</sub>	Chip Selects
OE#	Output Enable
V <sub>cc</sub>	Power Supply
GND	Ground
NC	Not Connected

### Block Diagram





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	4.6	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	4.6	V

**TRUTH TABLE**

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

**BGA THERMAL RESISTANCE**

Parameter	Symbol	Max	Unit	Note
Junction to Ambient (No Airflow)	Theta JA	16.9	°C/W	1
Junction to Ball	Theta JB	11.3	°C/W	1
Junction to Case (Top)	Theta JC	9.8	°C/W	1

NOTE: Refer to Application Note "PBGA Thermal Resistance Correlation" at [www.wedc.com](http://www.wedc.com) in the application notes section for modeling conditions.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V

**CAPACITANCE**

T<sub>a</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF
WE <sub>1-4</sub> # capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
CS <sub>1-4</sub> # capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

V<sub>CC</sub> = 3.3V ± 0.3V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current (x 32 Mode)	I <sub>CC</sub> x 32	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		400	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		120	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.0mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V.  
Contact factory for low power option.

**DATA RETENTION CHARACTERISTICS (WEDPS512K32LV-XBX only)**

-55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Data Retention Voltage	V <sub>CC</sub>	V <sub>CC</sub> = 2.19V	2.19		V
Data Retention Current	I <sub>CCDR</sub>	CS = V <sub>CC</sub> - 0.2V		8.0	mA



**AC CHARACTERISTICS**

V<sub>CC</sub> = 3.3V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	12		15		17		20		ns
Address Access Time	t <sub>AA</sub>		12		15		17		20	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		12		15		17		20	ns
Output Enable to Output Valid	t <sub>OE</sub>		7		8		8		10	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	1		1		1		1		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		7		8		8		10	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		7		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**

V<sub>CC</sub> = 3.3V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	12		15		17		20		ns
Chip Select to End of Write	t <sub>CW</sub>	10		12		12		14		ns
Address Valid to End of Write	t <sub>AW</sub>	10		12		12		14		ns
Data Valid to End of Write	t <sub>DW</sub>	8		9		9		10		ns
Write Pulse Width	t <sub>WP</sub>	10		12		14		14		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	2		2		3		3		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		7		8		8		9	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIGURE 4 – AC TEST CIRCUIT**

The diagram shows a Device Under Test (D.U.T.) connected to a bipolar supply (V<sub>Z</sub> = 1.5V). Two current sources are connected to the D.U.T. terminals, labeled I<sub>oL</sub> and I<sub>oH</sub>. A capacitor C<sub>eff</sub> = 50 pf is connected to the D.U.T. input. The supply is labeled as a Bipolar Supply.

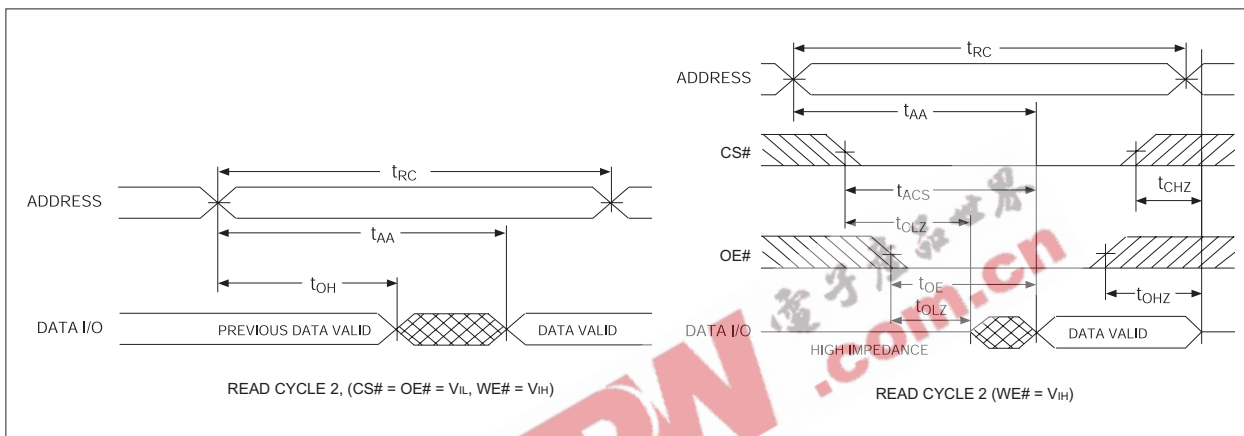
**AC Test Conditions**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

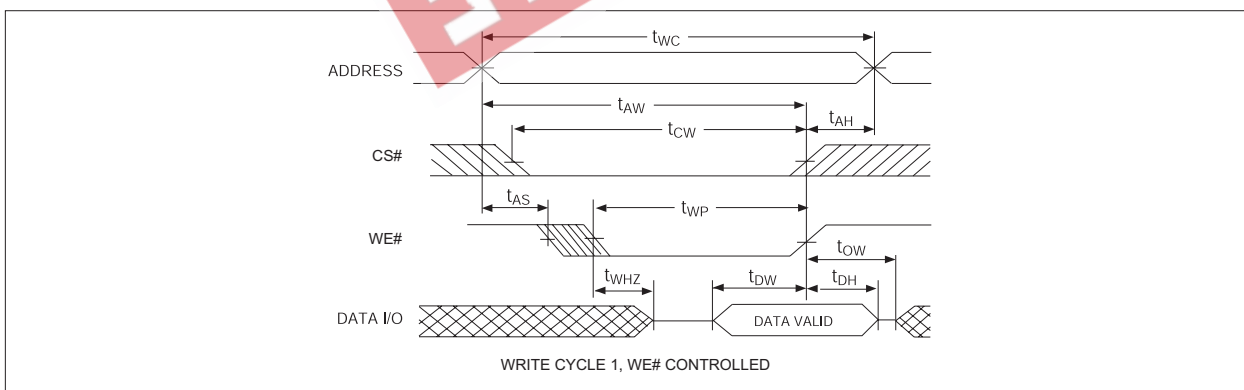
Notes:  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>oL</sub> & I<sub>oH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>oL</sub> & I<sub>oH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



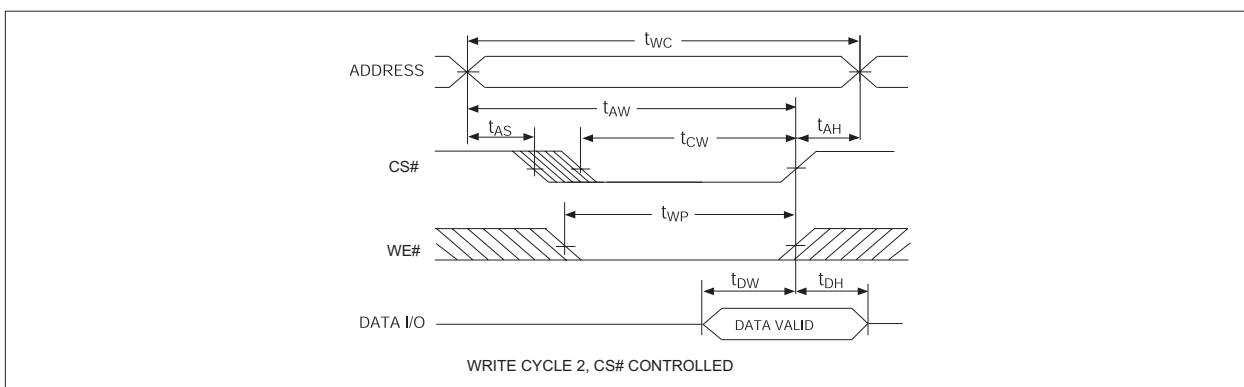
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED



WRITE CYCLE - CS# CONTROLLED







ORDERING INFORMATION

**WED P S 512K 32 L V - XX X X**

WHITE ELECTRONIC DESIGNS CORP.

PLASTIC

SRAM

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

OPTIONS:

L = Low power data retention

Low Voltage Supply 3.3V ± 10%

ACCESS TIME (ns)

PACKAGE TYPE:

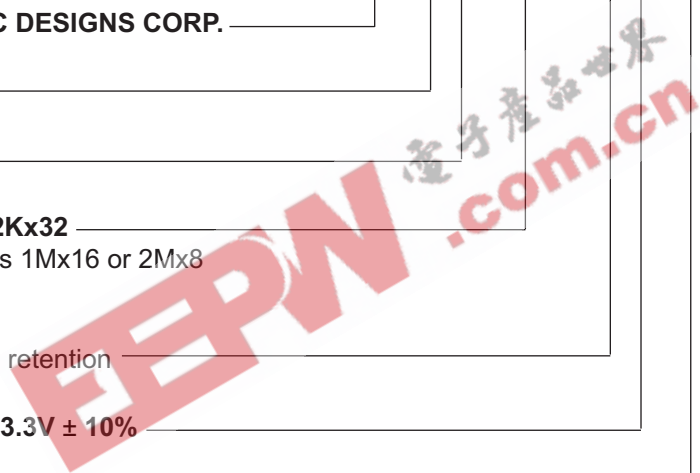
B = 143 PBGA, 16mm x 18mm, 288mm<sup>2</sup>

DEVICE GRADE:

M = MILITARY SCREENED -55°C TO +125°C

I = INDUSTRIAL -40°C TO 85°C

C = COMMERCIAL 0°C TO +70°C



**Document Title**

512K x 32 SRAM PBGA Multi-Chip Package

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 0	Initial Release	March 2002	Advanced
Rev 1	Changes (Pg. 1) 1.1 Switch Rows and Columns header position	March 2002	Advanced
Rev 2	Changes (Pg. 1) 2.1 Switch Rows and Columns header position (Pg. 1)	May 2002	Advanced
Rev 3	Changes (Pg. 1, 5) 3.1 Remove excess white space from package drawing for to create a consistent accurate style.	May 2002	Advanced
Rev 4	Changes (Pg. 1, 2, 7) 4.1 Add Thermal Resistance Table 4.2 Change product status to Final	January 2003	Final
Rev 5	Changes (Pg. 1, 2, 6, 7) 5.1 Add low power data retention option	June 2004	Final