



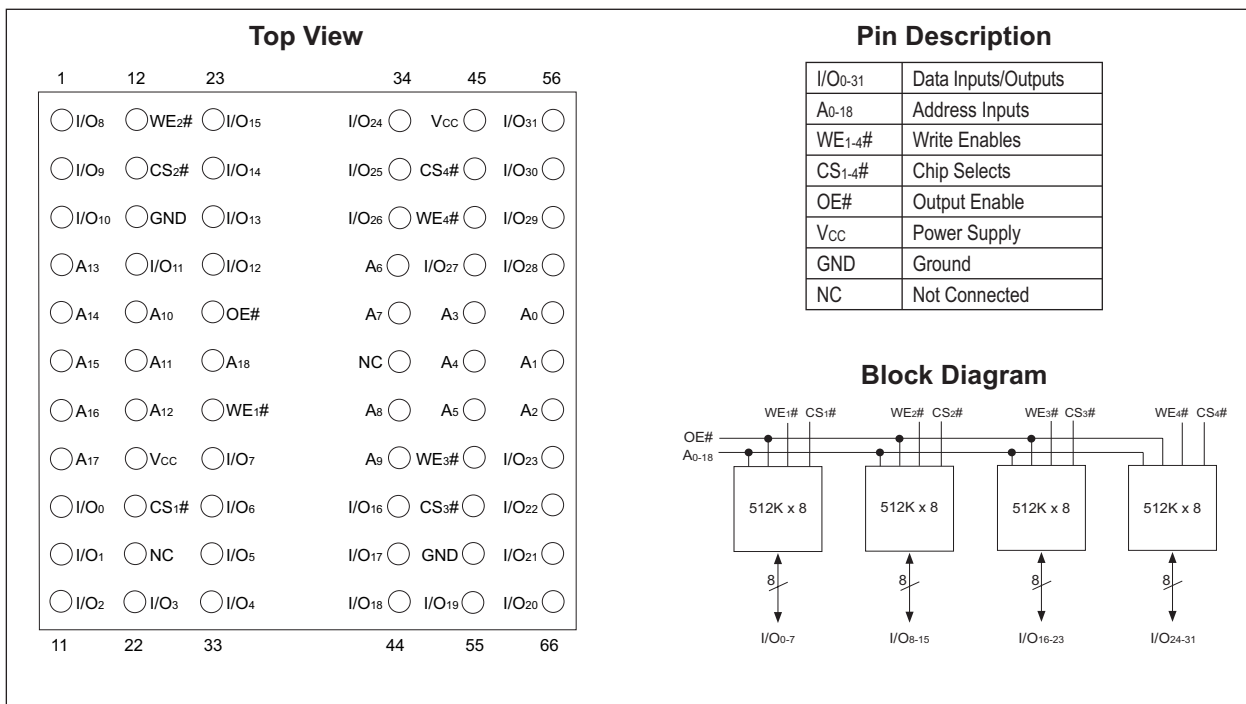
512Kx32 SRAM 3.3V MULTICHIP PACKAGE

FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
 - 68 lead, 22.4mm (0.880 inch) CQFP, (G2U), 3.56mm (0.140"), (Package 510)
- Organized as 512Kx32; User Configurable as 2x512Kx16 or 4x512Kx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
 - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
 - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32V-XG2UX - 8 grams typical
 - WS512K32NV-XH1X - 13 grams typical

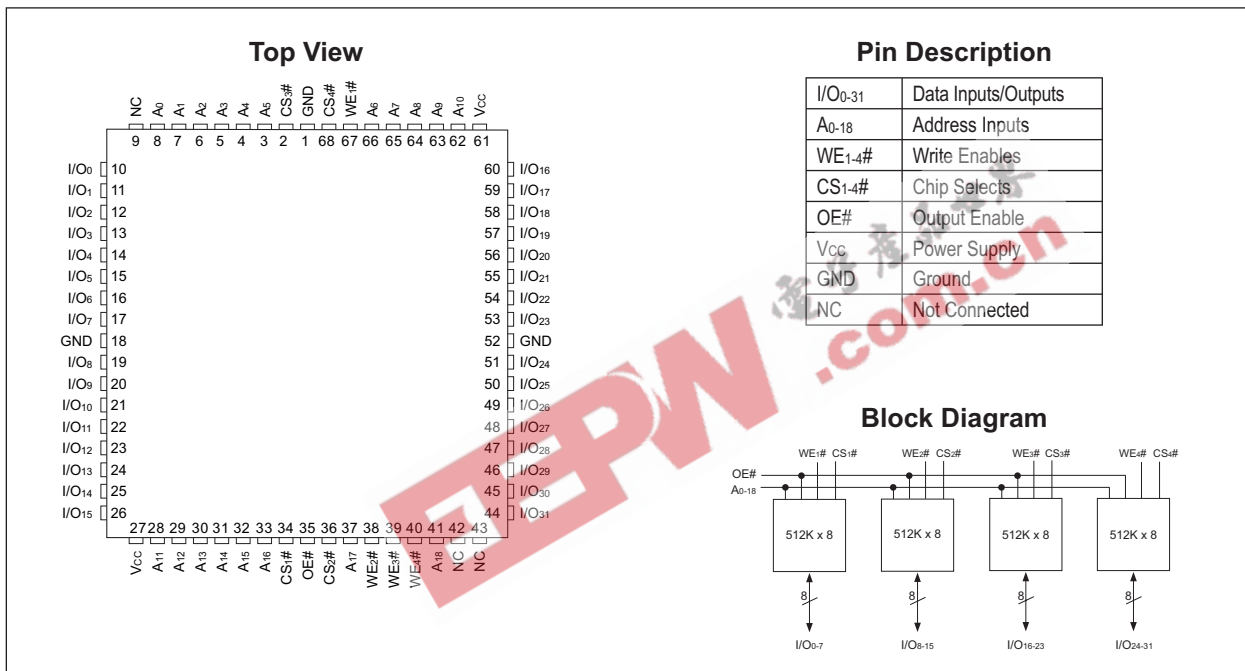
* This product is subject to change without notice.

PIN CONFIGURATION FOR WS512K32NV-XH1X





PIN CONFIGURATION FOR WS512K32V-XG2UX





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance HIP (PGA) CQFP G2U	C _{WE}	V _{IN} = 0V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C _{CS}	V _{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C _{I/O}	V _{I/O} = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC x 32}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		400	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		200	mA
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V.
Contact factory for low power option.



AC CHARACTERISTICS

$V_{CC} = 3.3V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		8		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}^1	1		1		1		ns
Output Enable to Output in Low Z	t_{OLZ}^1	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}^1		8		8		10	ns
Output Disable to Output in High Z	t_{OHZ}^1		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

$V_{CC} = 3.3V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		14		ns
Address Valid to End of Write	t_{AW}	12		12		14		ns
Data Valid to End of Write	t_{DW}	9		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}^1	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}^1		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

The diagram shows a Device Under Test (D.U.T.) connected to a bipolar supply $V_Z = 1.5V$. The supply is connected to the D.U.T. through a capacitor $C_{eff} = 50\text{ pf}$. Two current sources are connected to the D.U.T. outputs, labeled I_{OL} and I_{OH} .

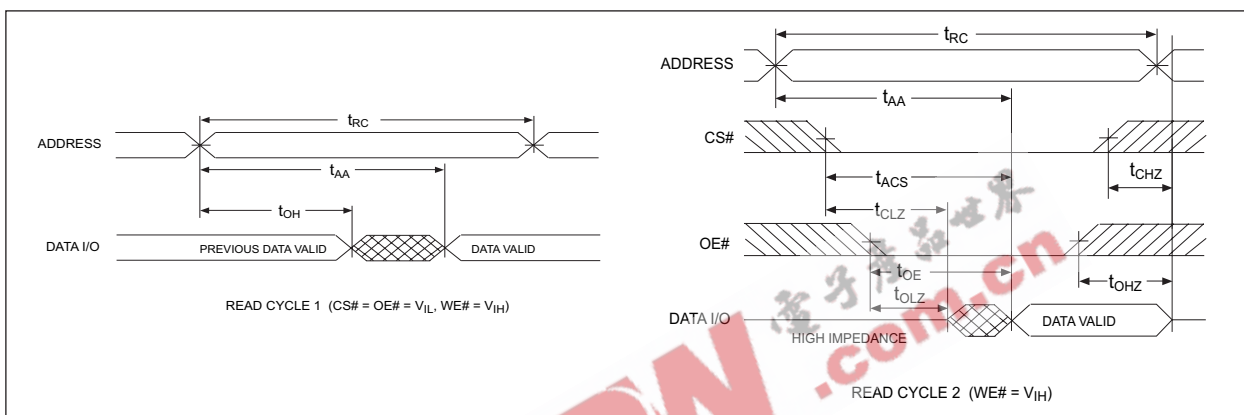
AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

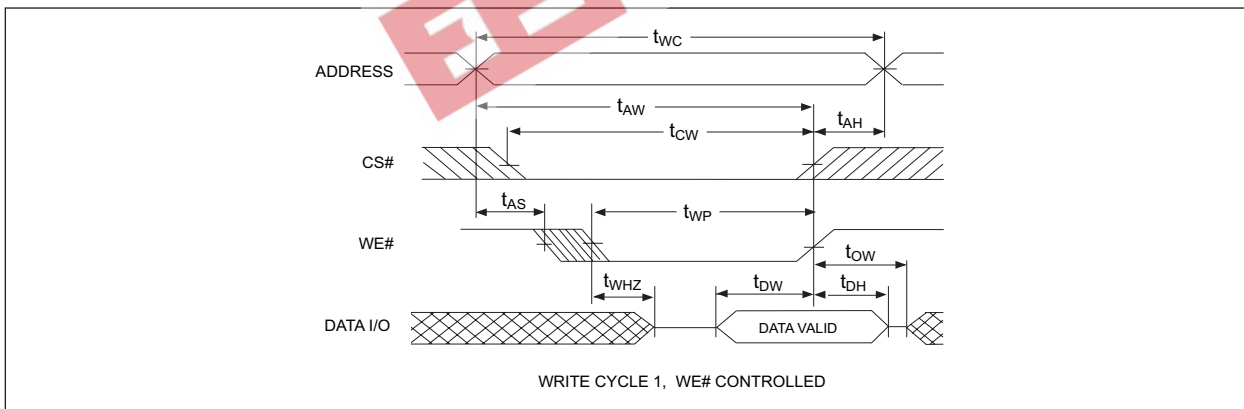
Notes:
 V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



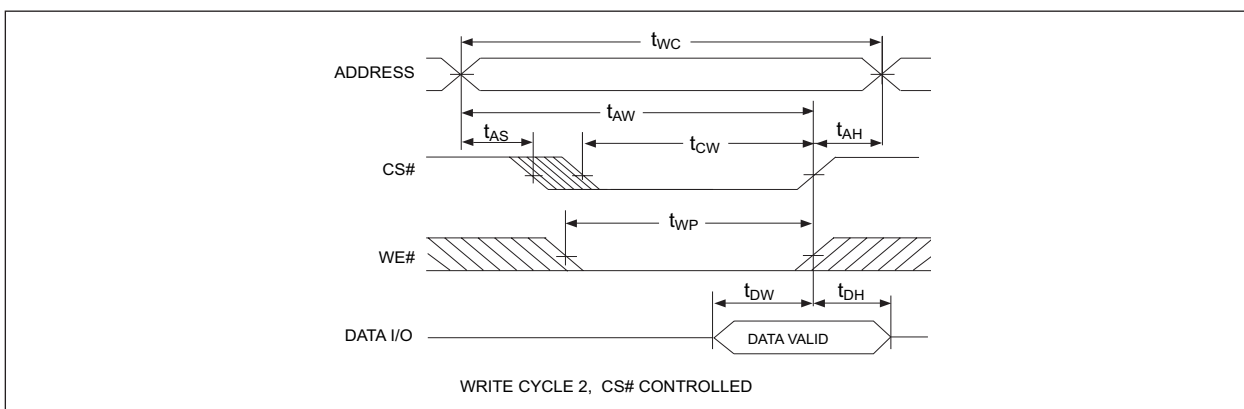
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED

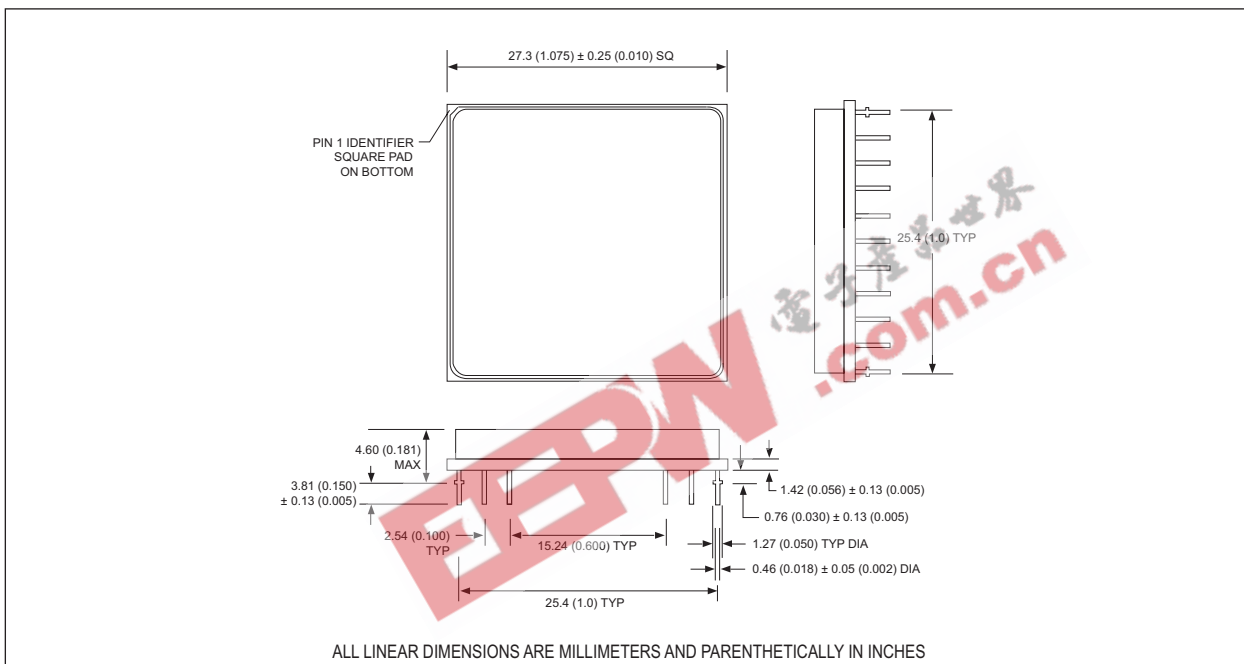


WRITE CYCLE - CS# CONTROLLED

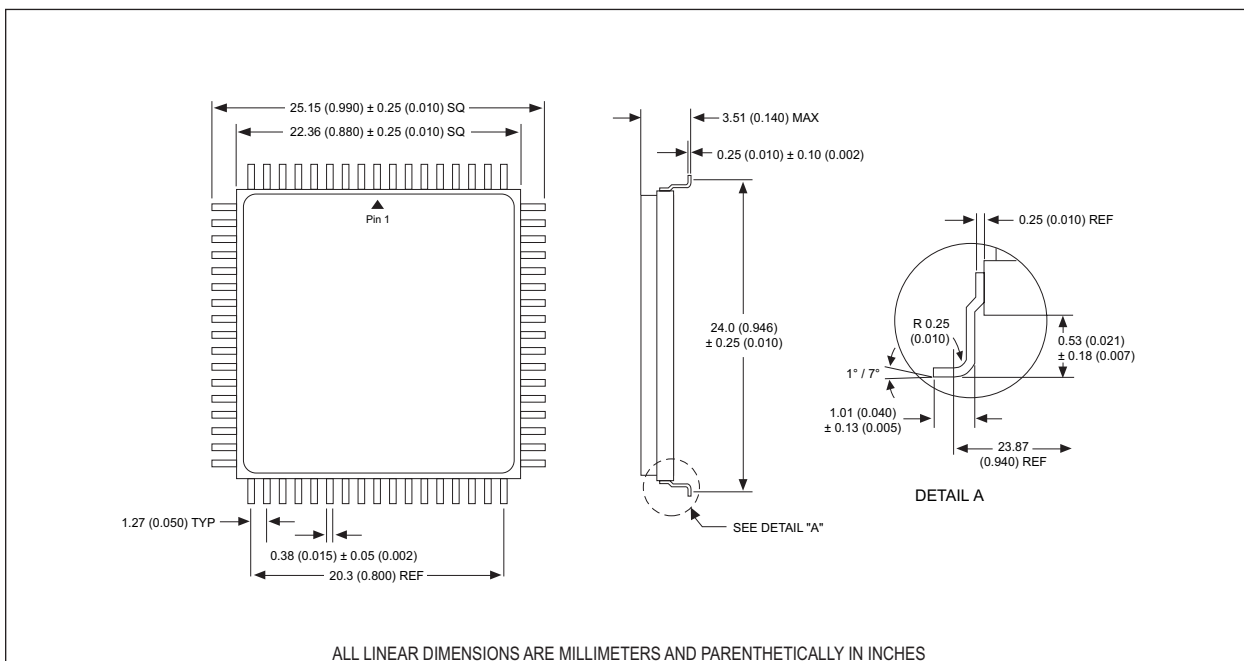




PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)





ORDERING INFORMATION

	W	S	512K32	X	V-XXX	X	X	X
WHITE ELECTRONIC DESIGNS CORP. _____								
SRAM _____								
ORGANIZATION, 512Kx32 _____ User configurable as 2x512Kx16 or 4x512Kx8								
IMPROVEMENT MARK: _____ N = No Connect at pin 21 and 39 in HIP for Upgrades (H1 only)								
Low Voltage Supply 3.3V ± 10% _____								
ACCESS TIME (ns) _____								
PACKAGE TYPE: _____ H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400) G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)								
DEVICE GRADE: _____ M = Military -55°C to +125°C I = Industrial -40°C to +85°C C = Commercial 0°C to +70°C								
LEAD FINISH: _____ Blank = Gold plated leads A = Solder dip leads								

