2Mx16 Flash MODULE, SMD 5962-97610

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
  - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207).
    Fits standard 56 SSOP footprint.
  - 44 pin Ceramic SOJ (Package 102)**
  - 44 lead Ceramic Flatpack (Package 208)**
- Sector Architecture
  - 32 equal size sectors of 64KBytes each
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx16; User Configurable as 2 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation.
- RESET# pin resets internal state machine to the read mode.
- Ready/Busy (RY#/BY#) output for detection of program or erase cycle completion.
- Multiple Ground Pins for Low Noise Operation

* This product is under development, is not qualified or characterized and is subject to change without notice.

** Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Notes.

FIGURE 1 – PIN CONFIGURATIONS

WF2M16-XDAX5
56 CSOP

TOP VIEW

CS1#	1	56	NC
A12	2	55	#RESET
A13	3	54	A11
A14	4	53	A10
A15	5	52	A9
NC	6	51	A1
CS2#	7	50	A2
NC	8	49	A3
A20	9	48	A4
A19	10	47	A5
A18	11	46	A6
A17	12	45	A7
A16	13	44	GND
Vcc	14	43	A8
GND	15	42	Vcc
I/O6	16	41	I/O9
I/O14	17	40	I/O1
I/O7	18	39	I/O8
I/O15	19	38	I/O0
RY/BY#	20	37	A0
OE#	21	36	NC
WE#	22	35	NC
NC	23	34	NC
I/O13	24	33	I/O2
I/O5	25	32	I/O10
I/O12	26	31	I/O3
I/O4	27	30	I/O11
Vcc	28	29	GND

WF2M16-XXX5
44 CSOJ (DL)**
44 FLATPACK (FL)**

TOP VIEW

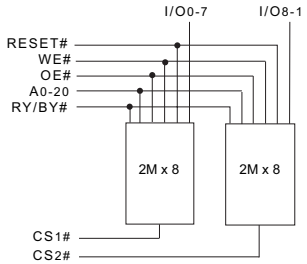
CS1#	1	56	NC
A12	2	55	#RESET
A13	3	54	A11
A14	4	53	A10
A15	5	52	A9
NC	6	51	A1
CS2#	7	50	A2
NC	8	49	A3
A20	9	48	A4
A19	10	47	A5
A18	11	46	A6
A17	12	45	A7
A16	13	44	GND
Vcc	14	43	A8
GND	15	42	Vcc
I/O6	16	41	I/O9
I/O14	17	40	I/O1
I/O7	18	39	I/O8
I/O15	19	38	I/O0
RY/BY#	20	37	A0
OE#	21	36	NC
WE#	22	35	NC
NC	23	34	NC
I/O13	24	33	I/O2
I/O5	25	32	I/O10
I/O12	26	31	I/O3
I/O4	27	30	I/O11
Vcc	28	29	GND

** Package to be developed.

PIN DESCRIPTION

I/O_{0-15}	Data Inputs/Outputs
A_{0-20}	Address Inputs
WE#	Write Enable
CS_{1-2}#	Chip Select
OE#	Output Enable
VCC	Power Supply
VSS	Ground
RY/BY#	Ready/Busy
RESET#	Reset

BLOCK DIAGRAM



NOTE:

1. RY/BY# is an open drain output and should be pulled up to Vcc with an external resistor.
2. Address compatible with Intel 2M8 56 SSOP.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	8	W
Storage Temperature	T_{STG}	-65 to +125	°C
Short Circuit Output Current	I_{OS}	100	mA
Data Retention (Mil Temp)		20	years
Endurance — write/erase cycles	(Mil Temp)	100,000 min.	cycles

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	25	pF
WE# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz	25	pF
CS# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	15	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	15	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	–	+0.8	V
Operating Temperature (Mil.)	T_A	-55	–	+125°C	°C
Operating Temperature (Ind.)	T_A	-40	–	+85	°C

DC CHARACTERISTICS - CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		80	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		120	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, CS# = V_{IH}, f = 5MHz, RESET# = V_{CC} ± 0.3V		4.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85xV_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:

1. The Icc current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC Characteristics – Write/Erase/Program Operations - WE# Controlled

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns
RESET# Pulse Width		t_{RP}	500		500		500		ns

NOTES:

1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Read Cycle Time	T_{AVAV}	T_{RC}	90		120		150		ns
Address Access Time	T_{AVQV}	T_{ACC}		90		120		150	ns
Chip Select Access Time	T_{ELQV}	T_{CE}		90		120		150	ns
Output Enable to Output Valid	T_{GLQV}	T_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	T_{EHQZ}	T_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	T_{GHQZ}	T_{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	T_{AXQX}	T_{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		T_{READY}		20		20		20	µs

1. Guaranteed by design, not tested.

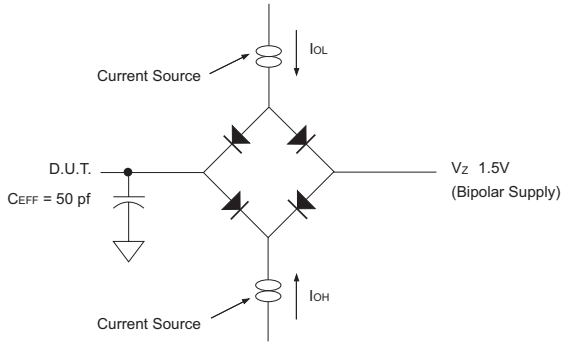
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 ý.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.ATE tester includes jig capacitance.

FIGURE 3 – RESET TIMING DIAGRAM

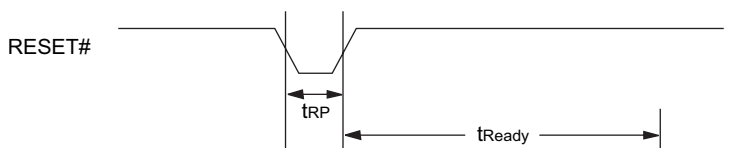


FIGURE 3 – AC WAVEFORMS FOR READ OPERATIONS

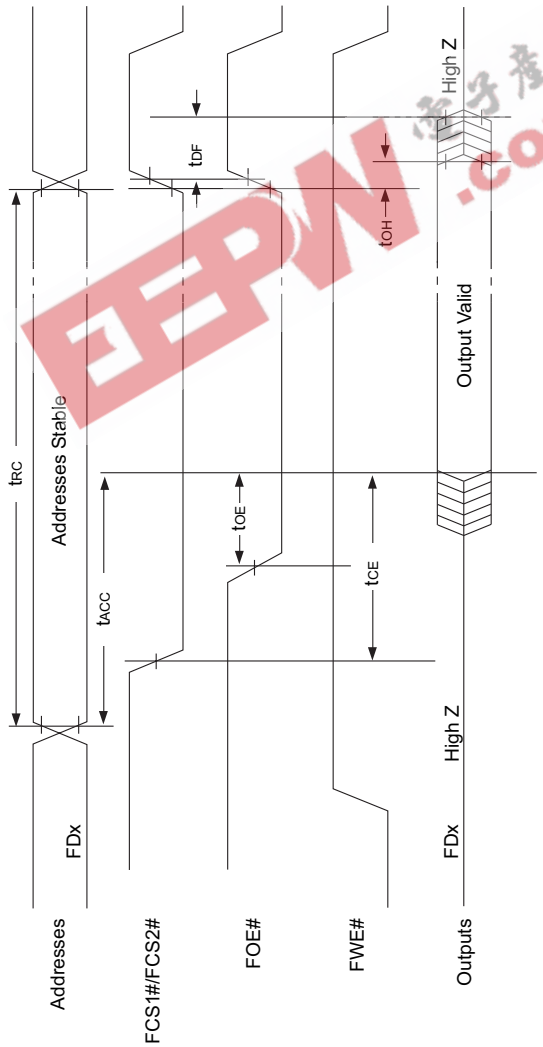
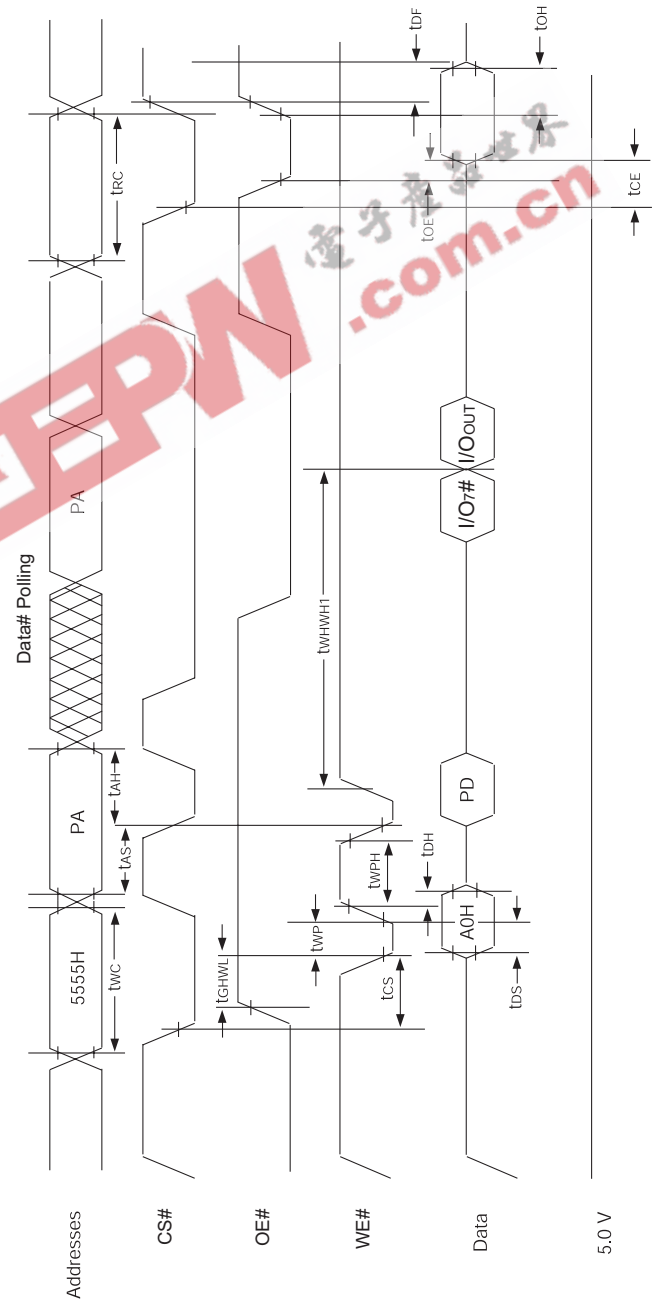


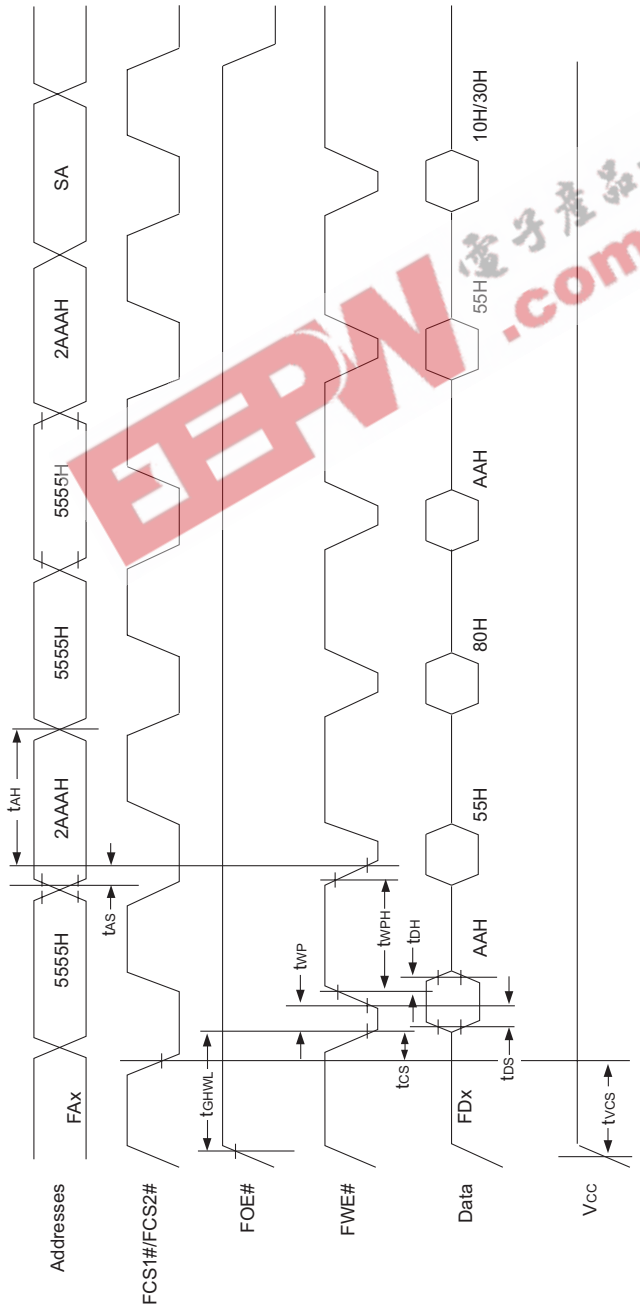
FIGURE 4 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 5 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:

1. SA is the sector address for Sector Erase.

FIG. 6 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

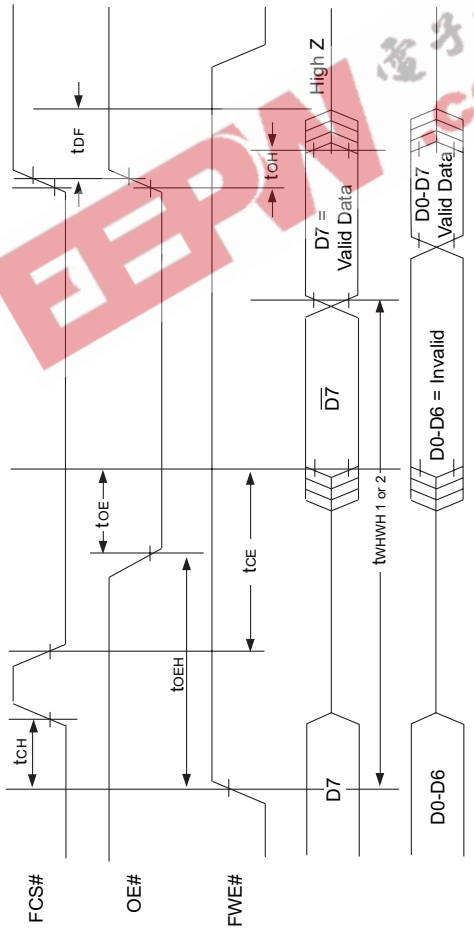
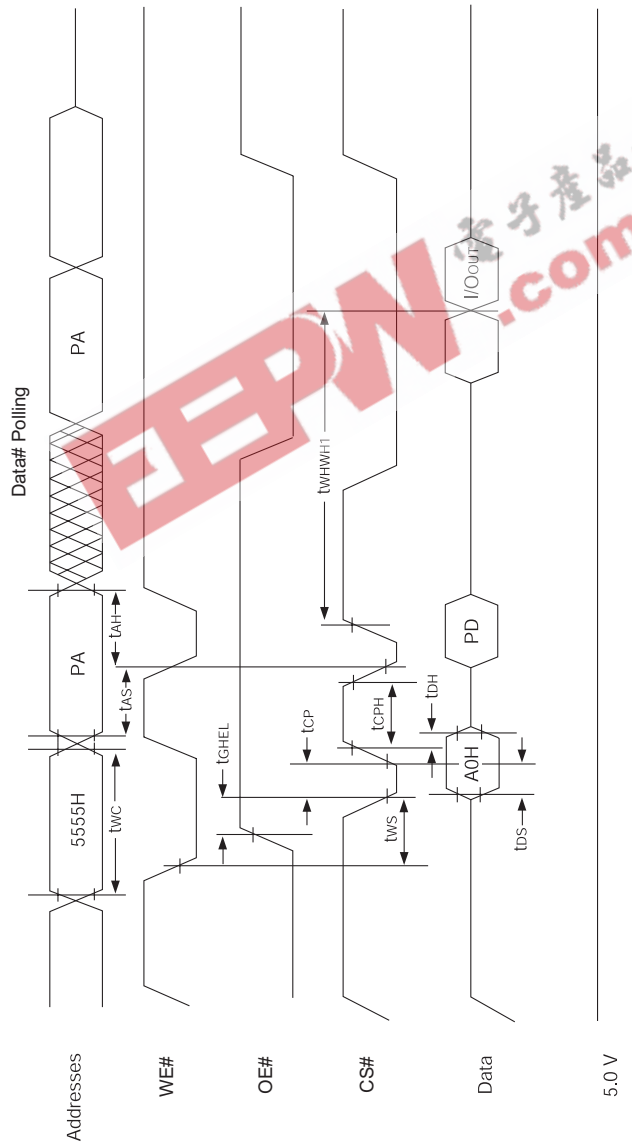


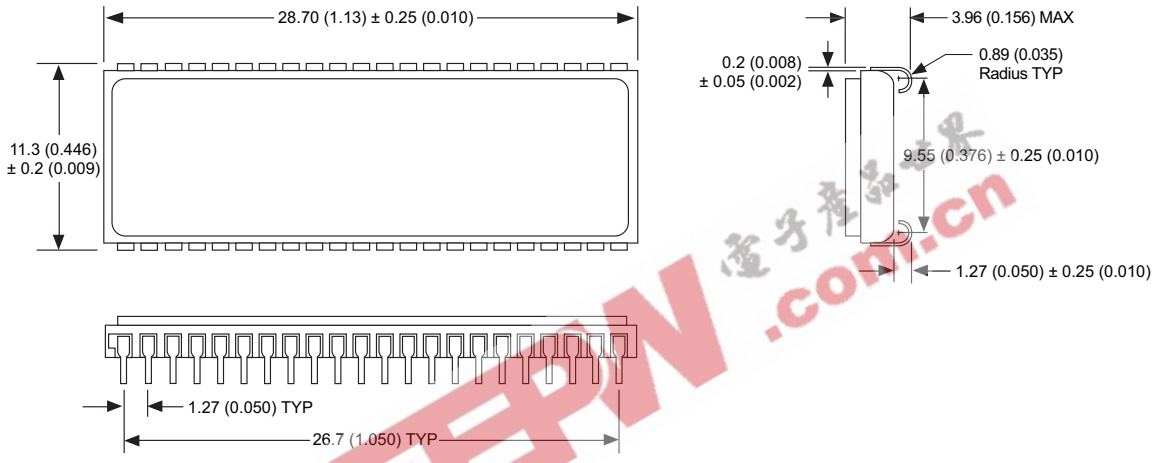
FIGURE 7 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

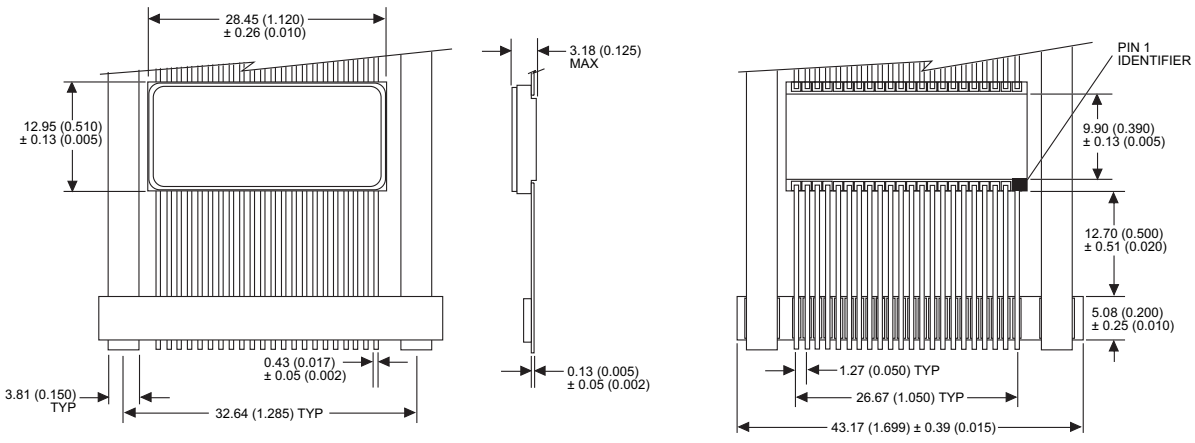
PACKAGE 102: 44 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

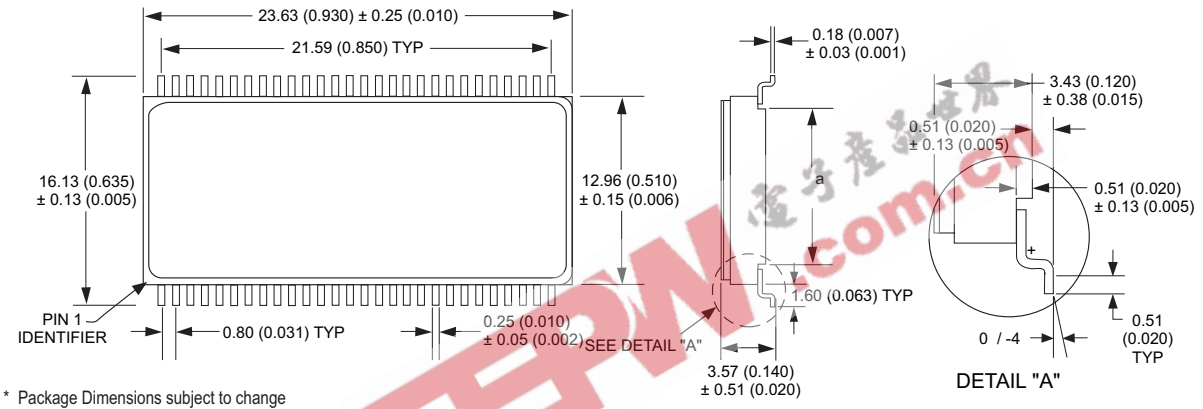
PACKAGE 208: 44 LEAD, CERAMIC FLAT PACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

PACKAGE 207: 56 LEAD, CERAMIC SOP*



* Package Dimensions subject to change

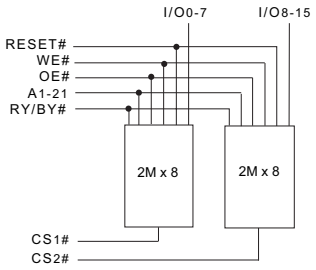
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIGURE 8 – ALTERNATE PIN CONFIGURATION FOR WF2M16W-XDAX5

56 CSOP
TOP VIEW

CS1#	1	56	NC
A12	2	55	RESET#
A13	3	54	A11
A14	4	53	A10
A15	5	52	A9
NC	6	51	A1
CS2#	7	50	A2
A21	8	49	A3
A20	9	48	A4
A19	10	47	A5
A18	11	46	A6
A17	12	45	A7
A16	13	44	GND
VCC	14	43	A8
GND	15	42	VCC
I/O6	16	41	I/O9
I/O14	17	40	I/O1
I/O7	18	39	I/O8
I/O15	19	38	I/O0
RY/BY#	20	37	NC
OE#	21	36	NC
WE#	22	35	NC
NC	23	34	NC
I/O13	24	33	I/O2
I/O5	25	32	I/O10
I/O12	26	31	I/O3
I/O4	27	30	I/O11
VCC	28	29	GND

BLOCK DIAGRAM



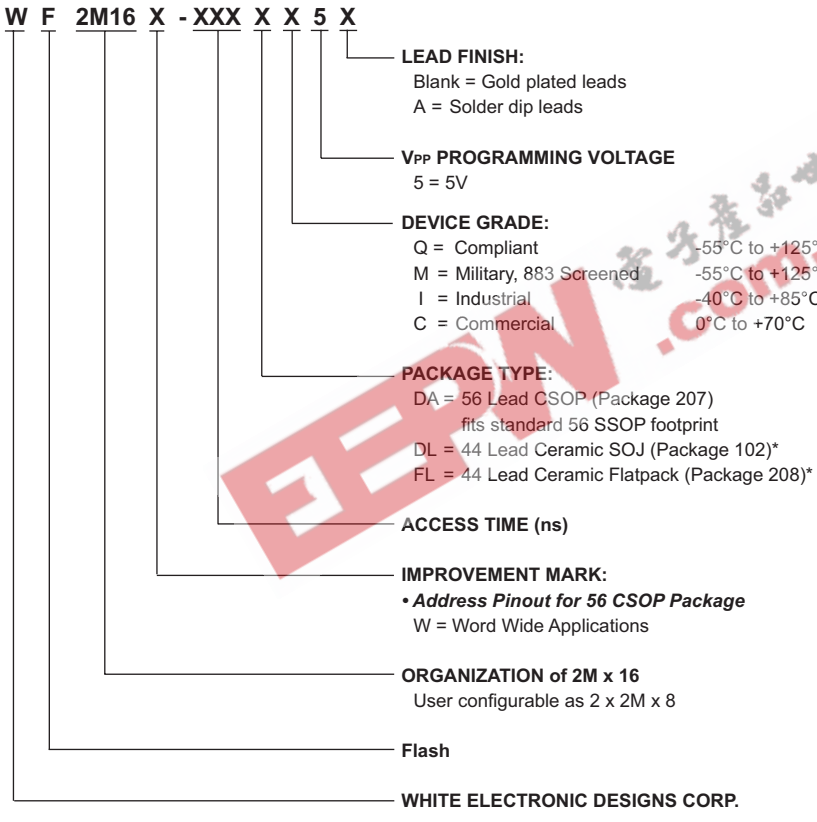
NOTE:

1. RY/BY# is an open drain output and should be pulled up toVcc with an external resistor.
2. Address compatible with Intel 1M16 56 SSOP.

PIN DESCRIPTION

I/O_{0-15}	Data Inputs/Outputs
A_{0-21}	Address Inputs
WE#	Write Enable
CS_{1-2}#	Chip Select
OE#	Output Enable
VCC	Power Supply
VSS	Ground
RY/BY#	Ready/Busy
RESET#	Reset

ORDERING INFORMATION



* Package to be developed.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 16 Flash MCP		150ns		5962-97610 04HXX
2M x 16 Flash MCP		120ns		5962-97610 05HXX
2M x 16 Flash MCP		90ns		5962-97610 06HXX