Winbond
Integrated Media Reader
W83L518D
Datasheet

W83L518D

Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		02/Jul.	1.0	1.0	1st Release
2					
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LIFE SUPPORT APPLICATIONS

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CONTENT

1 GENERAL DESCRIPTION

W83L518D is Winbond's innovative solution to a new class of storage devices for IA Noetebook, Desktop PC and PC system-related products. It incorporates a security Application: Smart Card Interface and two most promising compact storage interfaces: Memory Stick interface, and SD Memory Card/Multimedia Card interface in IT era.

To cater boundless IT implementation possibilities, W83L518D can be configured to interface with host through LPC bus. Base on the LPC interface, one Smart Card Interface port and two flash memory interfaces - Memory Stick and SD Memory ports are provided. The kind of versatility allows user to design very cost-effective products in a very flexible way.

The whole chip of W83L518D operates at voltage level of 3.3 V except Smart Card Interface port's I/O pins that are at 5 V to be compatible with mainstream Smart Card implementations. Advanced power management feature further optimizes power consumption whether in operation or in power down mode.

W83L518D comes as a 48-pin LQFP streamline package. Combining with powerful functions, effective power management, and versatile configurability, this integrated media reader offers a perfect approach for design of storage device of IT products.

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2 FUNCTIONS

2.1 General

- LPC bus is compliant with LPC Spec. 1.01
- LPC bus supports LDRQ# (LPC DMA), SERIRQ (serial IRQ)
- Programmable configuration settings
- 48 MHz crystal inputs
- PCICLK of 33 MHz is needed for LPC bus configuration

2.2 Smart Card Interface

- ISO-7816 compliant
- PC/SC T=0, T=1 compliant
- 16-byte transmitter FIFO and 16-byte receiver FIFO
- FIFO threshold interrupt to optimize system performance
- Programmable transmission clock frequency
- Versatile baud rate configuration
- UART-like register file structure
- General-purpose C4, C8 channels

2.3 Memory Stick Interface

- Memory Stick Standard Format Specifications ver. 1.3 compliant
- Support interrupt polling transmission
- Support FIFO threshold interrupt to optimize system performance
- Automatic clock halt to prevent underrun/overrun
- 16 MHz interface clock

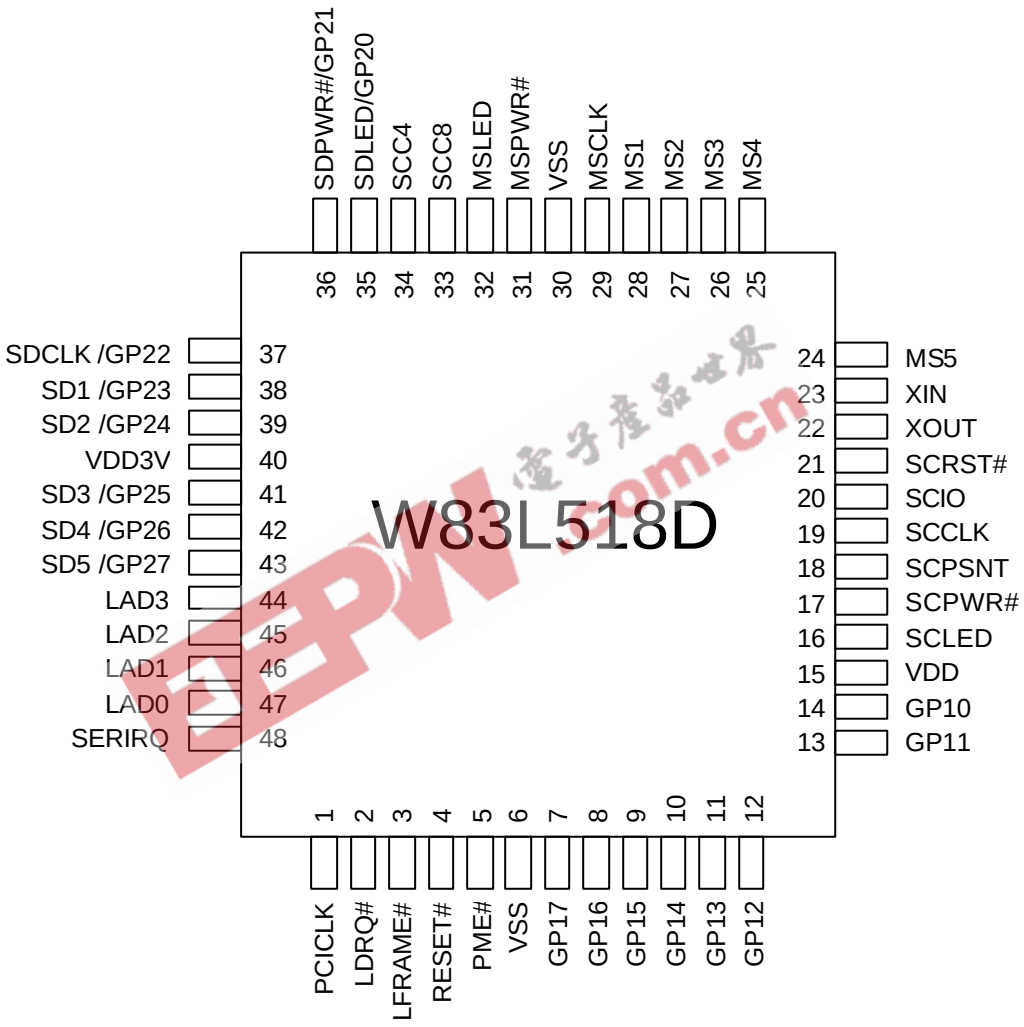
2.4 SD Memory Card Interface

- SD Memory Card Specifications: Part 1 PHYSICAL LAYER SPECIFICATION Version 1.0 Compliant
- Support interrupt polling transmission
- Support FIFO threshold interrupt to leverage system performance
- 24 MHz interface clock

2.5 Package

- 48-pin LQFP

3 PIN CONFIGURATION FOR W83L518D



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4 PIN DESCRIPTION

Note:

IN_t - 5V TTL level input pin

IN_{tp3} - 3.3V TTL level input pin

IN_{ts} - 5V TTL level Schmitt-trigger input pin

IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin

I/O_{12t} - 5V TTL level bi-directional pin with 12 mA drive-sink capability

I/O_{24t} - 5V TTL level bi-directional pin with 24 mA drive-sink capability

I/O_{16tp3} - 3.3V TTL level bi-directional pin with 16 mA drive-sink capability

O_2 - 5V output pin with 2 mA drive-sink capability

O_{12} - 5V output pin with 12 mA drive-sink capability

O_{16p3} - 3.3V output pin with 16 mA drive-sink capability

OD_{12p3} - 3.3V Open-drain output pin with 12 mA sink capability.

4.1 Bus Interface

SYMBOL	PIN	I/O	FUNCTION
PME#	5	OD_{12p3}	Active-low PME event.
RESET#	4	IN_{tsp3}	Active-low system reset signal.
LFRAME#	3	IN_{tsp3}	Active-low signal indicates start of a new LPC frame or termination of a premature frame.
LDRQ#	2	O_{16p3}	Encoded DMA Request signal.
PCICLK	1	In_{tsp3}	PCI clock input of 33 MHz.
SERIRQ	48	I/O_{16tp3}	Serial IRQ input/output.
LAD0	47	I/O_{16tp3}	This signal combining with other LADx signals communicate address, control, and data information over the LPC bus between a host and a peripheral.
LAD1	46	I/O_{16tp3}	This signal combining with other LADx signals communicate address, control, and data information over the LPC bus between a host and a peripheral.
LAD2	45	I/O_{16tp3}	This signal combining with other LADx signals communicate address, control, and data information over the LPC bus between a host and a peripheral.
LAD3	44	I/O_{16tp3}	This signal combining with other LADx signals communicate address, control, and data information over the LPC bus between a host and peripherals.

4.2 Smart Card Interface Pins

SYMBOL	PIN	I/O	FUNCTION
SCC4	34	I/O_{16tp3}	Smart Card interface general purpose I/O channel for connector pin C4 on a card.
SCC8	33	I/O_{16tp3}	Smart Card interface general purpose I/O channel for connector pin C8 on a card.
SCLED	16	O_{24}	This pin outputs an oscillating clock signal of various frequencies depending on traffic of primary Smart Card interface.
SCPWR#	17	O_{24}	Smart Card interface power control signal.
SCPSNT	18	IN_{ts}	Smart Card interface card present detection Schmitt-trigger input.
SCCLK	19	O_2	Smart Card interface clock output.
SCIO	20	I/O_{12t}	Smart Card interface data I/O channel.
SCRST#	21	O_{12}	Smart Card interface reset output.

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4.3 Memory Stick Interface/SD Memory Interface Pins

SYMBOL	PIN	I/O	FUNCTION
MSLED	32	O_{16p3}	Memory Stick function - This pin outputs an oscillating clock signal of various frequencies depending on traffic of the Memory Stick interface.
MSPWR#	31	O_{16p3}	Memory Stick function - This pin is power control signal for the Memory Stick interface.
MSCLK	29	O_{16p3}	Memory Stick function - This pin is SCLK for the Memory Stick interface.
MS1	28	O_{16p3}	Memory Stick interface pin.
MS2	27	I/O_{16tp3}	Memory Stick interface pin.
MS3	26	---	Memory Stick interface pin.
MS4	25	IN_{tsp3}	Memory Stick interface pin.
MS5	24	---	Memory Stick interface pin.
SD5	43	I/O_{16tp3}	SD interface pin.
SD interface pin.	42	I/O_{16tp3}	SD interface pin.
SD interface pin.	41	I/O_{16tp3}	SD interface pin.
SD interface pin.	39	I/O_{16tp3}	SD interface pin.
SD interface pin.	38	I/O_{16tp3}	SD interface pin.
SDCLK	37	O_{16p3}	SD function - This pin is CLK for the SD memory card interface.
SDPWR#	36	O_{16p3}	SD function - This pin is power control signal for the SD memory card interface.
SDLED	35	O_{16p3}	SD function - This pin outputs an oscillating clock signal of various frequencies depending on traffic of the SD memory card interface.
CARD_DETECT	13	IN_t	Function as an alternative card detection input for the SD memory interface.

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4.4 General-Purpose I/O Pins

SYMBOL	PIN	I/O	FUNCTION
GP17	7	I/O_{12t}	General-purpose I/O port 17.
GP16	8	I/O_{12t}	General-purpose I/O port 16.
GP15	9	I/O_{12t}	General-purpose I/O port 15.
GP14	10	I/O_{12t}	General-purpose I/O port 14.
GP13 GP12	11 12	I/O_{12t} I/O_{12t}	General-purpose I/O port 13. General-purpose I/O port 12.
GP11 EX_CD	13	I/O_{12t}	General-purpose I/O port 11. External card detedtion pin. The detectable level can be set on bit 2 of CR F0 on Logical device 3.
GP10 PHEFRAS	14	I/O_{12t} In_t	General-purpose I/O port 10. This pin also functions as a power-on setting pin whose value is latched on the rising edge of RESET# (pin 4) to select configuration ports as 2Eh/2Fh (PHEFRAS = 1) or 4Eh/4Fh (PHEFRAS = 0). It determines the default value of CR26 bit 6 (HEFRAS).

4.5 Crystal and Power Pins

SYMBOL	PIN	FUNCTION
XOUT, XIN	22, 23	Connected to a 48 MHz crystal and function as the working clock for all the media reader interfaces.
VDD3V	40	+3.3V power supply for host interface, Memory Stick/SD Memory interfaces, and internal core.
VDD	15	+5V power supply for Smart Card interface I/O pins.
VSS	6, 30	Ground.

5 GENERAL-PURPOSE I/O PORTS (GPIO)

W83L518D supports one group of dedicated general-purpose I/O ports and a multi-functional GPIO group, which share the same pines with the SD interface sockets. There are cases when only one socket is needed in a system and pins for the other unused socket are wasted. To provide the most cost-effective solution, W83L518D could be configured to transform these pins into general-purpose I/O ports.

The first group (GP10 ~ 17) is configured through the configuration registers CRF0 ~ CRF2 in logical device 2 and the other group (GP20 ~27) through CRF3 ~ F5. Users can configure each individual port to be an input or output port by programming respective bit in direction register (CRF0/CRF3: 0= output, 1 = input). Invert port value by setting inversion register (CRF2/CRF5: 0 = non-inverse, 1 = inverse). Port value is read/written through data register (CRF1/CRF4). Table 5.1 and 5.2 illustrate GPIO's assignment. To further facilitate system design, W83L518D allows direct accesses to data register and direction register through I/O ports, whose base address is programmable at CR 60, 61 in logical device 2. Detailed configuration is described in logical device 2 of section 6 CONFIGURATION REGISTER.

GP10 (pin 14) also functions as a power-on setting pin whose value is latched on the rising edge of RESET# (pin 4) to select configuation port addresses. Therefore, GP10 is a push-pull I/O port unlike the other GPIO ports, which are open-drained I/Os to support this power-on setting feature.

GP11 (pin 13) could function as a card detection input if selected by SDI to support some MMC cards, which don't offer card detection feature through DATA3 pin.

Table 5.1

DIRECTION BIT 0 = OUTPUT 1 = INPUT	INVERSION BIT 0 = NON INVERSE 1 = INVERSE	I/O OPERATION
0	0	Basic non-inverting output
0	1	Basic inverting output
1	0	Basic non-inverting input
1	1	Basic inverting input

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Table 5.2

GPIO PORT DATA REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
	BIT 6	GP16
	BIT 7	GP17
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25
	BIT 6	GP26
	BIT 7	GP27

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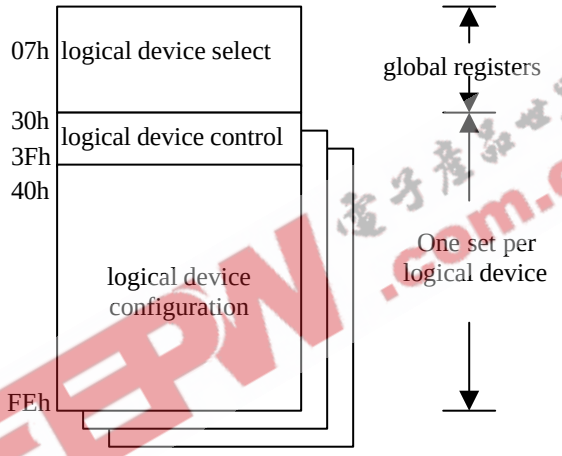
6 CONFIGURATION REGISTER

6.1 Plug and Play Configuration

W83L518D/W83L519D implement compatible PNP protocol to access configuration registers for setting up different types of configurations. There are four Logical Devices (Logical Device 0 to Logical Device 3) in W83L518D/W83L519D which correspond to four major functions: Smart Card Interface (logical device 0), Memory Stick Interface (logical device 1), GPIO (logical device 2) and SD Memory Interface (logical device 3). Each Logical Device has its own configuration registers (CR30 and above). Host can access those registers by writing an appropriate logical device number into logical device select register at CR07 first.



6.2 Compatible PnP

6.2.1 Extended Function Register

W83L518D/W83L519D provide two methods to enter Extended Function mode (compatible PnP) and access configuration registers dependent on value of HEFRAS (bit 6 of CR26. The corresponding power-on setting pin is pin 14) as follows:

HEFRAS	address and value
0	write 83h to I/O address 2Eh twice
1	write 83h to I/O address 4Eh twice

In Compatible PnP, a specific value (83h) must be written twice to the Extended Function Enable Register (EFER at I/O address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Function Index Register (EFIR, I/O address at 2Eh or 4Eh which is the same as EFER) to

identify which configuration register is to be accessed. User can then access the addressed configuration register through the Extended Function Data Register (EFDR, I/O address at 2Fh or 4Fh).

After programming of the configuration register is completed, another specific value (0AAh) should be written to EFER to leave Extended Function mode to prevent inadvertent accesses to those configuration registers. User may write a "1" to bit 5 of CR26 (LOCKREG) to prevent configuration registers from accidental accesses.

6.2.2 Extended Functions Enable Register (EFER)

After a power-on reset, W83L518D/W83L519D enters the default operation mode. A specific value must be programmed into the Extended Function Enable Register (EFER) so that configuration registers can be accessed. On a PC/AT system, its I/O address is 2Eh or 4Eh (as described in previous section).

6.2.3 Extended Function Index Register (EFIR), Extended Function Data Register (EFDR)

After entering Extended Function mode, Extended Function Index Register (EFIR) must be written with an index value (02h, 07h-FEh) to specify which configuration register is to be accessed through Extended Function Data Register (EFDR). EFIR is a write-only register at I/O address 2Eh or 4Eh (as described in section 9.2.1) on a PC/AT system and EFDR is a read/write register at I/O address 2Fh or 4Fh.

6.3 Configuration Sequence

To program configuration registers, specific configuration sequence must be followed:

(1) Write 83h to EFER twice to enter Extended Function mode.

(2) Select logical device select register by writing 07h to EFIR.

(3) Select logical device by writing a value to EFDR.

(4) Select control/configuration register by writing its index to EFIR.

(5) Access selected control/configuration register through EFDR.

(6) Repeat step 4 ~ 5 as needed.

(7) Leave Extended Function mode by writing AAh to EFER.

Step 2 and step 3 are not necessary for accessing global register (index 00h to 2Fh).

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6.3.1 Software programming example

The following example is written in Intel 8086 assembly language. EFER and EFIR are assumed to be at 2Eh, and EFDR is at 2Fh. Use 4Eh/4Fh instead of 2Eh/2Fh if HEFRAS (bit 6 of CR26) is set.

```
;--------------------------------------------------------------------------
; Enter Extended Function mode, interruptible double-write    |
;--------------------------------------------------------------------------
MOV         DX, 2Eh
MOV         AL, 83h
OUT DX, AL
OUT DX, AL
;--------------------------------------------------------------------------
; Configure logical device 1, configuration register CRF0   |
;--------------------------------------------------------------------------
MOV         DX, 2Eh
MOV         AL, 07h
OUT DX, AL          ; point to Logical Device Number Reg.
MOV         DX, 2Fh
MOV         AL, 01h
OUT DX, AL          ; select logical device 1
;
MOV DX, 2Eh
MOV         AL, F0H
OUT DX, AL          ; select CRF0
MOV         DX, 2Fh
MOV         AL, 3Ch
OUT DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------
; Exit extended function mode    |
;-----------------------------------------
MOV         DX, 2Eh
MOV         AL, AAh
OUT DX, AL
```

6.4 Global Registers

CR02 (Default 00h, write only)

Bit [7:1]: Reserved.

Bit 0: SWRST

= 0 Normal operation.

= 1 Software reset.

CR07 (Default 00h)

Bit [7:0]: Logical Device Number.

CR20 (read only)

Bit [7:0]: Device ID number (higher byte).

= 71h

CR21 (read only)

Bit [7:0]: Device ID number (lower byte)

= 1Xh (for W83L518D)

= 2Xh (for W83L519D)

X: Revision number

CR22 (Default 80h)

Bit 7: SCPWD

= 0 Power down Smart Card interface.

= 1 No Power down.

Bit 6: MSPWD

= 0 Power down Memory Stick interface.

= 1 No Power down.

Bit 5: SDPWD

= 0 Power down SD memory card interface.

= 1 No Power down.

Bit [4:0]: Reserved.

CR23 (Default 00h)

Bit 7: PME_EN. Power management event enable bit.

= 0 PME_L function is disabled.

= 1 Enable to issue a low pulse on PME_L when a power management event occurs.

Bit 6: MSPME_EN. Memory Stick interface power management event enable bit.

= 0 Memory Stick interface power management event is disabled.

= 1 Enable Memory Stick interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit 5: SDPME_EN. SD memory card interface power management event enable bit.

= 0 SD memory card interface power management event is disabled.

= 1 Enable SD memory card interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit 4: SCPME_EN. Smart Card interface power management event enable bit.

= 0 Smart Card interface power management event is disabled.

= 1 Enable Smart Card interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit [3:0]: Reserved.

CR24 (Default 00h)

Bit 7: Reserved.

Bit 6: MSPME_STS. Memory Stick interface power management event status bit.

= 0 No Memory Stick interface power management event occurs.

= 1 Memory Stick interface power management event occurs.

Bit 5: SDPME_STS. SD memory card interface power management event status bit.

= 0 No SD memory card interface power management event occurs.

= 1 SD memory card interface power management event occurs.

Bit 4: SCPME_STS. Smart Card interface power management event status bit.

= 0 No Smart Card interface power management event occurs.

= 1 No Smart Card interface power management event occurs.

Bit [3:0]: Reserved.

CR26 (Default 40h)

Bit 7: Reserved

Bit 6: HEFRAS, Extended Function Register Address Select. The corresponding power-on setting pin is GP10 (PHEFRAS, pin 14). The HEFRAS is defaulted to "1" if PHEFRAS is "0" and is defaulted to "0" if PHEFRAS is "1".

= 0 Extended Function Registers are at 2Eh/2Fh.

= 1 Extended Function Registers are at 4Eh/4Fh.

Bit 5: LOCKREG

= 0 Enable accesses of Configuration Registers.

= 1 Disable accesses of Configuration Registers.

Bit [4:0]: Reserved

CR29 (Default 00h, only valid in W83L518D)

Bit 7: Multi-function selection bit for pin 7 ~ 14

= 0 Pin 7 ~ 14 function as Smart Card interface socket B.

= 1 Pin 7 ~ 14 function as GPIO1.

Bit 6: Multi-function selection bit for pin 35 ~ 43

= 0 Pin 35 ~ 43 function as MSI/SDI socket B.

= 1 Pin 35 ~ 43 function as GPIO2.

Bit 5: Multi-function selection bit for pin 32 ~ 31 & pin 29 ~ 24.

= 0 Pin 32 ~ 31 and pin 29 ~ 24 function as MSA (MS interface card A).

= 1 Pin 32 ~ 31 and pin 29 ~ 24 function as SDA (SD interface card A).

Bit 4: Multi-function selection bit for pin 43 ~ 41 & pin 39 ~ 35.

= 0 Pin 43 ~ 41 & pin 39 ~ 35 function as MSB (MS interface card B).

= 1 Pin 43 ~ 41 & pin 39 ~ 35 function as SDB (MS interface card B).

Bit [3:0]: Reserved.

6.5 Logical Device 0 (Smart Card Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0 Logical device is inactive.

= 1 Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Smart Card interface.

CRF0 (Default 0x00)

Bit 7: IRQ sharing control bit.

= 0 No IRQ sharing.

= 1 IRQ sharing.

Bit 0: SCPSNT_POL (Smart Card PreSeNT POLarity). SCPSNT polarity bit.

= 0 SCPSNT is active high.

= 1 SCPSNT is active low.

6.6 Logical Device 1 (Memory Stick Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0: Logical device is inactive.

= 1: Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select MSI base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for MSI.

CR74 (Default 0x04)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select DRQ resource for MSI.

CRF0 (Default 0x00)

Bit [7:5]: Reserved.

Bit 4: IRQ polarity control bit by level mode.
= 0: IRQ is active high.
= 1: IRQ is active low.

Bit 3: IRQ polarity control bit by pulse mode.
= 0: IRQ is active low.
= 1: IRQ is active high.

Bit 2: IRQ sharing control bit.
= 0: No IRQ sharing.
= 1: IRQ sharing.

Bit 1: MS4 output polarity control bit.
0: MS4 output low.
1: MS4 output high.

Bit 0: MS4 output enable bit.
0: MS4 output disable.
1: MS4 output enable.

6.7 Logical Device 2 (GPIO)

CR30 (Default 00h)

Bit [7:3]: Reserved.

Bit 2: Individual disable/enable bit for GPIO2.

= 0 GPIO2 is disabled if bit 0 is also "0".

= 1 GPIO2 is enabled.

Bit 1: Individual disable/enable bit for GPIO1.

= 0 GPIO1 is disabled if bit 0 is also "0".

= 1 GPIO1 is enabled.

Bit 0: Logical device disable/enable bit.

= 0 GPIO1 and GPIO2 are disabled/enabled dependent on bit 1 and 2 respectively.

= 1 Activates GPIO1 and GPIO2.

CR60, CR61 (Both default 00h)

Base address configuration registers: programmable at addresses from 0100h to 0FF8h on 4-byte boundary. Base address + 0 and base address + 1 are for GPIO1 as direction register and data register respectively while base address + 2 and base address + 3 are for GPIO2 as direction register and data register respectively.

CRF0 (GP10 ~ GP17 direction register. Default FFh)

When set to "1", respective GPIO port is programmed as an input port. When set to a "0", respective GPIO port is programmed as an output port.

CRF1 (GP10 ~ GP17 data register. Default 00h)

If a port is programmed to be an output port, its respective bit can be read/written and output to respective pin. If a port is programmed to be an input port, its respective bit reflects what is on respective pin.

CRF2 (GP10 ~ GP17 inversion register. Default 00h)

When set to "1", respective incoming/outgoing port value is inverted. When set to "0", respective incoming/outgoing port value is the same as in data register.

CRF3 (GP20 ~ GP27 direction register. Default FFh)

When set to "1", respective GPIO port is programmed as an input port. When set to a "0", respective GPIO port is programmed as an output port.

CRF4 (GP20 ~ GP27 data register. Default 00h)

If a port is programmed to be an output port, its respective bit can be read/written and output to respective pin. If a port is programmed to be an input port, its respective bit reflects what is on respective pin.

CRF5 (GP20 ~ GP27 inversion register. Default 00h)

When set to "1", respective incoming/outgoing port value is inverted. When set to "0", respective incoming/outgoing port value is the same as in data register.

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6.8 Logical Device 3 (SD Memory Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0 Logical device is inactive.

= 1 Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select SD Card interface base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for SD interface.

CR74 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select DRQ resource for SD interface.

CRF0 (Default 0x01)

Bit [7:6]: Reserved.

Bit 5: Set the output value of the DATA3 pin when bit4 is setted 1.

= 0 The DATA3 pin will output low.

= 1 The DATA3 pin will output high.

Bit 4: Set the DATA3 (MS1 or MSB1) pin to output pin.

= 0 Set the DATA3 pin to bi-direction pin.

= 1 Set the DATA3 pin to output pin.

Bit 3: Reserved.

Bit 2: Select the pole of the GP11 card-detect pin.

= 0 When detecting the low signal indicate the card is inserted and high signal indicate the card is extracted.

= 1 When detecting the high signal incicate the card is inserted and low signal indicate the card is extracted.

Bit 1: Select GP11 pin to detect card.

= 0 Don' t use the GP11 pin to detect card.

= 1 Use the GP11 (SCBPWR_L) pin to detect card.

Bit 0: Select DATA3 pin to detect card.

= 0 Don' t use the DATA3 (MS1 or MSB1) to detect card.

= 1 Use the DATA3 (MS1 or MSB1) pin to detect card.

CRF1 (Default 0x01)

Bit [7:4]: Reserved.

Bit 3: Set the IRQ pole for level mode.

= 0 The IRQ is active high.

= 1 The IRQ is active low.

Bit 2: Set the IRQ pole for pulse mode.

= 0 The IRQ is active low.

= 1 The IRQ is active high.

Bit 1: Set the IRQ to level mode or pulse mode.

= 0 The IRQ is level mode.

= 1 The IRQ is pulse mode.

Bit 0: Use debounce function for card-detect circuit.

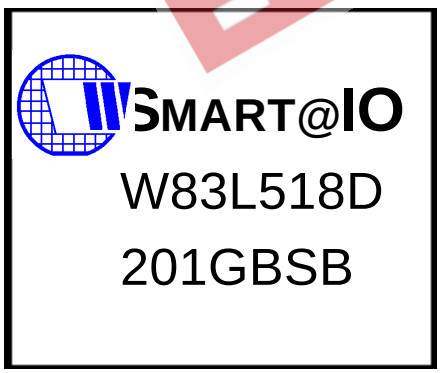
= 0 No debouunce.

= 1 Use debounce function.

7 ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83L518D	48-pin LQFP	

8 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the SMART@IO Trademark

2nd line: The chip part number.

3rd line: Tracking code 201 G B SB

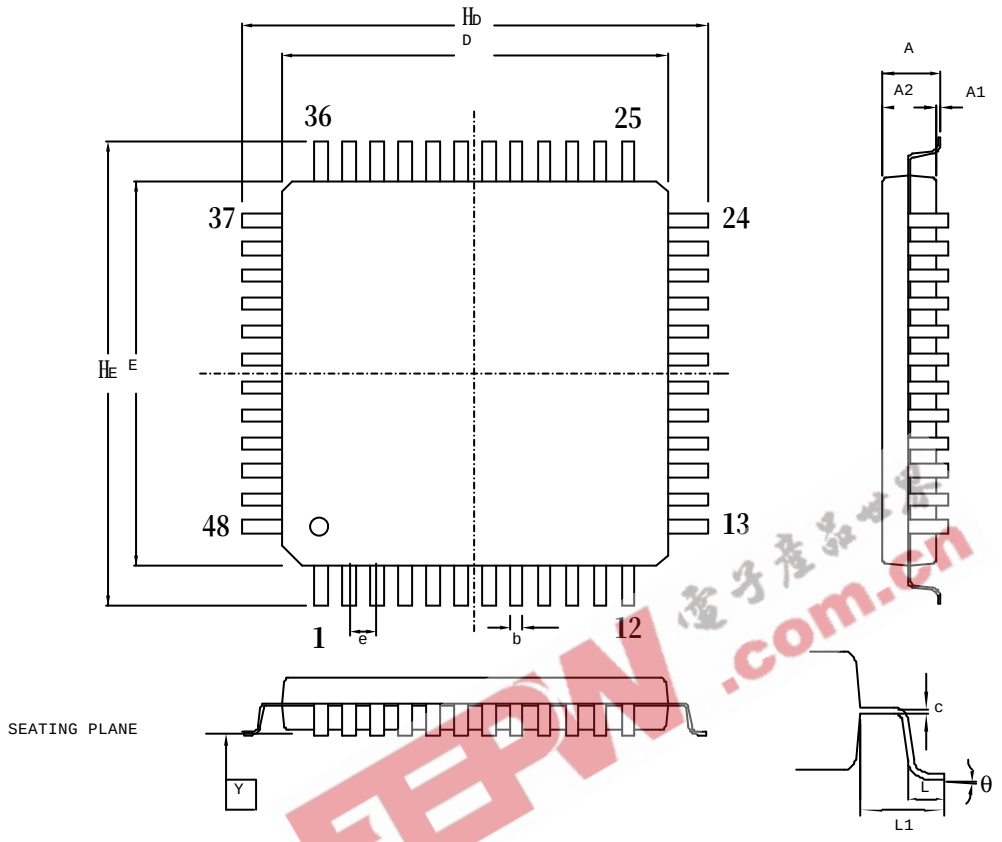
201: packages made in '02, week 01

G: assembly house ID; O means OSE, G means GR, …

BSB: IC revision

9 PACKAGE DRAWING AND DIMENSIONS

Package- 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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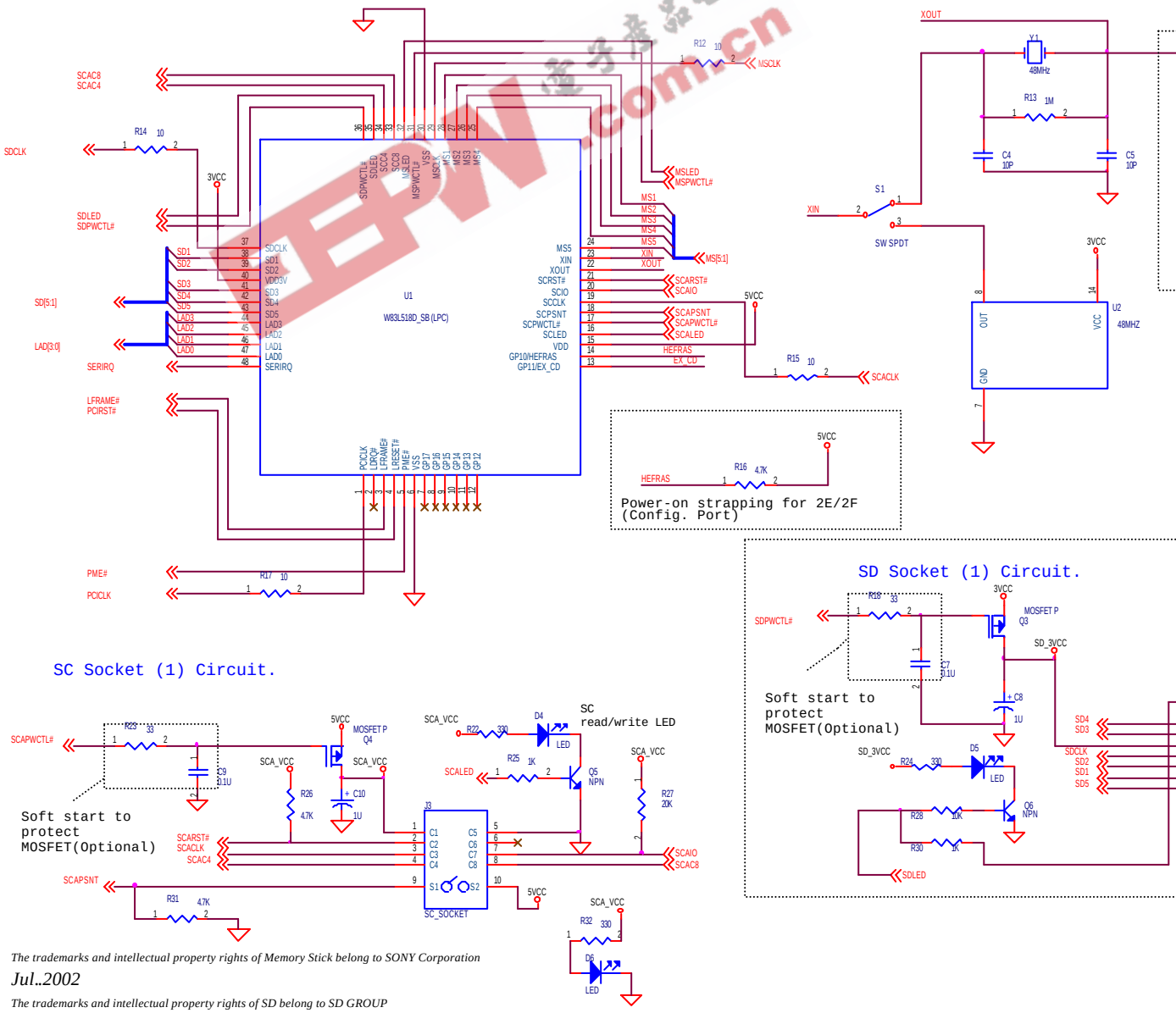
10 THE W83L518D SCHEMATIC



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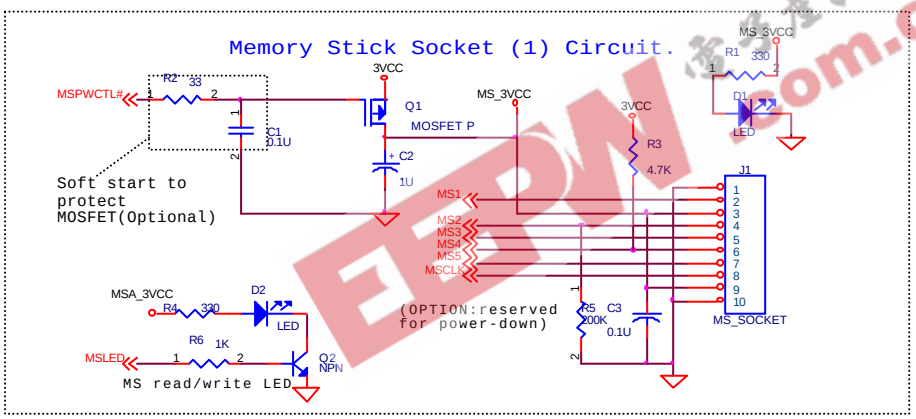
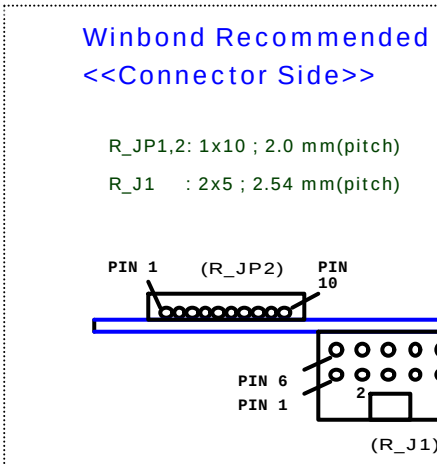
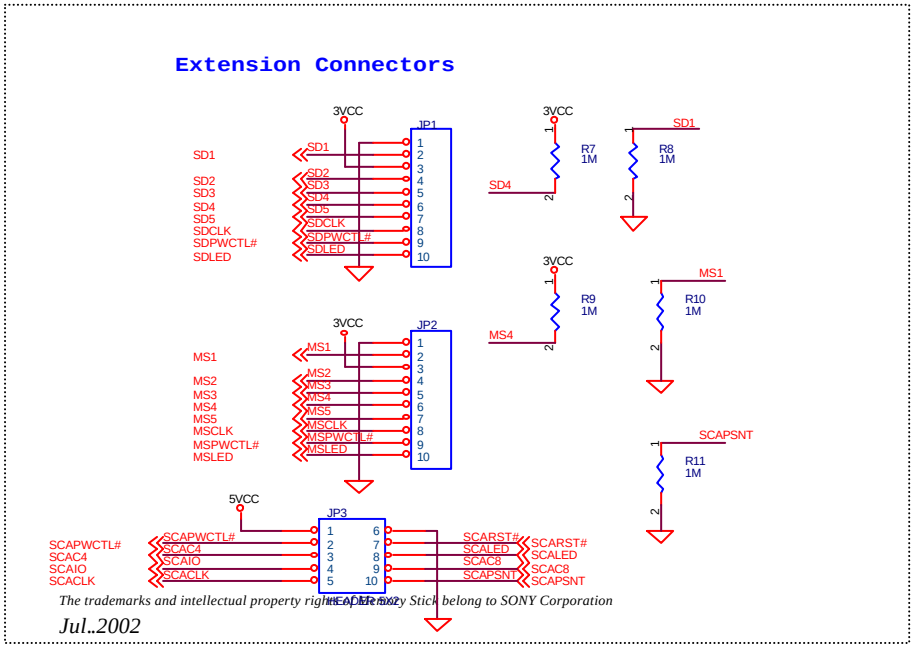
The W83L518D Schematic







Note 1: The RESET# should be connected with on PCI bus or LREST#on LPC bus(activ

Note 2: There is either function of SD and sockets interface can be implemented

Note 3: If any of SC or MS/SD function isn't SCPSNT/SCBPSNT should be tied to a p MS[5:2]/SD[5:2] to pull-high resisto consumption. (recommended: 4.7K-8.2

Note 4: The trade marks and intellectual pro Corporation.Information check: https

Note 5: If JP1,2,3,4 are designed for Winbon connector spec.
JP1,2: 1X10;pitch(2.0mm)
JP3: 2X5 ;pitch(2.54mm)

Note 6: For the recommended reader, please c CO.,LTD(http://www.tzt.com.tw)

Note 7: There are some difference as followi
(Ver 0.1 --> Ver 0.2)
(1)Added circuit(GP10/EX-CD)to imple
(2)Modified pulled-high resistor for
(3)Added configuration port selectio
(Ver 0.2 --> Ver 0.3)
(1)Added power-on strapping circuit
(2)Modified pull-down resistor tied

(Ver 0.3 --> Ver 0.4)
(1)Modified some erroneous netname
(2)DMA transaction cannot be support

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